Chefree Technology Corp.

TFT COLOR LCD MODULE

MODEL: CH123ZLXLWH-001

(Complied with RoHS)

LVDS interface

Version: P03

Customer : _____

Approved By : _____

Date: _____

CHEFREE		
APPROVAL	**CHECKER**	**PREPARE**
Tim	Mark	Jacky

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1. RECORD OF REVISION

Version	Revise Date	Page	Content	Author
V01	2020/11/26	all	Pre-spec, First release.	
V02	2020/11/30	all	updated some information.	
V03	2020/12/7	16	updated LVDS timing.	

2. General Description

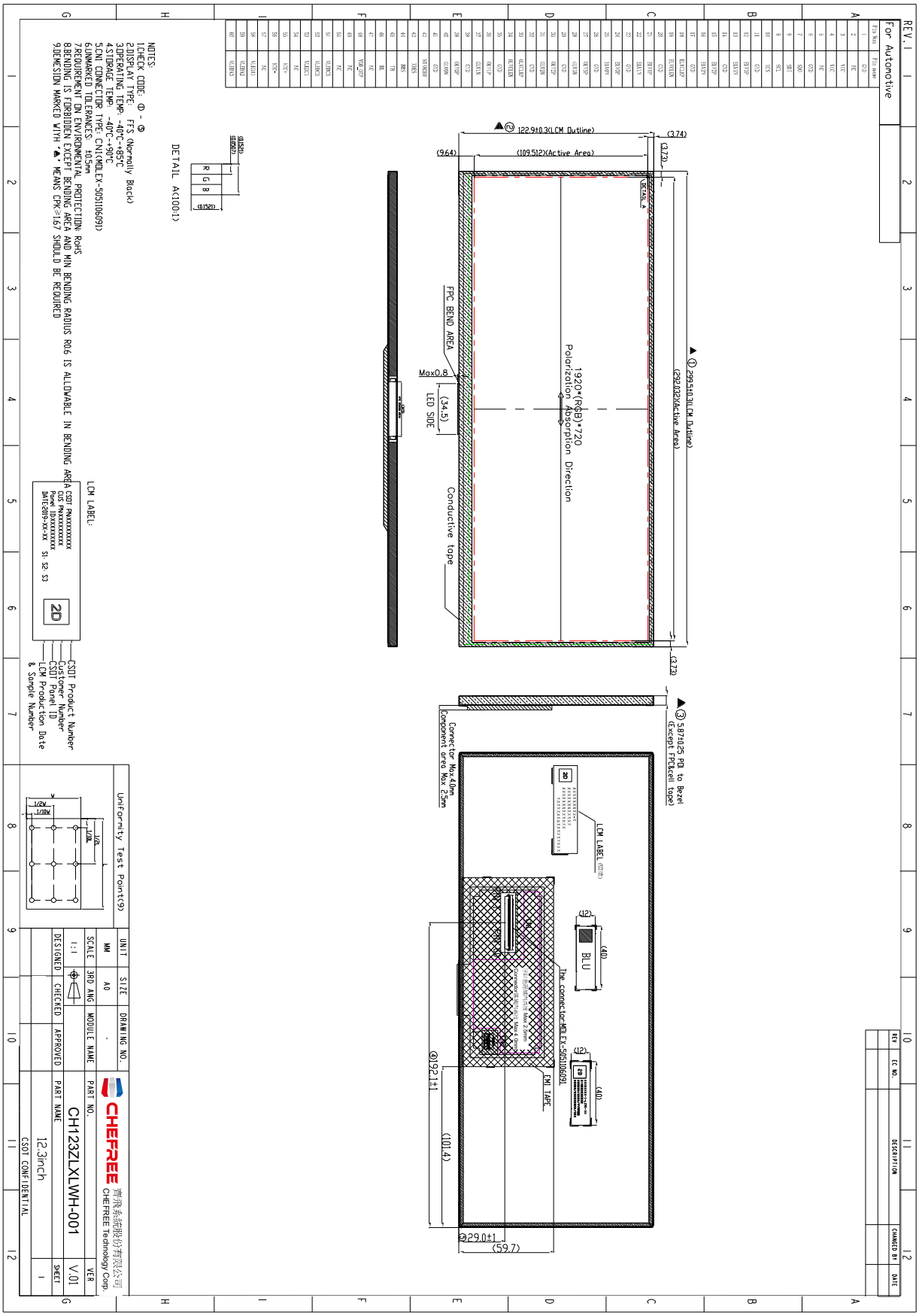
2.1 Introduction

The CH123ZLXLWH-001 is a color active matrix thin film transistor (TFT) liquid crystal display (LCD). This model is composed by LTPS LCD, Drive IC, FPC(flexible printed circuit),backlight unit.

2.2 Specifications Summary

No.	Item	Specification	Unit	Note
1	LCD size	12.3	inch	
2	Resolution	1920 x RGB x 720	--	
3	PPI	167		
4	Color pixel alignment	RGB Vertical Stripe		
5	TFT Technology	LTPS	--	
	Touch Technology	Without touch	--	For optical bonding
6	Display mode	Normal Black	--	
7	Active Area	292.032(W)*109.512(H)	mm	
8	Pixel pitch	0.1521 (W) * 0.1521 (H)	mm	
9	Aspect ratio	8:3		
10	LCM Outline Dimension	299.5(W)*122.9(H)*5.87(T)	mm	w/o protective film
11	Interface	Dual LVDS		
12	Color bit	24 bit		
13	Weight	(281)	g	
14	Polarizer surface treatment	HC		
15	Polarizer Surface hardness	Min 3H		
15	Environmental Protection Requirement	RoHS	--	

3. LCM Mechanism Diagram



4. Electrical Characteristics

4.1 LCM Typical Operation Condition

Parameter	Symbol	Value			Unit	Remarks(Ta=25℃)
		Min.	Typ.	Max.		
Power Supply for Logic	VCC	3.0	3.3	3.6	V	
Current for VCC	IVCC	--	TBD	200	mA	
Input voltage	VIH	0.7 *VCC		VCC+0.3	V	
	VIL	GND-0.3		0.3 *VCC	V	
Output voltage	VOH	VCC-0.4	-	-	V	
	VOL	GND	-	GND+0.4	V	
Frame Frequency	FR	--	60	--	Hz	

Note: The operations are guaranteed under the recommended operating conditions only. These operations are not guaranteed if a quick voltage change occurs during operation. To prevent noise, a bypass capacitor must be inserted into the line close to power pin.

4.2 BLU Typical Operation Condition

Item	Symbol	Min	Typ	Max	Unit	Remark
Forward Current	IBL		(90)		mA	Note1
Forward Voltage	VBL	(27)	(30)	(33)	V	
Backlight Power Consumption	P	-	(8.1)	-	W	
Lifetime	-	10000	30000	-	Hours	Note2,3,4

Table 4.2.1 LED backlight characteristics

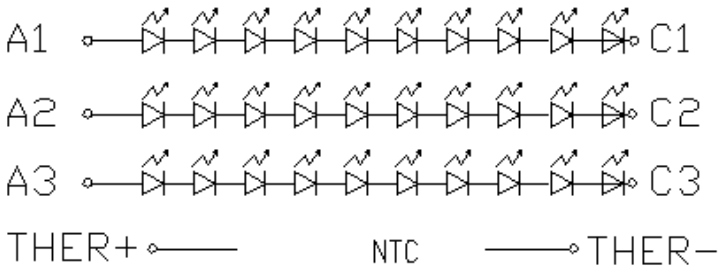


Figure 4.2.1 LED connection of backlight

Note1: IBL is defined for one channel LEDs.

Note2: Optical performance should be evaluated at Ta=25℃ only. If the LEDs are driven at high current or at high ambient temperature & humidity condition, the lifetime of the LEDs will be reduced. Operating lifetime means the brightness decrease to 80% of the original brightness at 10000H and decrease to 50% of the original brightness at 30000H.

Note3: NTC thermistor is included in the LED circuit and the part number is NCP15XH103F0SRC. It is used for measuring LED temperature and is located in the LED circuit on the backlight FPC.

Item	Value	Remarks
Type	NCP15XH103F0SRC	Murata
Resistance / Tolerance	10kΩ±1%	Ta=25°C
Permissive Operating Current	0.31mA	Ta=25°C

Table 4.2.2 Thermistor description Temperature and resistance relationship table

Temp. (° C)	Resistance (kΩ)
-40	195.652
-35	148.171
-30	113.347
-25	87.559
-20	68.237
-15	53.65
-10	42.506
-5	33.892
0	27.219
5	22.021
10	17.926
15	14.674
20	12.081
25	10
30	8.315
35	6.948
40	5.834
45	4.917
50	4.161
55	3.535
60	3.014
65	2.586
70	2.228
75	1.925
80	1.669
85	1.452
90	1.268
95	1.11
100	0.974
105	0.858

110	0.758
115	0.672
120	0.596
125	0.531

Note4: Derating curve will be updated when sample phase.

4.3 Module pin define

FPC Pin Assignment. (Connector: Molex 5051106091)

PIN	SYMBOL	FUNCTION	I/O/P	Remarks
1	GND	Ground	P	
2	NC	No connection	-	
3	VCC	Power supply, TYP 3.3V, Max current 200mA	P	
4	VCC	Power supply, TYP 3.3V, Max current 200mA	P	
5	NC	No connection	-	
6	GND	Ground	P	
7	SDO	SPI interface serial data output signal	O	
8	SDI	SPI interface serial data input signal	I	
9	SCL	SPI interface CLK signal	I	
10	XCS	SPI interface CS signal	I	
11	GND	Ground	P	
12	ELV3P	(LVDS) EVEN LVDS data 3+	I	
13	ELV3N	(LVDS) EVEN LVDS data 3-	I	
14	GND	Ground	P	
15	ELV2P	(LVDS) EVEN LVDS data 2+	I	
16	ELV2N	(LVDS) EVEN LVDS data 2-	I	
17	GND	Ground	P	
18	ELVCLKP	(LVDS) EVEN LVDS clock +	I	
19	ELVCLKN	(LVDS) EVEN LVDS clock -	I	
20	GND	Ground	P	
21	ELV1P	(LVDS) EVEN LVDS data 1+	I	
22	ELV1N	(LVDS) EVEN LVDS data 1-	I	
23	GND	Ground	P	
24	ELV0P	(LVDS) EVEN LVDS data 0+	I	
25	ELV0N	(LVDS) EVEN LVDS data 0-	I	
26	GND	Ground	P	
27	OLV3P	(LVDS) ODD LVDS data 3+	I	
28	OLV3N	(LVDS) ODD LVDS data 3-	I	
29	GND	Ground	P	

30	OLV2P	(LVDS) ODD LVDS data 2+	I	
31	OLV2N	(LVDS) ODD LVDS data 2-	I	
32	GND	Ground	P	
33	OLVCLKP	(LVDS) ODD LVDS clock +	I	
34	OLVCLKN	(LVDS) ODD LVDS clock -	I	
35	GND	Ground	P	
36	OLV1P	(LVDS) ODD LVDS data 1+	I	
37	OLV1N	(LVDS) ODD LVDS data 1-	I	
38	GND	Ground	P	
39	OLV0P	(LVDS) ODD LVDS data 0+	I	
40	OLV0N	(LVDS) ODD LVDS data 0-	I	
41	GND	Ground	P	
42	STANDBY	Standby mode setting pin, STANDBY=L, standby by mode, Driver IC timing controller, output buffer, DAC and power circuit all off. STANDBY=H, Normal operation, Refer to Power on/off sequence for detail control requirement.	I	
43	XRES	Hardware reset signal, XRES=L, reset, XRES=H, normal operation. Refer to Power on/off sequence and reset timing for detail control requirement.	I	
44	BRS	fail_detect output	O	
45	TB	Vertical shift direction select	I	Note3
46	RL	Horizontal shift direction select	I	Note3
47	NC	No connection	-	
48	VDD_OTP	OTP power supply, Customer side NC	P	
49	NC	No connection	-	
50	NC	No connection	-	
51	VLEDK3	Backlight power supply Cathode	P	
52	VLEDK2	Backlight power supply Cathode	P	
53	VLEDK1	Backlight power supply Cathode	P	
54	NC	No connection	-	
55	NTC+	Thermal Sensor	P	
56	NTC-	Thermal Sensor	P	
57	NC	No connection	-	
58	VLEDA1	Backlight power supply Anode	P	
59	VLEDA2	Backlight power supply Anode	P	
60	VLEDA3	Backlight power supply Anode	P	

Note1: I: input ; O: output; P: Power

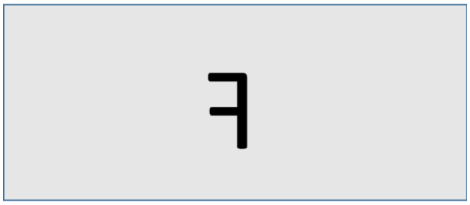
Note2: Connector is located on display rear side.

Note3: RL/TB pin control the source and gate scan direction.

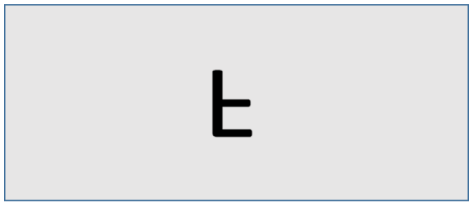
RL=1, Scan direction: S1->S2->...->S2160, RL=0, Scan direction: S2160->S2159->...->S1.

TB=1, Scan direction: Top->Bottom, TB=0, Scan direction: Bottom->TOP.

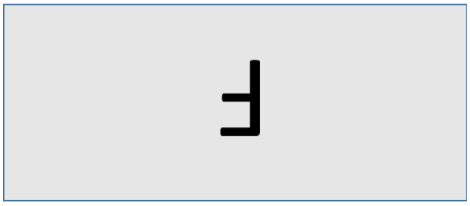
TB=H, RL=H



TB=H, RL=L



TB=L, RL=H



TB=L, RL=L

4.4 Timing Description

1) OVERVIEW

This LCD module is equipped with two kind of Interfaces used for transferring of command data and pixel data.

2) SPI interface

- SPI interface is used for command transmission.

3) LVDS

- 8 pairs for transferring of pixel data (OLV3P/N~ OLV0P/N, ELV3P/N~ ELV0P/N)
- 2 pairs of clock (ELVCLKP/N and OLVCLKP/N)

4) SERIAL INTERFACE

Signal Definition

Signal	Description
CS	Chip select signal
SCL	Serial clock signal
SDI	Serial data input signal
SDO	Serial data output signal

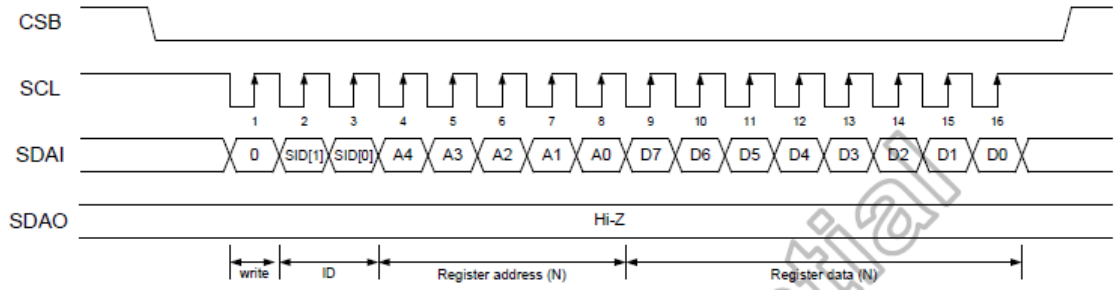


Figure 3.1: SPI signals, normal read mode for 4-wire

5) Reset timing

11.2.6 Reset timing

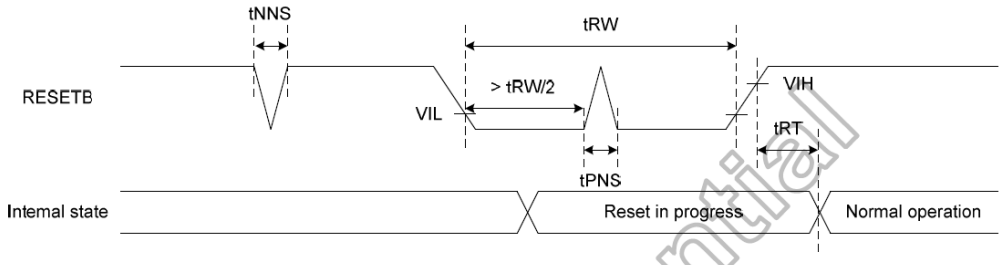


Figure 11.7: Reset input timing

(VDD1=VDD2=3.0 to 3.6V, GND=0V, T_A=-40 to +105 ℃)

Signal	Parameter	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
RESETB	Reset pulse width	tRW	15	-	-	μs
	Reset complete time	tRT	-	-	5	μs
	Positive spike noise width	tPNS	-	-	100	ns
	Negative spike noise width	tNNS	-	-	100	ns

Table 11.5: Reset timing parameter

Figure 3.2: Reset input timing

4.5 COMMANDS

<TBD>

4.6 OUTPUT SIGNAL CHARACTERISTICS OF BRS

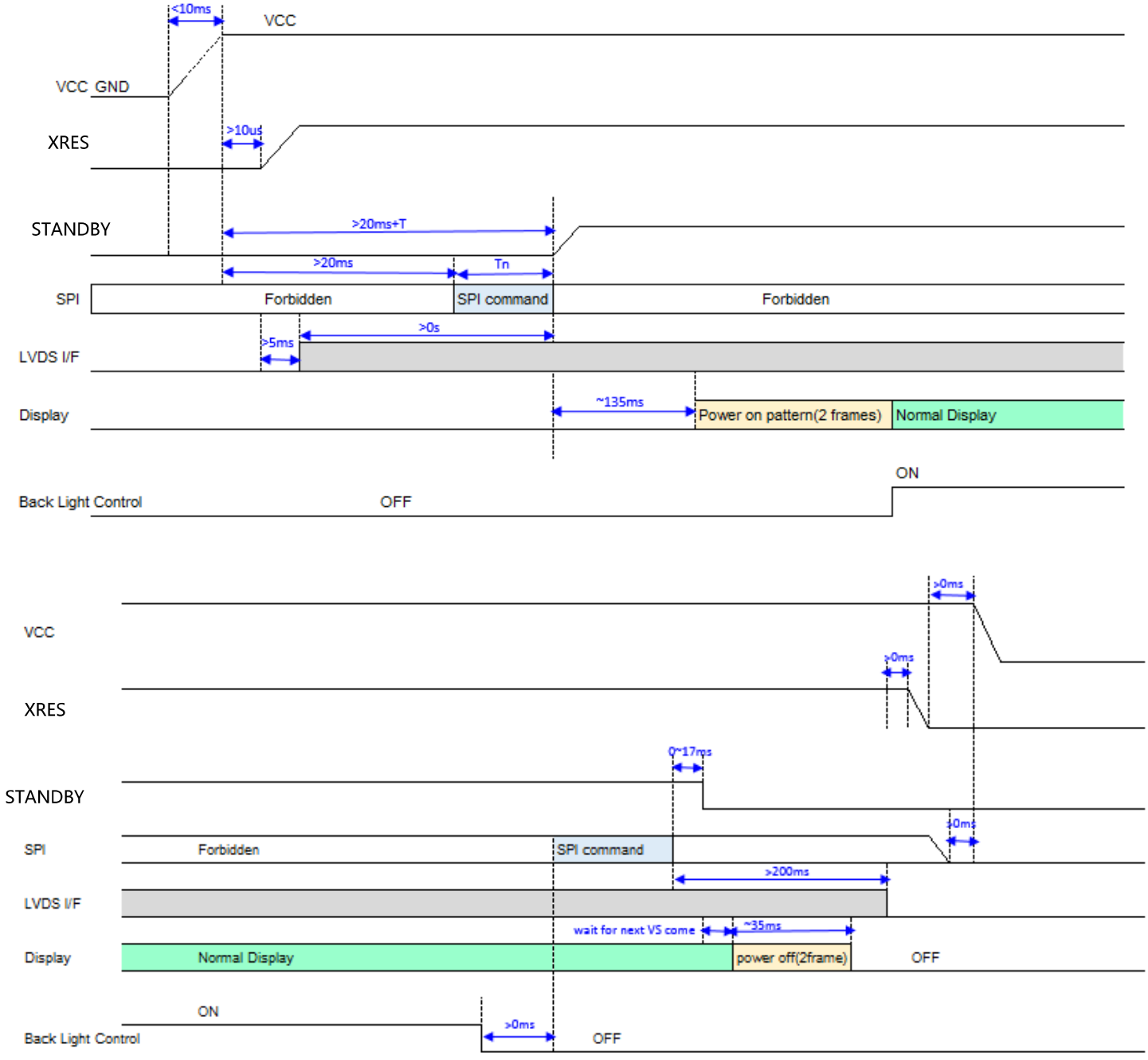
Fail_DET output	Status	Remarks
Low	Abnormal	--
High	Normal	--

Abnormal status Description:

Item	Detection type	Causes	Action	Detection period
1	OTP trimming fail	OTP's value mismatch with register's value	None	After OTP trimming
2	EEPROM reload fail	EEPROM's header or checksum fail	None	Each EEPROM reload
3	Inputted signals fail	CLK/HS/VS/DE lose	Enter Self protection mode **(refer to Section 7.6.2)**	Real-time
4	Tradition Gate fail	Gate driver signal fail	None	Per frame
5	Source fail	Source driver signal fail	None	Per line
6	Power fail	VCC1/VSP/VSN voltage too low	Enter GAS function **(refer to Section 7.6.1)**	Real-time
7	LVDS fail	LVDS-RX unlock	Enter Self protection mode **(refer to Section 7.6.2)**	Real-time
8	OTP reload fail	OTP reload values mistake	None	Real-time

5. ELECTRICAL SPECIFICATION

5.1 Power on/off sequence (For reference, will be updated when design phase)



5.2 DC CHARACTERISTICS OF LVDS

(VCC= 3.0V to 3.6V, VSS=0V, T_A=-40~85℃)

Parameter	Symbol	Condition	Rating			Unit	Remarks
			Min.	Typ.	max.		
Differential threshold high	VTH	VCM=1.2V	+100	--	--	mV	

voltage							
Differential threshold low voltage	VTL	VCM=1.2V	--	--	-100	mV	
Input differential voltage	VID		100	--	600	mV	
Common voltage	VCM		1	1.2	1.7-|VID|/2	V	
Termination resistor	RTRM		TBD	100	TBD	ohm	

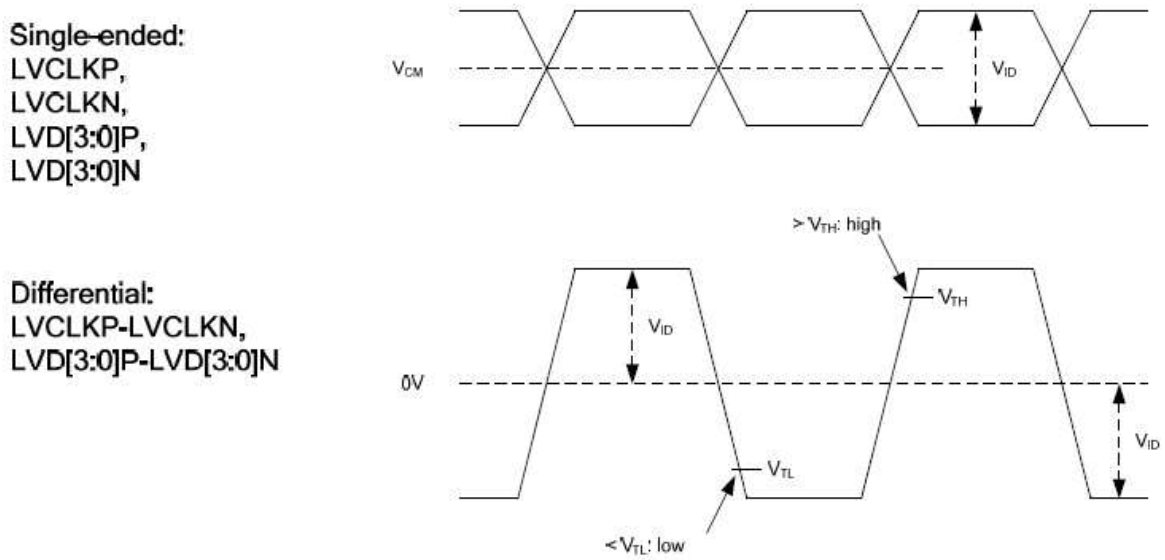


Figure 4.1: LVDS mode DC electrical characteristics

5.3 LVDS mode AC electrical characteristics

(VCC=3.0V to 3.6V, VSS =0V, T_A=-40~85℃)

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Clock frequency(1-port/2-port)	F_{LVCYC}	15	-	105/110	MHz
Clock period(1-port/2-port)	T_{LVCYC}	9.52/9.09			ns
1data bit time	UI	-	1/7		T_{LVCYC}
Clock high time	T_{LVCH}	-	4		UI
Clock low time	T_{LVCL}	-	3		UI
Position 1	T_{POS1}	-0.2	0	0.2	UI
Position 0	T_{POS0}	0.8	1	1.2	UI
Position 6	T_{POS6}	1.8	2	2.2	UI
Position 5	T_{POS5}	2.8	3	3.2	UI
Position 4	T_{POS4}	3.8	4	4.2	UI
Position 3	T_{POS3}	4.8	5	5.2	UI
Position 2	T_{POS2}	5.8	6	6.2	UI
Input eye width	T_{EYEW}	0.6	-	-	UI
Input eye border	T_{EX}	-0.2	0	0.2	UI
LVDS wake up time	T_{ENLVDS}	-	-	150	ms
LVDS clock to clock skew	T_{skew_EO}	-1/7	-	1/7	UI

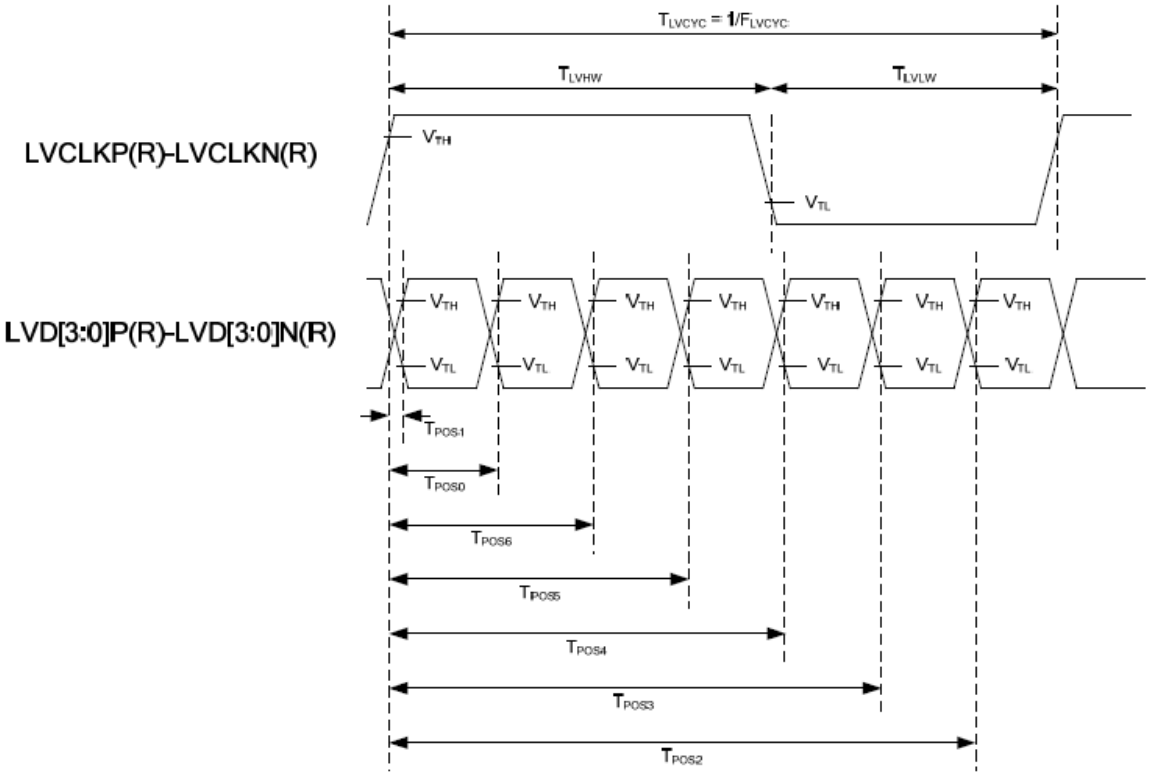


Figure 4.3.1: LVDS input timing

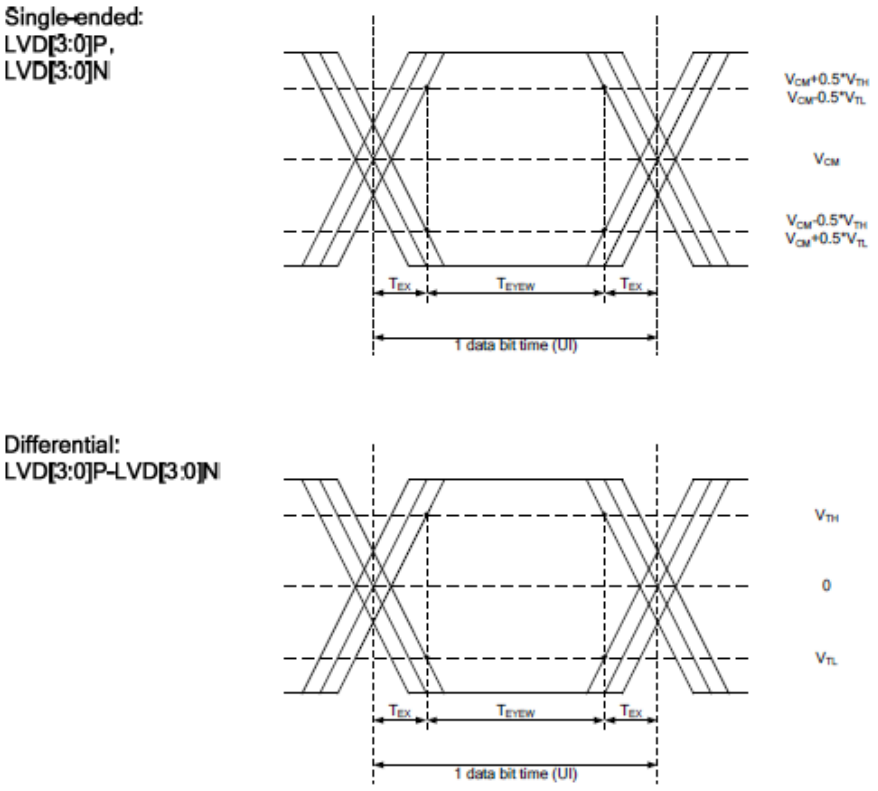


Figure 4.3.2: LVDS input eye diagram

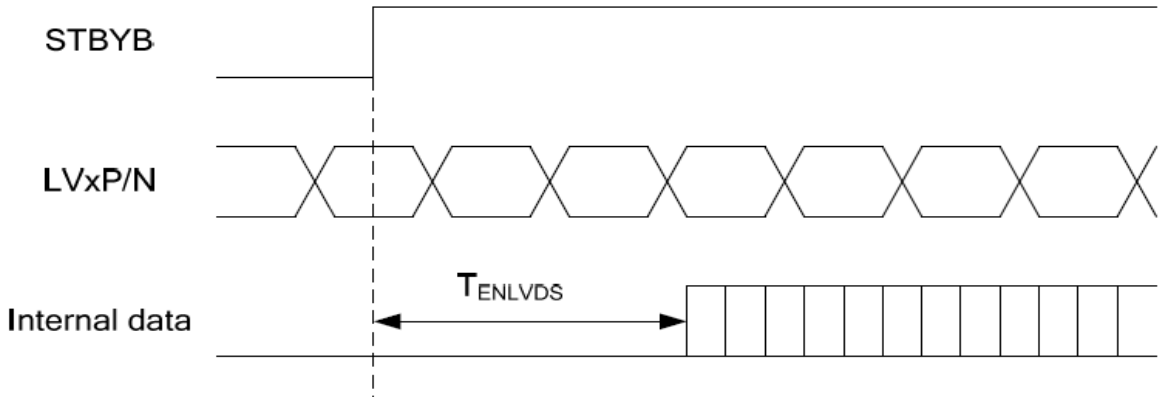


Figure 4.3.3: LVDS wake up time

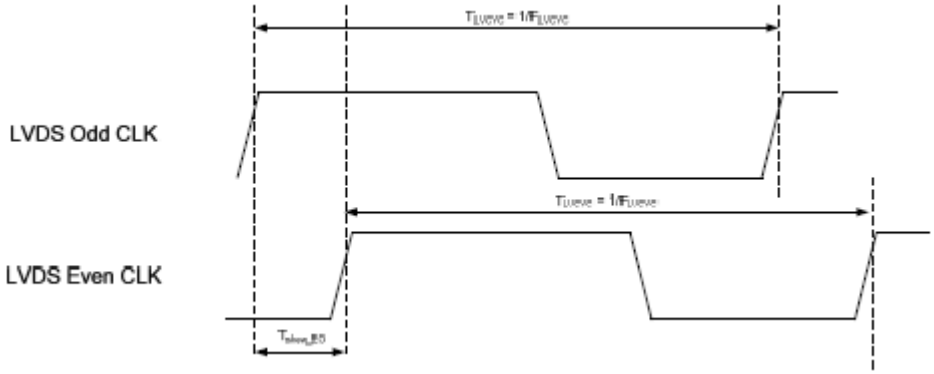


Figure 4.3.4: LVDS clock to clock skew

5.4 LVDS with SSC

The LVDS receiver can support spread spectrum clock (SSC). Limitation is listed as below.

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Modulation frequency(1)	SSCMF	LVDS clock frequency center at 105MHz	FDCLK / th *1000	10.1	200	KHz
		LVDS clock frequency center at 80MHz	FDCLK / th *1000		200	KHz
		LVDS clock frequency center at 60MHz	FDCLK / th *1000		150	KHz
		LVDS clock frequency center at 40MHz	FDCLK / th *1000		159	KHz
		LVDS clock frequency center at 20MHz	FDCLK / th *1000		100	KHz
		LVDS clock frequency center at 15MHz	FDCLK / th *1000		100	KHz
Modulation rate	SSCMR	LVDS clock frequency + SSCMR in the range of 15MHZ~105Mhz			±3	%

Note: (1) For example, FDCLK is 90.84MHz for 1920xRGBx720 resolution, th (period of line) is 1992 DCLK, thus SSCMF should be larger than 92.84MHz/1992*1000 = 46.6kHz (which is 1/th).

Table 11.3: SSC limitation of LVDS interface

5.5 LVDS Input / Output Timing

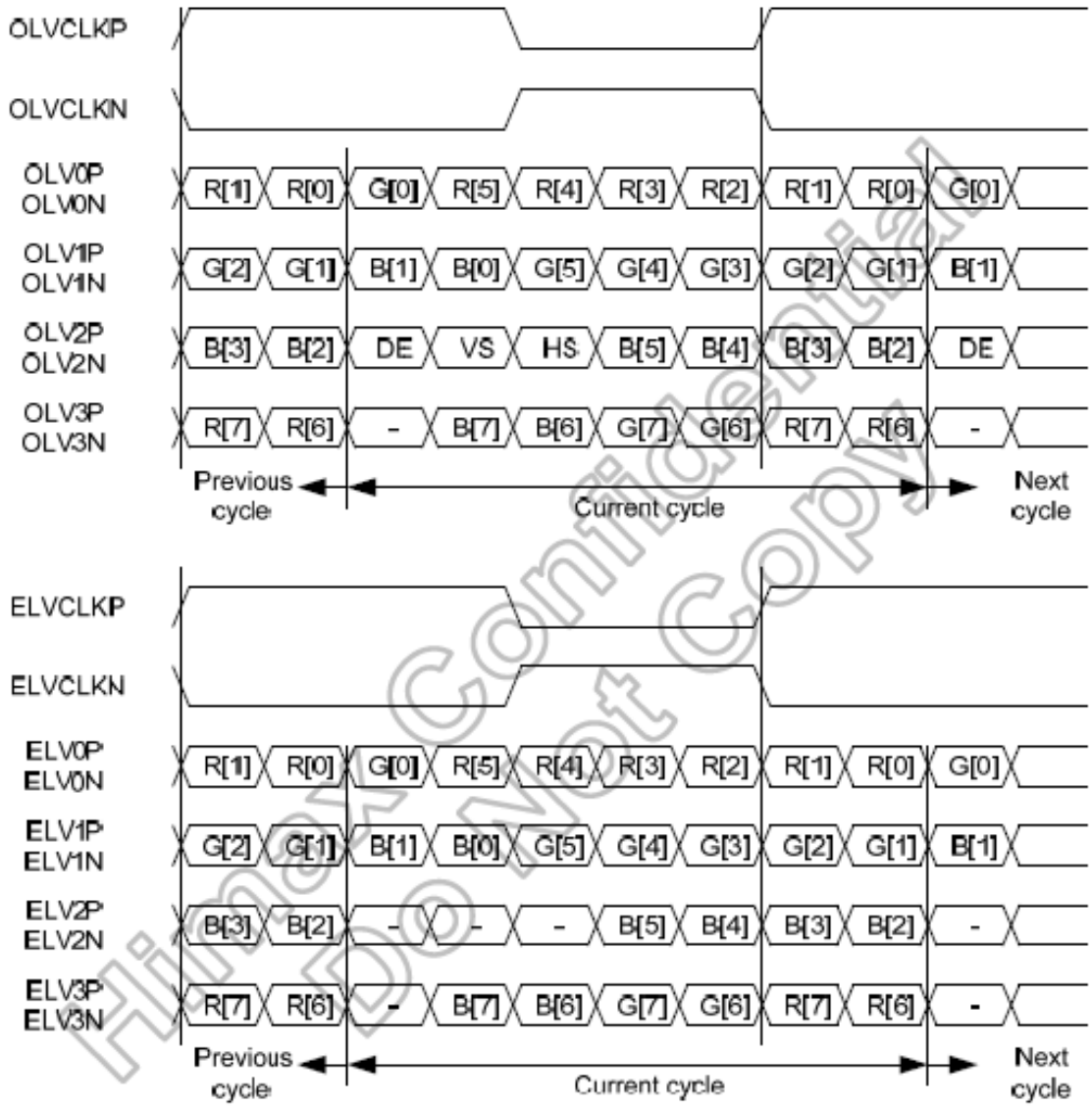


Figure 4.5.2: 2-port LVDS signals, VESA format, 8-bit mode

Parameter	Symbol	1920xRGBx720			Unit
		Min.	Typ.	Max.	
CLK frequency	FCLK		47.06		MHZ
Horizontal valid data	thd		960		CLK
Hsync pulse Width	thpw	6	12	254	CLK
Hsync back porch	thbp	7	16	255	CLK
Hsync front porch	thfp	46	56	-	CLK
1 horizontal line	th	1013	1032	1440	CLK
Vertical valid data	tvd		720		H
Vsync pulse width	tvpw	1	3	254	H

Vsync back porch	tvbp	2	24	255	H
Vsync front porch	tvfp	6	16	-	H
1 vertical field	tv	728	760	1080	H
Frame rate	FR	-	60	-	Hz

Note: (1) FR (Frame rate)=FCLK / th / tv.

(2) Horizontal back-porch could be adjusted at Sync mode by register R07h of page 0.

(3) Vertical back-porch could be adjusted at Sync mode by register R06h of page 0.

(4) th=thbp + thfp + thd and tv=tvbp + tvfp + tvd.

6. Optical Specification

Item	Symbol	Condition	Values			Unit	Notes
			Min.	Typ.	Max.		
Luminance	L	25deg.C	800	1000	/	cd/m²	Perpendicular Note 2,
Contrast Ratio	CR	25deg.C	1100	1500	/	/	Perpendicular Note 2,4
Viewing angle (CR≥ 10)	/	Φ=0/90/180/270(deg.)	80	85	/	/	Note 1,2
Response time	Ton+ Toff	Ta=25deg.C	/	/	20	ms	Note 2,3
		Ta=-20deg.C	/	/	200		
		Ta=-30deg.C	/	/	350		
	GTG	Ta=25deg.C	/	/	25		
		Ta=-20deg.C	/	/	210		
		Ta=-30deg.C	/	/	430		
Color Gamut	NTSC	/	70%	75%	/	/	Note 2,5
Gamma	/	25℃	1.9	2.2	2.5	/	Note 2
		-30~50℃	1.9	2.2	2.5	/	
Color chromaticity (CIE1931)	Wx	/	-0.040	0.302	+0.040	/	Note 2,5
	Wy	/		0.328			
	Rx	/	-0.030	0.649	+0.030		
	Ry	/		0.345			
	Gx	/		0.307			
	Gy	/		0.632			
	Bx	/		0.153			
	By	/		0.063			
White Luminance homogeneity	YU	9points	80%	/	/	/	Note 2,6
Black Luminance homogeneity	YU	9points	50%	/	/	/	Note 2,6
Reflectivity	SCI	D65 @Center (360~740nm)	/	/	6.2	%	Note 2
L	/		28.56	29.56	30.56	/	
a*	/		-0.88	0.12	1.12	/	
b*	/		-2.1	-1.1	-0.1	/	
Flicker	/	Center	/	/	-25	dB	Note 2,7

Test Conditions:

①VCC=3.3V, the ambient temperature is 25℃.

②All input terminals LCD panel must be ground while measuring the center area of the panel. The LED driving condition is IL=90mA.

③The test systems refer to Note 2.

Note 1: Definition of viewing angle range.

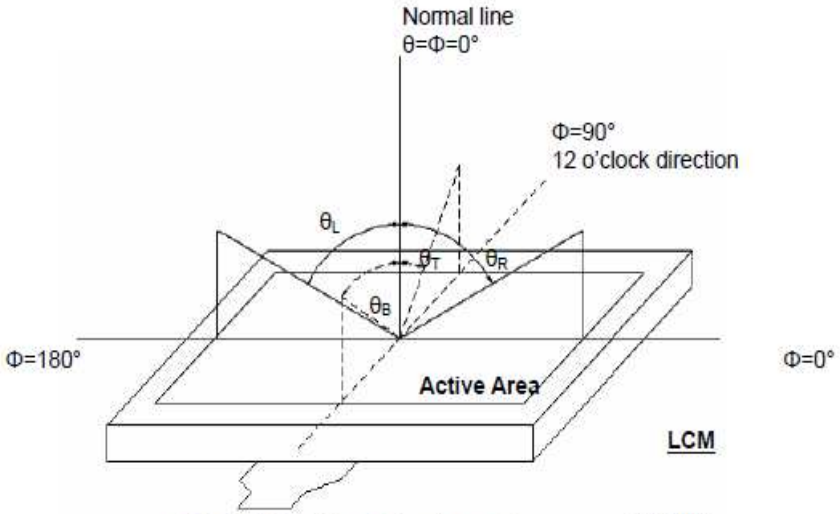


Fig. 4-1 Definition of viewing angle

Note 2: Definition of optical measurement system.

The optical characteristics should be measured in dark room. The optical properties are measured at the center point of the LCD screen. (Viewing angle is measured by CS2000A/Height :500mm，or EZ Contrast MS88, Response time @25℃ is measured by Optiscope 200, Flicker &Gamma are measured by CA310，Reflectivity is measured by CM3600A，other items are measured by CS2000A or CS2000/ Field of view: 1°/Height: 500mm.)

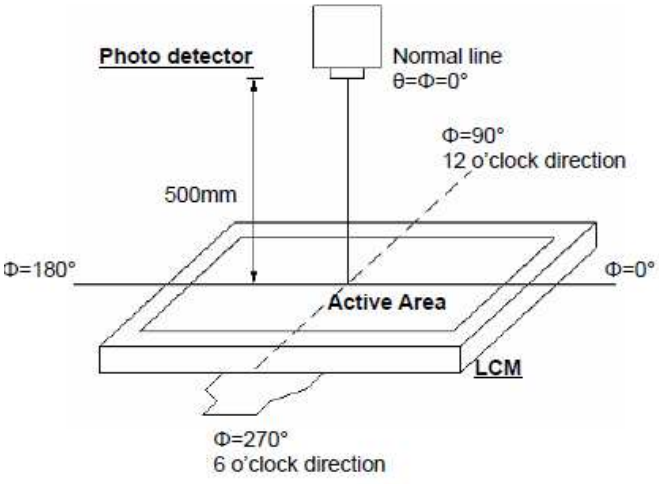
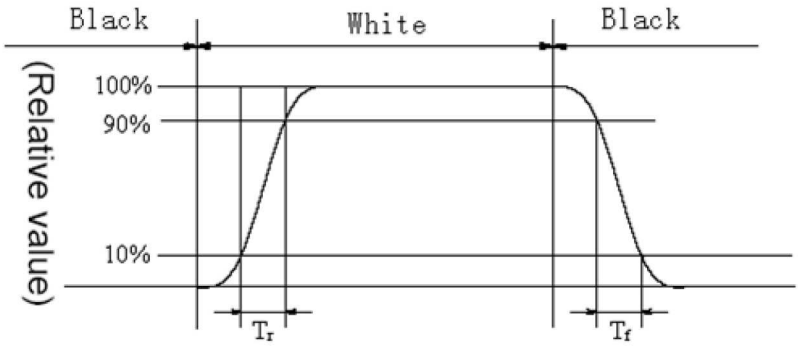


Fig. 4-2 Optical measurement system setup

Note 3: Definition of Response time

The response time is defined as the LCD optical switching time interval between "White" state and "Black" state. Rise time (TON) is the time between photo detector output intensity changed from 10% to 90%. And fall time (TOFF) is the time between photo detector output intensity changed from 90% to 10%.



Note 4: Definition of contrast ratio

Contrast ratio (CR) = Luminance measured when LCD on the "White" state/ Luminance measured when LCD on the "Black" state

Note 5: Definition of color chromaticity

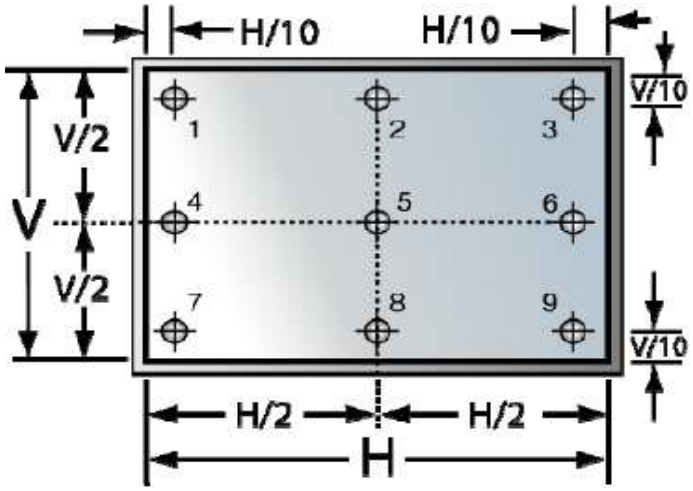
Color coordinates measured at center point of LCD.

Note 6: Definition of Luminance Uniformity

Measure the luminance of gray level 255 or L0 at 9 points

δW 9p = {Minimum [L (1)+ L (2)+ L (3)+ L (4)+ L (5)+ L (6)+ L (7) +L (8) +L (9)] /

Maximum [L (1)+ L (2)+ L (3)+ L (4)+ L (5)+ L (6)+ L (7) +L (8) +L (9)]}*100%

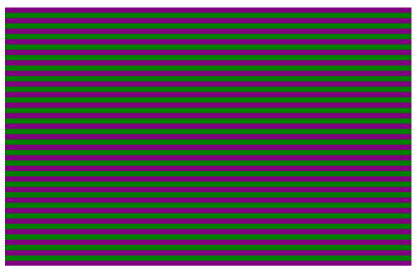


Note 7: Definition of Flicker

Flicker measured with CA310，and it should be measured with flicker pattern at the center point of the LCD.

Flicker measured with the way of JEITA at 30Hz.

Flicker pattern: Column Inversion.



7. Reliability Test Item

No.	Test Item	Test Condition	Standard
1	High Temperature Operation	85℃ 504H	Note1
2	High Temperature Storage	90℃ 504H	Note1
3	Low Temperature Storage	-40℃ 504H	Note1
4	Low Temperature Operation	-40℃ 504H	Note1
5	High Temperature and Humidity Operation	60℃,90%RH 504H	Note1
6	Thermal Shock (non-Operation)	-40℃/30min~85℃/30min~,300cycle Change time 30s	Note1
7	Vibration (non-Operation)	Frequency:8-33.3Hz Total amplitude:1.3mm Frequency:33.3-400Hz Acceleration:29.4m/s² sweep time 15minutes 2hours each for X and Z, directions, 4hours for Y, directions	Note2
8	Shock (non-Operation)	100G(g=9.8m/m2), 6 ms;10 Times in Each Direction(+/-X,+/-Y,+/-Z)	Note2
9	Static load (non-Operation)	Press the center of LCM with pan silicon rubber head (diameter of 15 mm). Pressure 50N for 1 seconds，30 N force for 8 h	Note2
10	ESD	LCD power on. Contact mode：150pF 330Ω ±6 KV ,class B; ±8 KV class B; Air mode：150pF 330Ω ±15KV Class B (考察整個系統要求，無顯示功能失效)	Note2
11	Image Sticking	Burn in: Checkerboard, 1h @+65°C Test: 50% Grey (release 2min， L2)	

Note1： After this test has been done 2 hours , a display is rejected when one of the following defects occurs:

- more than 50% contrast reduction after HTO 500hrs test .
- doubling of specified maximum total power consumption
- more than 30% reduction of the original brightness & contrast after lifetime（25℃）operating test
- For operating test regular visual inspection to be performed within test duration
- Test 1~5 after 504H continued to 1000 Hours, only function assurance, support test result , no speciation assurance.

Note2： After this test has been done, the specimen should function normally without any fatal defect (no picture, line defect, out of synchronization).

8. Incoming inspection sheet

No.	**Major Defect**	Inspection standards (acceptable level)
1	Function defect	RGB timing error(correlate drived) Wrong color/Less brightness (Out of Optical Spec) No backlight or other part missing Broken glass caused abnormal or no display NOT allowed
2	Abnormal display	Abnormal operation including distinct RGB line defects and white line defect Vertical or horizontal stripes Yellow Border variation of film thickness from bonding (white picture, 1h heat up at +85°C, no visible yellow border) Inhomogeneous color of the background (except Mura) NOT allowed

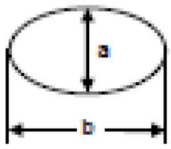
No.	**Minor Defect**	Inspection standards (acceptable level)
1	Black spots (Extraneous substances)	Inspection mode: white picture φ≤0.15 Not counted 0.15 ﹤φ ≤ 0.35 N≦3 (distance≥12mm) 0.35 ﹤φ NG
2	White spots (Extraneous substances)	Inspection mode: black picture φ≤0.15 Not counted 0.15 ﹤φ ≤ 0.35 N≦3 (distance≥12mm) 0.35 ﹤φ NG
3	Bright + black dots (Pixel Defect)	<table><tr><th>Item</th><th>Bright dot (sub-pixel)</th><th>Black dot (sub-pixel)</th><th>Total</th></tr><tr><td>Defect in Screen</td><td>0</td><td>4 (distance≥12mm)</td><td>4</td></tr></table> Bright and Black dot area covering more than 50% of sub pixel: NOK Bright and Black dot area covering less than or equal 50% of sub pixel: OK
4	Lint	Operating (black picture position) w≦0.03 and L<3.0 Not counted 0.03<w≦0.05 and L≦3 N≦2 0.05<w or L >3.0 NG

5	Scratches	Operating (black picture position) w≦0.03 Not counted 0.03<w≦0.05 and L≦3.0 N≦2 0.05<w or L >3.0 NG
6	Dent/Bubble	Dent and Bubble on polarizer φ <0.15 Not counted 0.15 ≤φ ≤ 0.35 N≦3 0.35 < φ NG
7	Mura	Pattern: Black raster（L0/255） -Put 5% ND filter on LCD surface,100lux max -Judgment Mura which can be seen through 5%ND filter,100lux max not allowed 

Note1)

Average diameter : D(mm)

D=(a+b)/2



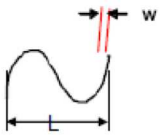
Note2)

Length: L (mm)

L = longest point

Width : w(mm)

w=Line width



9. General Precautions

1) Safety

Liquid crystal is poisonous. Do not put it in your mouth. If liquid crystal touches your skin or clothes, wash it off immediately by using soap and water.

2) Handling

The LCD panel is plate glass. Do not subject the panel to mechanical shock or to excessive force on its surface.

The polarizer attached to the display is easily damaged. Please handle it carefully to avoid scratch or other damages.

To avoid contamination on the display surface, do not touch the module surface with bare hands.

Keep a space so that the LCD panels do not touch other components.

Put cover board such as acrylic board on the surface of LCD panel to protect panel from damages.

Transparent electrodes may be disconnected if you use the LCD panel under environmental conditions where the condensation of dew occurs.

Do not leave module in direct sunlight to avoid malfunction of the ICs.

3) Static Electricity

Be sure to ground module before turning on power or operating module.

Do not apply voltage which exceeds the absolute maximum rating value.

4) Storage

Store the module in a dark room where must keep at 25±10□ and 65%RH or less.

Do not store the module in surroundings containing organic solvent or corrosive gas.

Store the module in an anti-electrostatic container or bag.

5) Cleaning

Do not wipe the polarizer with dry cloth. It might cause scratch.

Only use a soft sloth with IPA to wipe the polarizer, other chemicals might permanent damage to the polarizer.