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April 2014

FQA13N80_F109

N-Channel QFET® MOSFET

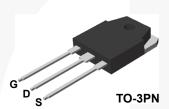
800 V, 12.6 A, 750 m Ω

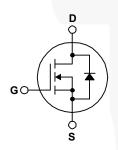
Description

This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.

Features

- 12.6 A, 800 V, $R_{DS(on)}$ = 750 m Ω (Max.) @ V_{GS} = 10 V, I_D = 6.3 A
- Low Gate Charge (Typ. 68 nC)
- · Low Crss (Typ. 30 pF)
- · 100% Avalanche Tested





Absolute Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol	Parameter		FQA13N80_F109	Unit
V _{DSS}	Drain-Source Voltage		800	V
I _D	Drain Current - Continuous (T _C = 25°C)		12.6	Α
	- Continuous (T _C = 100°C)		8.0	Α
I _{DM}	Drain Current - Pulsed	(Note 1)	50.4	Α
V _{GSS}	Gate-Source Voltage		± 30	V
E _{AS}	Single Pulsed Avalanche Energy	1100	mJ	
I _{AR}	Avalanche Current (N		12.6	Α
E _{AR}	Repetitive Avalanche Energy (Note		30	mJ
dv/dt	Peak Diode Recovery dv/dt	4.0	V/ns	
P _D	Power Dissipation (T _C = 25°C)		300	W
	- Derate above 25°C	2.38	W/°C	
T _J , T _{STG}	Operating and Storage Temperature Range	-55 to +150	°C	
T _L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	°C	

Thermal Characteristics

Symbol	Parameter	FQA13N80_F109	Unit	
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	0.42	°C/W	
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink, Typ.	0.24	°C/W	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	40	°C/W	

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FQA13N80_F109	FQA13N80	TO-3PN	Tube	N/A	N/A	30 units

Electrical Characteristics T_C = 25°C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Тур	Max	Unit
Off Charac	teristics					ı
BV _{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_{D} = 250 μ A	800			V
ΔBV _{DSS} / ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C		0.95		V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 800 V, V _{GS} = 0 V			10	μА
		V _{DS} = 640 V, T _C = 125°C			100	μА
I _{GSSF}	Gate-Body Leakage Current, Forward	V _{GS} = 30 V, V _{DS} = 0 V			100	nA
I _{GSSR}	Gate-Body Leakage Current, Reverse	V _{GS} = -30 V, V _{DS} = 0 V			-100	nA
On Charact	teristics					
V _{GS(th)}	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	3.0		5.0	V
R _{DS(on)}	Static Drain-Source On-Resistance	$V_{GS} = 10 \text{ V}, I_D = 6.3 \text{A}$		0.58	0.75	Ω
g _{FS}	Forward Transconductance	$V_{DS} = 50 \text{ V}, I_{D} = 6.3 \text{A}$		13		S
Dynamic C	haracteristics					
C _{iss}	Input Capacitance	$V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V},$		2700	3500	pF
C _{oss}	Output Capacitance	f = 1.0 MHz		275	360	pF
C _{rss}	Reverse Transfer Capacitance			30	39	pF
Switching (Characteristics					
t _{d(on)}	Turn-On Delay Time	$V_{DD} = 400 \text{ V}, I_D = 12.6\text{A},$		60	130	ns
t _r	Turn-On Rise Time	$R_G = 25 \Omega$		150	310	ns
t _{d(off)}	Turn-Off Delay Time			155	320	ns
t _f	Turn-Off Fall Time	(Note 4)		110	230	ns
Qg	Total Gate Charge	V _{DS} = 640 V, I _D = 12.6A,		68	88	nC
Q _{gs}	Gate-Source Charge	V _{GS} = 10 V		15		nC
Q _{gd}	Gate-Drain Charge	(Note 4)		32		nC
Drain-Sour	ce Diode Characteristics and Maximum Rating	gs	-/-			
Maximum Continuous Drain-Source Diode Forward Current					12.6	Α
I _{SM}	Maximum Pulsed Drain-Source Diode Forward Current				50.4	Α
V _{SD}	Drain-Source Diode Forward Voltage V _{GS} = 0 V, I _S = 12.6A				1.4	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _S = 12.6 A,		850		ns
Q _{rr}	Reverse Recovery Charge	$dI_F / dt = 100 A/\mu s$		11.3	/	μС

Notes: 1. Repetitive Rating : Pulse width limited by maximum junction temperature 2. L = 13 mH, I_{AS} = 12.6 A, V_{DD} = 50 V, R_G = 25 Ω , Starting T_J = 25°C 3. I_{SD} \leq 12.6 A, di/dt \leq 200 A/µs, V_{DD} \leq BV_{DSS}, Starting T_J = 25°C 4. Essentially independent of operating temperature

Typical Characteristics

Figure 1. On-Region Characteristics

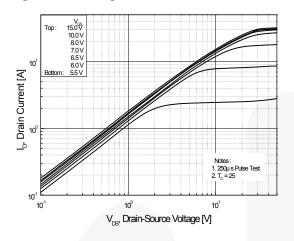


Figure 2. Transfer Characteristics

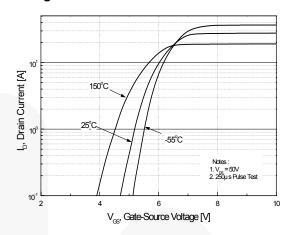


Figure 3. On-Resistance Variation vs.

Drain Current and Gate Voltage

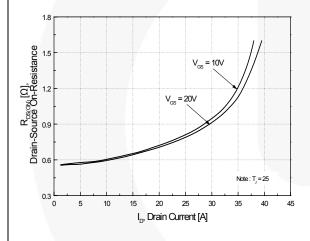


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperatue

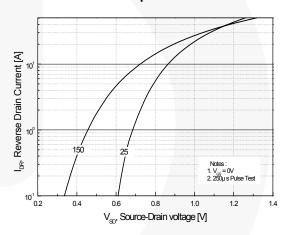


Figure 5. Capacitance Characteristics

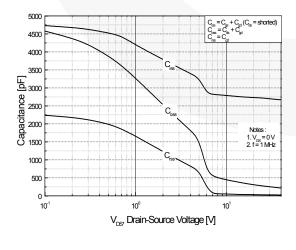
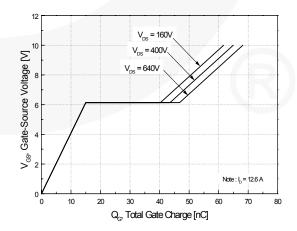


Figure 6. Gate Charge Characteristics



Typical Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

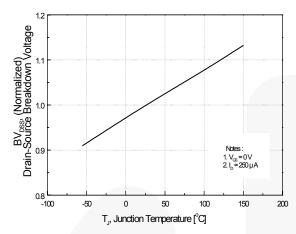


Figure 8. On-Resistance Variation vs. Temperature

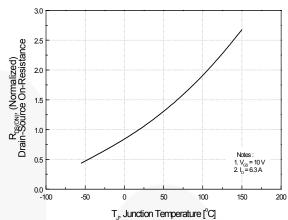


Figure 9. Maximum Safe Operating Area

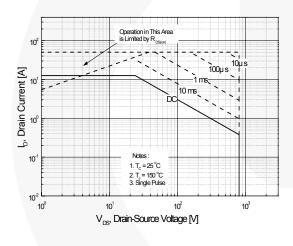


Figure 10. Maximum Drain Current vs. Case Temperature

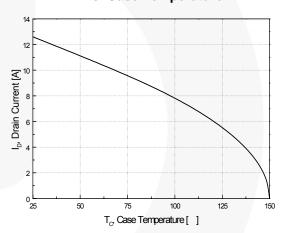
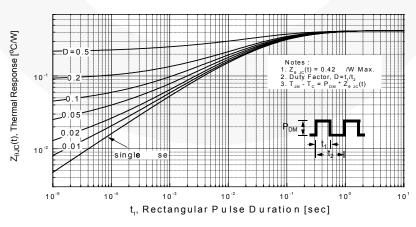


Figure 11. Transient Thermal Response Curve



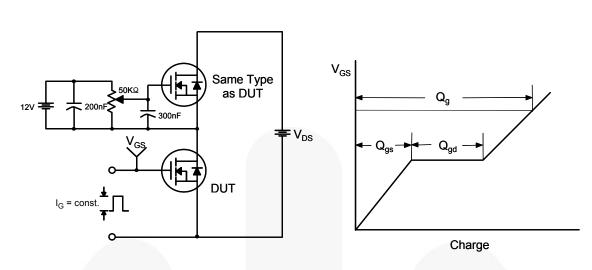


Figure 12. Gate Charge Test Circuit & Waveform

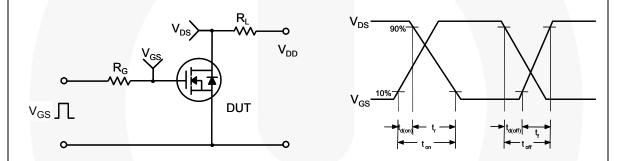


Figure 13. Resistive Switching Test Circuit & Waveforms

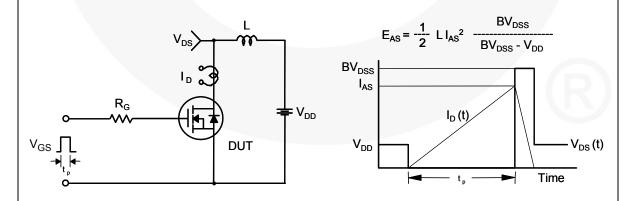
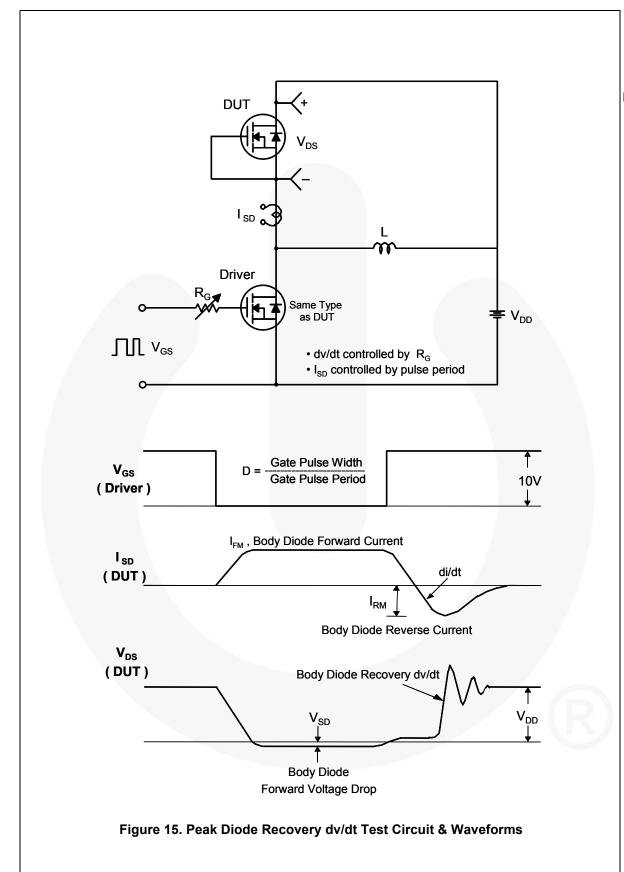
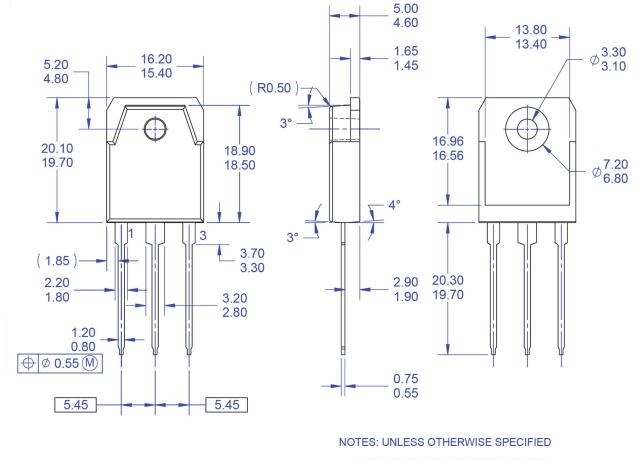


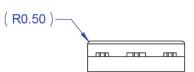
Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms



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Mechanical Dimensions





- A) THIS PACKAGE CONFORMS TO EIAJ SC-65 PACKAGING STANDARD.
- ALL DIMENSIONS ARE IN MILLIMETERS.
- **DIMENSION AND TOLERANCING PER** ASME14.5-2009.
- D) DIMENSIONS ARE EXCLUSSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSSIONS.
 E) DRAWING FILE NAME: TO3PN03AREV1.
- FAIRCHILD SEMICONDUCTOR.

Figure 16. TO3PN, 3-Lead, Plastic, EIAJ SC-65

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