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# 74AC374, 74ACT374

## Octal D-Type Flip-Flop with 3-STATE Outputs

### Features

- $I_{CC}$  and  $I_{OZ}$  reduced by 50%
- Buffered positive edge-triggered clock
- 3-STATE outputs for bus-oriented applications
- Outputs source/sink 24mA
- See 273 for reset version
- See 377 for clock enable version
- See 373 for transparent latch version
- See 574 for broadside pinout version
- See 564 for broadside pinout version with inverted outputs
- ACT374 has TTL-compatible inputs

### General Description

The AC/ACT374 is a high-speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and 3-STATE outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable ( $\overline{OE}$ ) are common to all flip-flops.

### Ordering Information

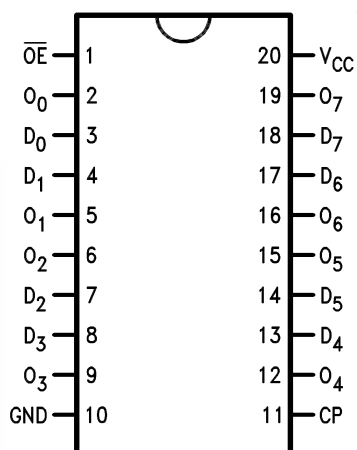
Order Number	Package Number	Package Description
74AC374SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74AC374SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74AC374MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74AC374PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
74ACT374SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74ACT374SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74ACT374MSA	MSA20	20-Lead Shrink Small Outline Package (SSOP), JEDEC MO-150, 5.3mm Wide
74ACT374MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74ACT374PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.



All packages are lead free per JEDEC: J-STD-020B standard.

## Connection Diagram



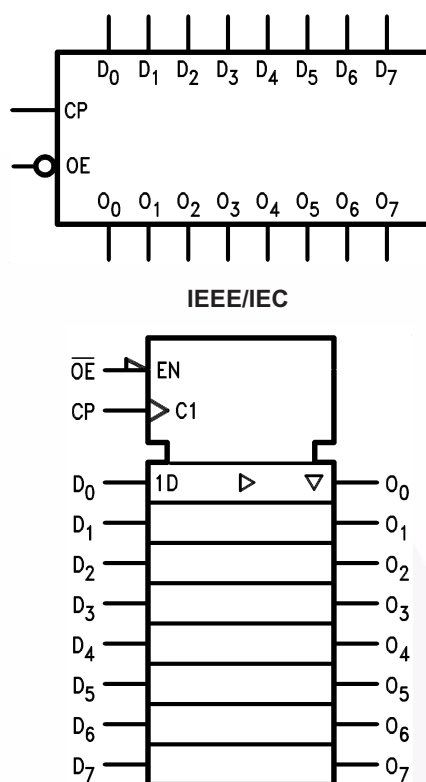
## Pin Description

Pin Names	Description
D <sub>0</sub> –D <sub>7</sub>	Data Inputs
CP	Clock Pulse Input
$\overline{OE}$	3-STATE Output Enable Input
O <sub>0</sub> –O <sub>7</sub>	3-STATE Outputs

## Functional Description

The AC/ACT374 consists of eight edge-triggered flip-flops with individual D-type inputs and 3-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ( $\overline{OE}$ ) LOW, the contents of the eight flip-flops are available at the outputs. When the  $\overline{OE}$  is HIGH, the outputs go to the high impedance state. Operation of the  $\overline{OE}$  input does not affect the state of the flip-flops.

## Logic Symbols



## Truth Table

Inputs			Outputs
D <sub>n</sub>	CP	$\overline{OE}$	O <sub>n</sub>
H	↗	L	H
L	↗	L	L
X	X	H	Z

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Z = High Impedance

↗ = LOW-to-HIGH Transition

The diagram illustrates an 8-bit shift register implemented with eight D flip-flops. The clock input (CP) is connected to the clock input of every flip-flop. The data input (D) of each flip-flop is connected to the output (Q) of the preceding flip-flop in the chain. The output of the final flip-flop is connected to the output of the first flip-flop, forming a closed loop. The output of each flip-flop is also connected to a buffer (represented by a triangle symbol) and labeled  $O_0$  through  $O_7$ . The output of the first flip-flop is also connected to the output of the last flip-flop, forming a closed loop. The output of each flip-flop is also connected to a buffer (represented by a triangle symbol) and labeled  $O_0$  through  $O_7$ . The output of the first flip-flop is also connected to the output of the last flip-flop, forming a closed loop.

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
$V_{CC}$	Supply Voltage	−0.5V to +7.0V
$I_{IK}$	DC Input Diode Current $V_I = -0.5V$	−20mA
	$V_I = V_{CC} + 0.5$	+20mA
$V_I$	DC Input Voltage	−0.5V to $V_{CC} + 0.5V$
$I_{OK}$	DC Output Diode Current $V_O = -0.5V$	−20mA
	$V_O = V_{CC} + 0.5V$	+20mA
$V_O$	DC Output Voltage	−0.5V to $V_{CC} + 0.5V$
$I_O$	DC Output Source or Sink Current	±50mA
$I_{CC}$ or $I_{GND}$	DC $V_{CC}$ or Ground Current per Output Pin	±50mA
$T_{STG}$	Storage Temperature	−65°C to +150°C
$T_J$	Junction Temperature	140°C

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
$V_{CC}$	Supply Voltage AC	2.0V to 6.0V
	ACT	4.5V to 5.5V
$V_I$	Input Voltage	0V to $V_{CC}$
$V_O$	Output Voltage	0V to $V_{CC}$
$T_A$	Operating Temperature	−40°C to +85°C
$\Delta V / \Delta t$	Minimum Input Edge Rate, AC Devices: $V_{IN}$ from 30% to 70% of $V_{CC}$ , $V_{CC}$ @ 3.3V, 4.5V, 5.5V	125mV/ns
$\Delta V / \Delta t$	Minimum Input Edge Rate, ACT Devices: $V_{IN}$ from 0.8V to 2.0V, $V_{CC}$ @ 4.5V, 5.5V	125mV/ns

## DC Electrical Characteristics for AC

Symbol	Parameter	V <sub>CC</sub> (V)	Conditions	T <sub>A</sub> = +25°C		T <sub>A</sub> = −40°C to +85°C		Units
				Typ.	Guaranteed Limits			
V <sub>IH</sub>	Minimum HIGH Level Input Voltage	3.0	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> − 0.1V	1.5	2.1	2.1		V
		4.5		2.25	3.15	3.15		
		5.5		2.75	3.85	3.85		
V <sub>IL</sub>	Maximum LOW Level Input Voltage	3.0	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> − 0.1V	1.5	0.9	0.9		V
		4.5		2.25	1.35	1.35		
		5.5		2.75	1.65	1.65		
V <sub>OH</sub>	Minimum HIGH Level Output Voltage	3.0	I <sub>OUT</sub> = −50μA	2.99	2.9	2.9		V
		4.5		4.49	4.4	4.4		
		5.5		5.49	5.4	5.4		
		3.0	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> , I <sub>OH</sub> = −12mA		2.56	2.46		
		4.5	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> , I <sub>OH</sub> = −24mA		3.86	3.76		
		5.5	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> , I <sub>OH</sub> = −24mA <sup>(1)</sup>		4.86	4.76		
V <sub>OL</sub>	Maximum LOW Level Output Voltage	3.0	I <sub>OUT</sub> = 50μA	0.002	0.1	0.1		V
		4.5		0.001	0.1	0.1		
		5.5		0.001	0.1	0.1		
		3.0	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> , I <sub>OL</sub> = 12mA		0.36	0.44		
		4.5	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> , I <sub>OL</sub> = 24mA		0.36	0.44		
		5.5	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> , I <sub>OL</sub> = 24mA <sup>(1)</sup>		0.36	0.44		
I <sub>IN</sub> <sup>(2)</sup>	Maximum Input Leakage Current	5.5	V <sub>I</sub> = V <sub>CC</sub> , GND		±0.1	±1.0		μA
I <sub>OZ</sub>	Maximum 3-STATE Leakage Current	5.5	V <sub>I</sub> (OE) = V <sub>IL</sub> , V <sub>IH</sub> ; V <sub>I</sub> = V <sub>CC</sub> , GND; V <sub>O</sub> = V <sub>CC</sub> , GND		±0.25	±2.5		μA
I <sub>OLD</sub>	Minimum Dynamic Output Current <sup>(3)</sup>	5.5	V <sub>OLD</sub> = 1.65V Max.			75		mA
I <sub>OHD</sub>		5.5	V <sub>OHD</sub> = 3.85V Min.			−75		mA
I <sub>CC</sub> <sup>(2)</sup>	Maximum Quiescent Supply Current	5.5	V <sub>IN</sub> = V <sub>CC</sub> or GND		4.0	40.0		μA

## Notes:

1. All outputs loaded; thresholds on input associated with output under test.
2.  $I_{IN}$  and  $I_{CC}$  @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V  $V_{CC}$ .
3. Maximum test duration 2.0ms, one output loaded at a time.

## DC Electrical Characteristics for ACT

Symbol	Parameter	V <sub>CC</sub> (V)	Conditions	T <sub>A</sub> = +25°C		T <sub>A</sub> = −40°C to +85°C		Units
				Typ.	Guaranteed Limits			
V <sub>IH</sub>	Minimum HIGH Level Input Voltage	4.5	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> − 0.1V	1.5	2.0	2.0		V
		5.5		1.5	2.0	2.0		
V <sub>IL</sub>	Maximum LOW Level Input Voltage	4.5	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> − 0.1V	1.5	0.8	0.8		V
		5.5		1.5	0.8	0.8		
V <sub>OH</sub>	Minimum HIGH Level Output Voltage	4.5	I <sub>OUT</sub> = −50μA	4.49	4.4	4.4		V
		5.5		5.49	5.4	5.4		
		4.5	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> , I <sub>OH</sub> = −24mA		3.86	3.76		
		5.5	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> , I <sub>OH</sub> = −24mA <sup>(4)</sup>		4.86	4.76		
V <sub>OL</sub>	Maximum LOW Level Output Voltage	4.5	I <sub>OUT</sub> = 50μA	0.001	0.1	0.1		V
		5.5		0.001	0.1	0.1		
		4.5	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> , I <sub>OL</sub> = 24mA		0.36	0.44		
		5.5	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> , I <sub>OL</sub> = 24mA <sup>(4)</sup>		0.36	0.44		
I <sub>IN</sub>	Maximum Input Leakage Current	5.5	V <sub>I</sub> = V <sub>CC</sub> , GND		±0.1	±1.0		μA
I <sub>OZ</sub>	Maximum 3-STATE Leakage Current	5.5	V <sub>I</sub> = V <sub>IL</sub> , V <sub>IH</sub> ; V <sub>O</sub> = V <sub>CC</sub> , GND		±0.25	±2.5		μA
I <sub>CCT</sub>	Maximum I <sub>CC</sub> /Input	5.5	V <sub>I</sub> = V <sub>CC</sub> − 2.1V	0.6		1.5		mA
I <sub>OLD</sub>	Minimum Dynamic Output Current <sup>(5)</sup>	5.5	V <sub>OLD</sub> = 1.65V Max.			75		mA
I <sub>OHD</sub>		5.5	V <sub>OHD</sub> = 3.85V Min.			−75		mA
I <sub>CC</sub>	Maximum Quiescent Supply Current	5.5	V <sub>IN</sub> = V <sub>CC</sub> or GND		4.0	40.0		μA

**Notes:**

4. All outputs loaded; thresholds on input associated with output under test.  
 5. Maximum test duration 2.0ms, one output loaded at a time.

**AC Electrical Characteristics for AC**

Symbol	Parameter	V <sub>CC</sub> (V) <sup>(6)</sup>	T <sub>A</sub> = +25°C, C <sub>L</sub> = 50pF			T <sub>A</sub> = -40°C to +85°C, C <sub>L</sub> = 50pF		Units
			Min.	Typ.	Max.	Min.	Max.	
f <sub>MAX</sub>	Maximum Clock Frequency	3.3	60	110		60		MHz
		5.0	100	155		100		
t <sub>PLH</sub>	Propagation Delay, CP to O <sub>n</sub>	3.3	3.0	11.0	13.5	1.5	15.5	ns
		5.0	2.5	8.0	9.5	1.5	10.5	
t <sub>PHL</sub>	Propagation Delay, CP to O <sub>n</sub>	3.3	2.5	10.0	12.5	2.0	14.0	ns
		5.0	2.0	7.0	9.0	1.5	10.0	
t <sub>PZH</sub>	Output Enable Time	3.3	3.0	9.5	11.5	1.5	13.0	ns
		5.0	2.0	7.0	8.5	1.0	9.5	
t <sub>PZL</sub>	Output Enable Time	3.3	2.5	9.0	11.5	1.5	13.0	ns
		5.0	2.0	6.5	8.5	1.0	9.5	
t <sub>PHZ</sub>	Output Disable Time	3.3	3.0	10.5	12.5	2.0	14.5	ns
		5.0	2.0	8.0	11.0	2.0	12.5	
t <sub>PLZ</sub>	Output Disable Time	3.3	2.0	8.0	11.5	1.0	12.5	ns
		5.0	1.5	6.5	8.5	1.0	10.0	

**Note:**

6. Voltage range 3.3 is 3.3V ± 0.3V. Voltage range 5.0 is 5.0V ± 0.5V.

**AC Operating Requirements for AC**

Symbol	Parameter	V <sub>CC</sub> (V) <sup>(7)</sup>	T <sub>A</sub> = +25°C, C <sub>L</sub> = 50pF		T <sub>A</sub> = −40°C to +85°C, C <sub>L</sub> = 50pF	Units
			Typ.	Guaranteed Minimum		
t <sub>S</sub>	Setup Time, HIGH or LOW, D <sub>n</sub> to CP	3.3	2.0	5.5	6.0	ns
		5.0	1.0	4.0	4.5	
t <sub>H</sub>	Hold Time, HIGH or LOW, D <sub>n</sub> to CP	3.3	−1.0	1.0	1.0	ns
		5.0	0	1.5	1.5	
t <sub>W</sub>	CP Pulse Width, HIGH or LOW	3.3	4.0	5.5	6.0	ns
		5.0	2.5	4.0	4.5	

**Note:**

7. Voltage range 3.3 is 3.3V ± 0.3V. Voltage range 5.0 is 5.0V ± 0.5V.

**AC Electrical Characteristics for ACT**

Symbol	Parameter	$V_{CC} (V)^{(8)}$	$T_A = +25^{\circ}C$ , $C_L = 50pF$			$T_A = -40^{\circ}C$ to $+85^{\circ}C$ , $C_L = 50pF$		Units
			Min.	Typ.	Max.	Min.	Max.	
$f_{MAX}$	Maximum Clock Frequency	5.0	100	160		90		MHz
$t_{PLH}$	Propagation Delay, CP to $O_n$	5.0	2.0	8.5	10.0	2.0	11.5	ns
$t_{PHL}$	Propagation Delay, CP to $O_n$	5.0	2.0	8.0	9.5	1.5	11.0	ns
$t_{PZH}$	Output Enable Time	5.0	2.0	8.0	9.5	1.5	10.5	ns
$t_{PZL}$	Output Enable Time	5.0	1.5	8.0	9.0	1.5	10.5	ns
$t_{PHZ}$	Output Disable Time	5.0	1.5	8.5	11.5	1.0	12.5	ns
$t_{PLZ}$	Output Disable Time	5.0	1.5	7.0	8.5	1.0	10.0	ns

**Note:**

8. Voltage range 5.0 is  $5.0V \pm 0.5V$ .

**AC Operating Requirements for ACT**

Symbol	Parameter	$V_{CC} (V)^{(9)}$	$T_A = +25^{\circ}C$ , $C_L = 50pF$		$T_A = -40^{\circ}C$ to $+85^{\circ}C$ , $C_L = 50pF$	Units
			Typ.	Guaranteed Minimum		
$t_S$	Setup Time, HIGH or LOW, $D_n$ to CP	5.0	1.0	5.5	5.5	ns
$t_H$	Hold Time, HIGH or LOW, $D_n$ to CP	5.0	0	1.5	1.5	ns
$t_W$	CP Pulse Width, HIGH or LOW	5.0	2.5	5.0	5.0	ns

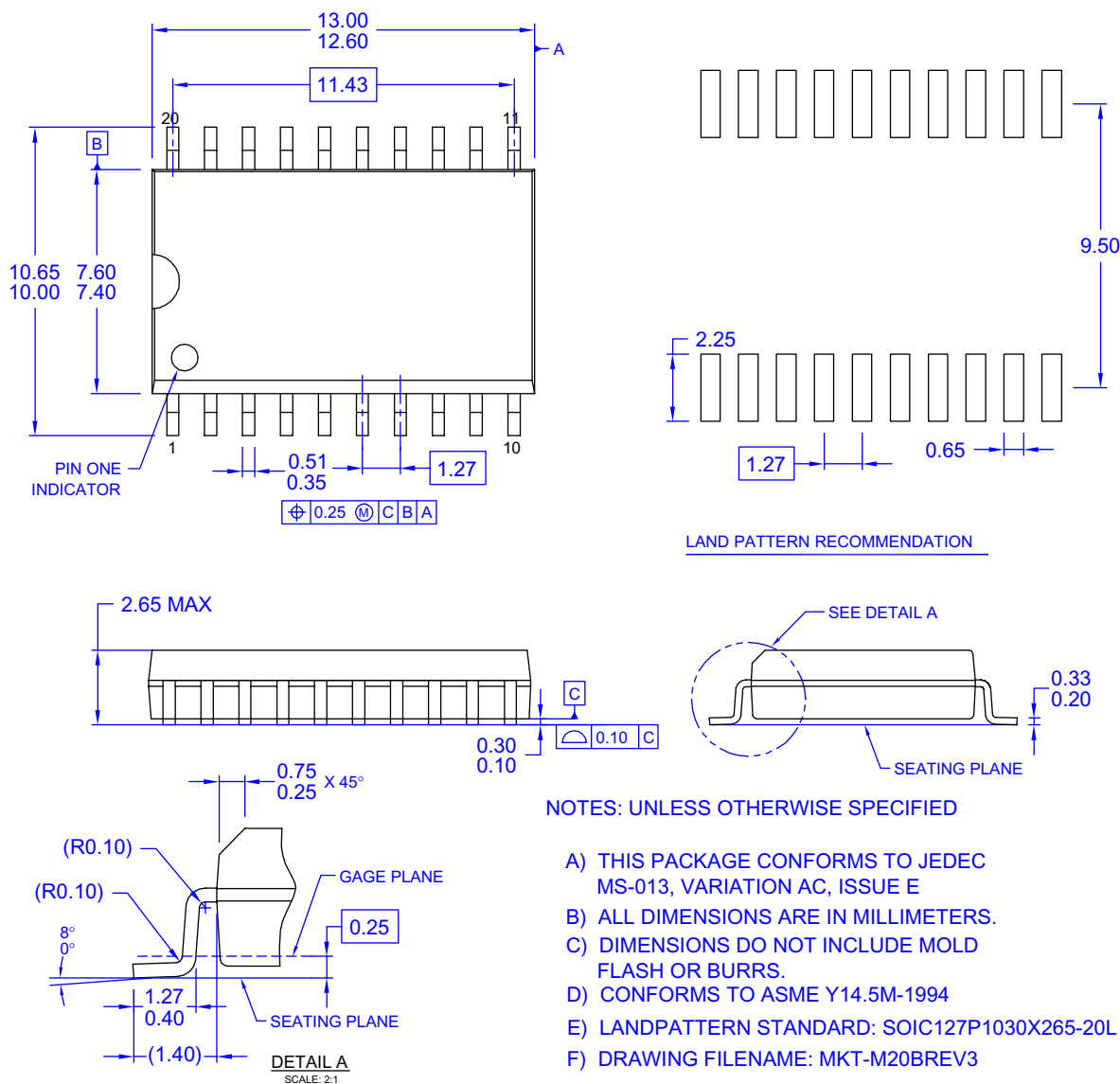
**Note:**

9. Voltage range 5.0 is  $5.0V \pm 0.5V$ .

**Capacitance**

Symbol	Parameter	Conditions	Typ.	Units
$C_{IN}$	Input Capacitance	$V_{CC} = OPEN$	4.5	pF

## Physical Dimensions



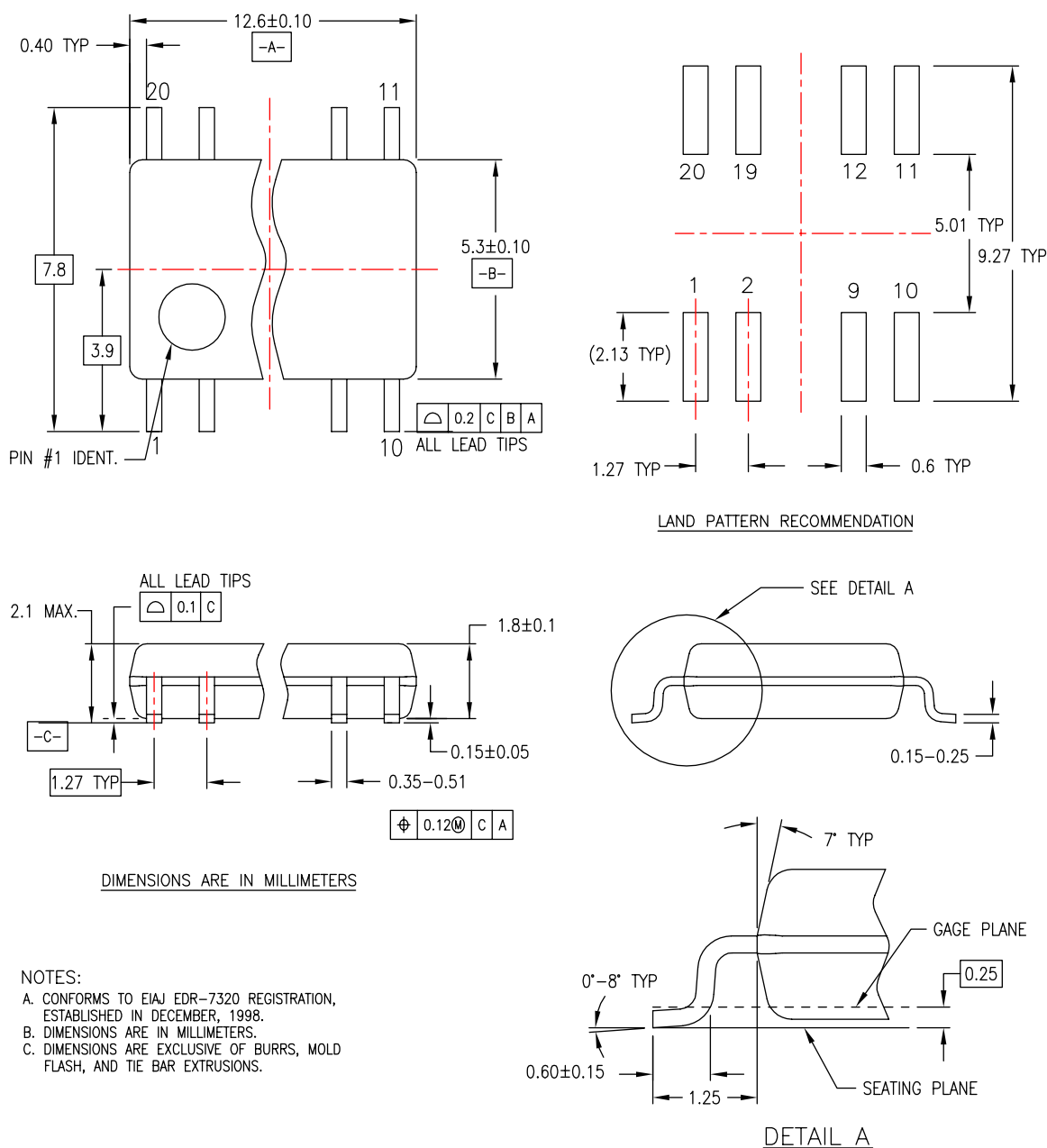
**Figure 1. 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide**

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## Physical Dimensions (Continued)



M20DREVC

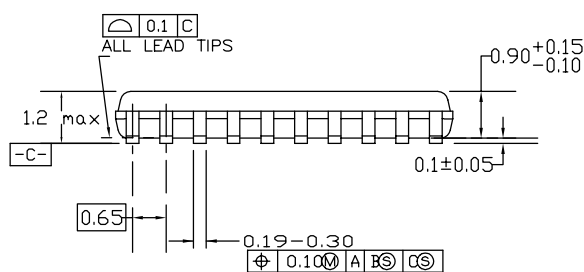
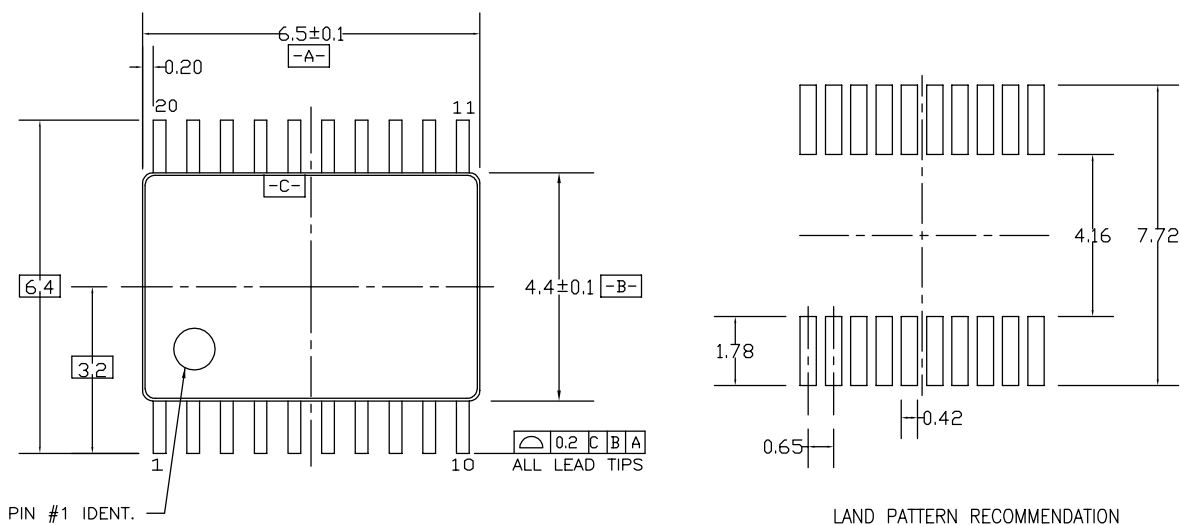
Figure 2. 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide

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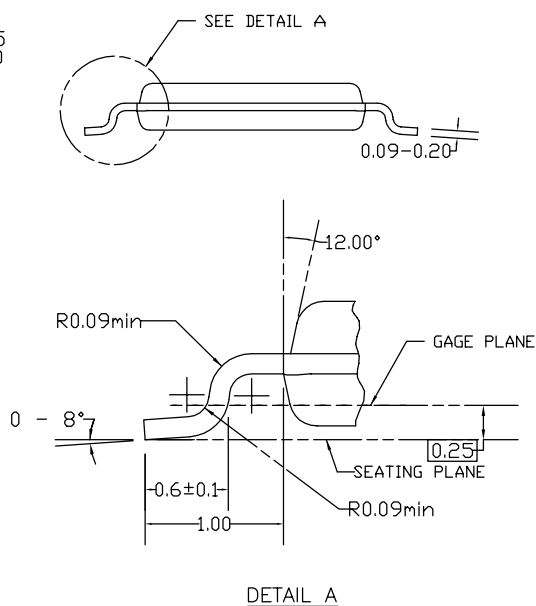
## Physical Dimensions (Continued)



DIMENSIONS ARE IN MILLIMETERS

## NOTES:

- CONFORMS TO JEDEC REGISTRATION MD-153, VARIATION AC, REF NOTE 6, DATE 7/93.
- DIMENSIONS ARE IN MILLIMETERS.
- DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS.
- DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.



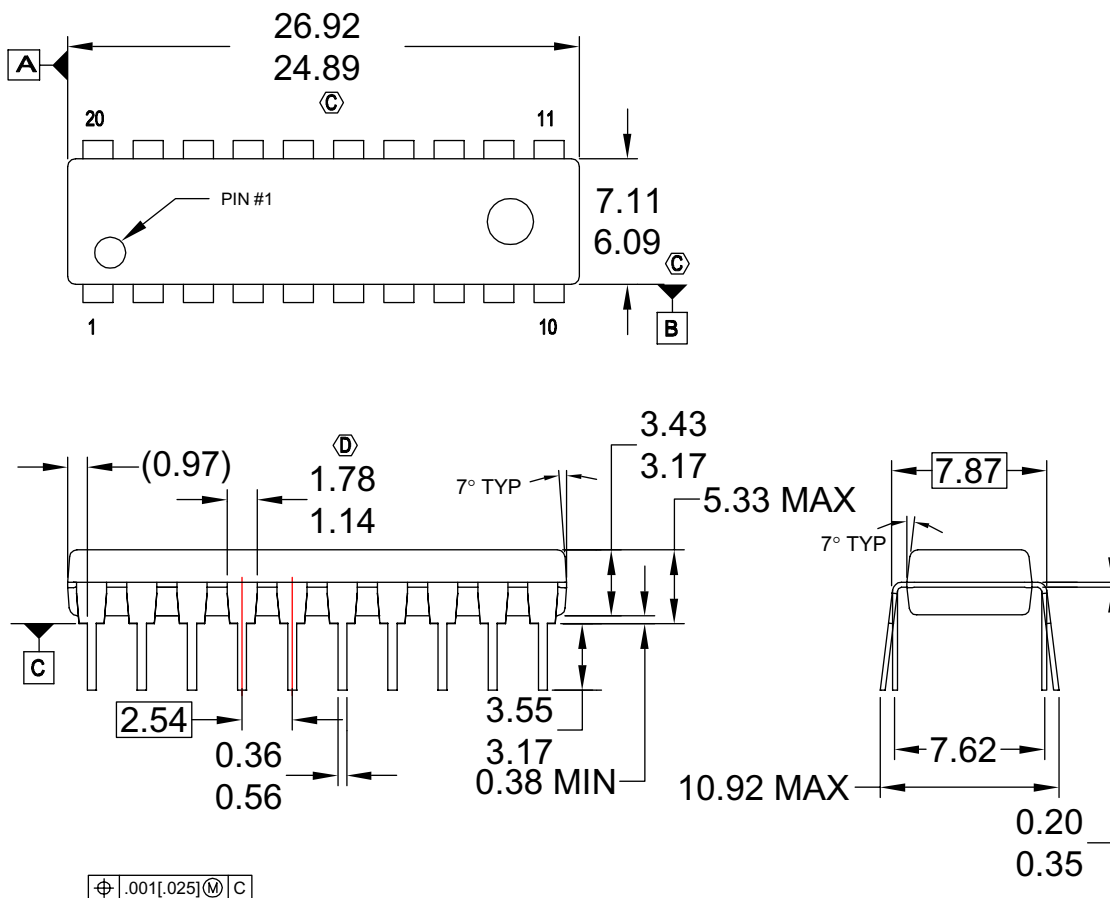
MTC20REV D1

Figure 3. 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

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**Physical Dimensions** (Continued)**NOTES:**

- A. CONFORMS TO JEDEC REGISTRATION MS-001, VARIATIONS AD.
- B. ALL DIMENSIONS ARE IN MILLIMETERS
- C. DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.25MM.
- D. DOES NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT EXCEED 0.25MM.
- E. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- F. DRAWING FILE NAME: N20AREV8

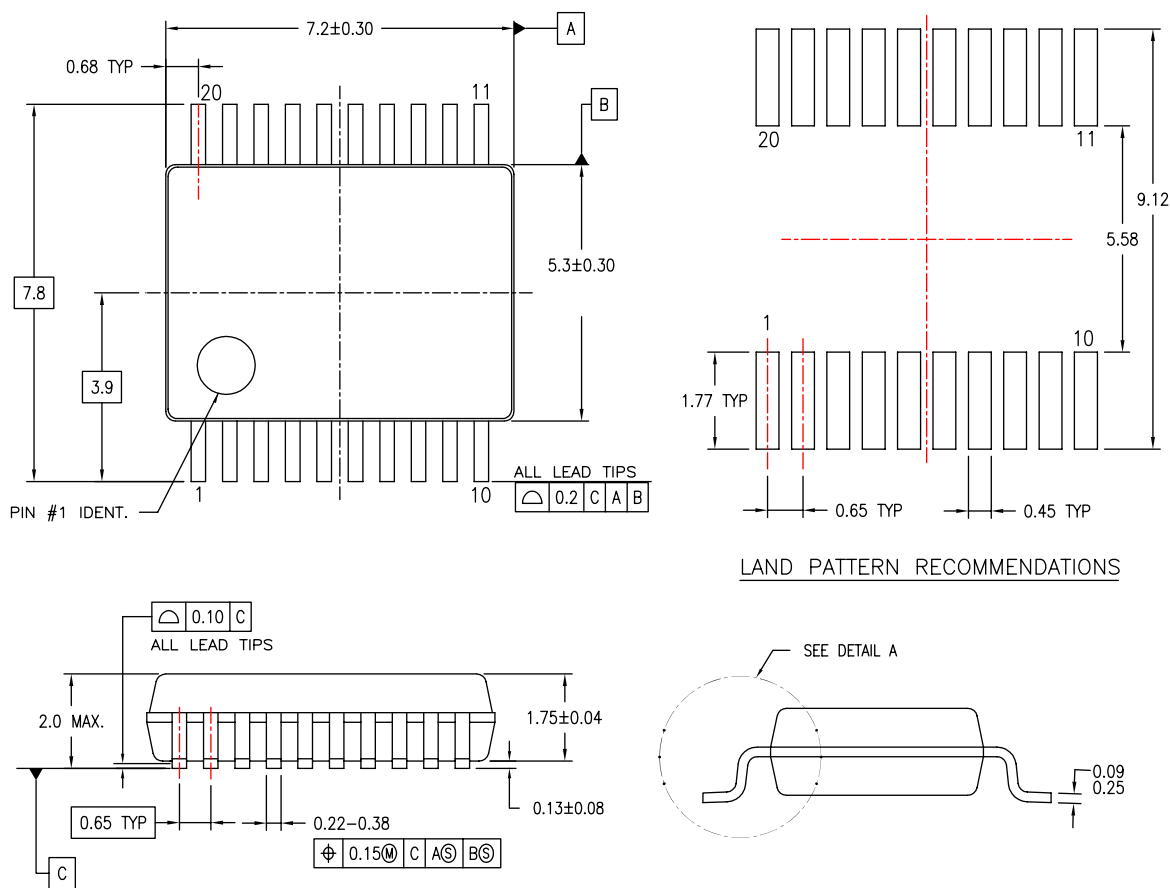
**Figure 4. 20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide**

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## Physical Dimensions (Continued)



DIMENSIONS ARE IN MILLIMETERS

## NOTES:

- CONFORMS TO JEDEC REGISTRATION MO-150, VARIATION AE, DATE 1/94.
- DIMENSIONS ARE IN MILLIMETERS.
- DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- DIMENSIONS AND TOLERANCES PER ASME Y14.5M - 1994.

MSA20REVB

Figure 5. 20-Lead Shrink Small Outline Package (SSOP), JEDEC MO-150, 5.3mm Wide

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

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