High Efficiency, Eight-String, White LED Driver for LCD Backlight Applications

Data Sheet

ADD5201

FEATURES

- **White LED driver based on inductive boost converter**
  - **Integrated 50 V MOSFET with 2.9 A peak current limit**
  - **Input voltage range: 6 V to 21 V**
  - **Maximum output adjustable up to 45 V**
  - **350 kHz to 1 MHz adjustable operating frequency**
  - **Built-in soft start for boost converter**
- **Drives up to eight LED current sources**
  - **LED current adjustable up to 30 mA for each channel**
  - **Headroom control to maximize efficiency**
  - **Adjustable output dimming frequency: 200 Hz to 10 kHz**
  - **LED open/short fault protection**
- **Selectable brightness control interface modes**
  - **PWM input**
  - **SMBus serial interface**
  - **Selectable dimming controls**
  - **Fixed delay PWM dimming control with 8-bit resolution**
  - **No delay PWM dimming control with 8-bit resolution**
  - **Phase shift PWM dimming control with 8-bit resolution**
  - **Direct PWM dimming control**
  - **DC current dimming mode with 8-bit resolution**
- **General**
  - **Thermal shutdown**
  - **Undervoltage lockout**
  - **28-lead, 4 mm × 4 mm LFCSP**

APPLICATIONS

Notebook PCs, UMPCs, and monitor displays

BLOCK DIAGRAM

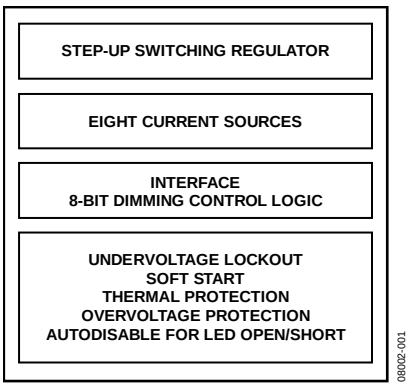

Figure 1.

GENERAL DESCRIPTION

The ADD5201 is a white LED driver for backlight applications based on high efficiency, current mode, step-up converter technology. It is designed with a 0.15 Ω, 2.9 A internal switch and a pin adjustable operating frequency between 350 kHz and 1 MHz. The ADD5201 contains eight regulated current sources for uniform brightness intensity. Each current source can be driven up to 30 mA.

The ADD5201 drives up to eight parallel strings of multiple series connected LEDs with a ±1.5% current regulation accuracy. The device provides an adjustable LED driving current up to 30 mA for each channel by an external resistor. The ADD5201 provides various brightness control methods. The LED dimming control can be achieved through SMBus and/or pulse-width modulation (PWM) input. Each dimming mode is selectable with two external dimming mode selection pins. The device provides a pin adjustable output dimming frequency range from 200 Hz to 10 kHz.

The ADD5201 operates over an input voltage range of 6 V to 21 V, but the device can function with a voltage as low as 5.4 V. The ADD5201 has multiple safety protection features to prevent damage during fault conditions. If any LED is open or short, the device automatically disables the faulty current regulator. The internal soft start prevents inrush current during startup. A thermal shutdown protection prevents thermal damage.

The ADD5201 is available in a low profile, thermally enhanced, 4 mm × 4 mm × 0.75 mm, 28-lead, RoHS compliant lead frame chip scale package (LFCSP) and is specified over the industrial temperature range of −25°C to +85°C.

Rev. A

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REVISION HISTORY

4/12—Revision A: Initial Version

FUNCTIONAL BLOCK DIAGRAM

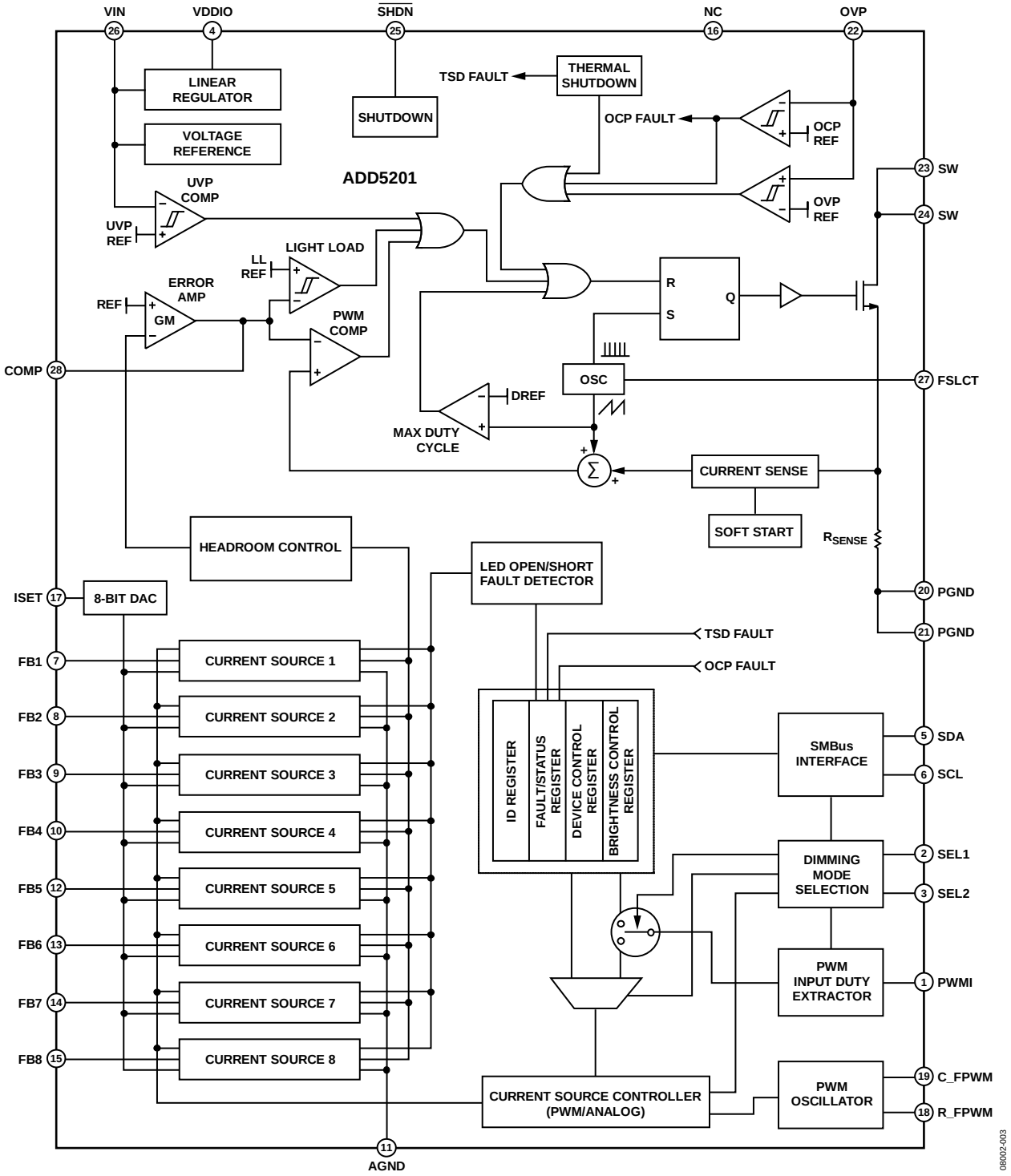

Figure 2. Functional Block Diagram

SPECIFICATIONS

V_{IN} = 12 V, $\overline{SHDN}$ = high, T_A = −25°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.

STEP-UP SWITCHING REGULATOR SPECIFICATIONS

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
SUPPLY						
Input Voltage Range	V_{IN}		6		21	V
BOOST OUTPUT						
Output Voltage	V_{OUT}				45	V
SWITCH						
On Resistance	$R_{DS(ON)}$	V_{IN} = 12 V, I_{SW} = 100 mA		150	210	mΩ
Leakage Current	I_{LKG}			44	70	µA
Peak Current Limit[1]	I_{CL}		2.9	3.4	4.0	A
OSCILLATOR						
Switching Frequency	f_{SW}	R_F = 150 kΩ	820	1000	1180	kHz
	f_{SW}	R_F = 470 kΩ		350		kHz
Maximum Duty Cycle	D_{MAX}	R_F = 470 kΩ	85	90		%
Soft Start Time	t_{SS}			1.5		ms
OVERVOLTAGE PROTECTION						
Overvoltage Threshold on OVP Pin						
Rising	V_{OVPR}		1.17	1.20	1.24	V
Falling	V_{OVPF}		1.08	1.12	1.16	V
Allowable OVP Level[2]	V_{OVP}				47.7	V

[1] Test without ramp compensation; the current limit is guaranteed by design and/or correlation to static test. The current limit is dependent on the duty cycle.
[2] A maximum 1% deviation of R2/R1 for the OVP setting is considered. The allowable OVP level must not exceed the SW absolute maximum rating of 50 V when considering the OVP setting for the deviation of the resistors and the ADD5201 V_{OVPR} deviation. See Figure 22 for more information.

$$V_{OVP} = \frac{1.2\ V}{R1} \times (R1 + R2)$$

LED CURRENT REGULATION SPECIFICATIONS

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
CURRENT SOURCE						
ISET Pin Voltage	V_{SET}	6 V ≤ V_{IN} ≤ 21 V	1.16	1.2	1.24	V
Adjustable LED Current[1]	I_{LED}		0		30	mA
Constant Current Sink of 20 mA[2]	I_{LED20}	R_{SET} = 141.56 kΩ	19.4	20	20.6	mA
Headroom Voltage of 20 mA	V_{HR20}	R_{SET} = 141.56 kΩ		0.65	0.85	V
Current Matching Between Strings[2]		R_{SET} = 141.56 kΩ	−1.5		+1.5	%
LED Current Accuracy[2]		R_{SET} = 141.56 kΩ	−3		+3	%
Current Source Leakage Current					1	µA
f_{PWM} GENERATOR						
Dimming Frequency Range	f_{PWM}	6 V ≤ V_{IN} ≤ 21 V	200		10,000	Hz
Dimming Frequency		R_{FPWM} = 50 kΩ, C_{FPWM} = 150 pF	820	1000	1180	Hz
LED FAULT DETECTION						
Open Fault Delay[1]	$t_{D\_OPENFAULT}$				6.5	µs

[1] Guaranteed by design.
[2] Test at T_A = +25°C.

SMBus SPECIFICATIONS

Table 3.

Parameter[1]	Symbol	Min	Typ	Max	Unit
SMBus INTERFACE					
Data, Clock Input Low Level	V_{IL}			0.5	V
Data, Clock Input High Level	V_{IH}	2.2		5.5	V
Data, Clock Output Low Level	V_{OL}			0.8	V
SMBus TIMING SPECIFICATIONS					
Clock Frequency	f_{SMB}	10		100	kHz
Bus-Free Time Between Stop and Start Conditions	t_{BUF}	4.7			µs
Hold Time After Start Condition[2]	$t_{HD;STA}$	4.0			µs
Setup Time					
Repeated Start Condition	$t_{SU;STA}$	4.7			µs
Stop Condition	$t_{SU;STO}$	4.0			µs
Data	$t_{SU;DAT}$	250			ns
Data Hold Time	$t_{HD;DAT}$	300			ns
Clock Period					
Low	t_{LOW}	4.7			µs
High	t_{HIGH}	4.0		50	µs
Clock/Data					
Fall Time	t_F			300	ns
Rise Time	t_R			1	µs

[1] These specifications are guaranteed by design.
[2] After this period, the first clock is generated.

GENERAL SPECIFICATIONS

Table 4.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
SUPPLY						
Input Voltage Range	V_{IN}		6		21	V
Quiescent Current	I_Q	6 V ≤ V_{IN} ≤ 21 V, $\overline{SHDN}$ = high		2.5	5.0	mA
Shutdown Supply Current	I_{SD}	6 V ≤ V_{IN} ≤ 21 V, $\overline{SHDN}$ = low		40	160	µA
VDDIO REGULATOR						
Regulated Output	V_{VDDIO_REG}	6 V ≤ V_{IN} ≤ 21 V	3.2	3.3	3.4	V
Short-Circuit Current	I_{VDDIO_SC}	6 V ≤ V_{IN} ≤ 21 V	2.3	5.0		mA
PWM INPUT						
Voltage						
High	V_{PWM_HIGH}		2.2		5.5	V
Low	V_{PWM_LOW}				0.8	V
Allowable Input Range			200		10,000	Hz
THERMAL SHUTDOWN						
Threshold[1]	T_{SD}			160		°C
Hysteresis[1]	T_{SDHYS}			30		°C
UVLO						
V_{IN} Threshold						
Falling	V_{UVLOF}	V_{IN} falling	4.4	4.6		V
Rising	V_{UVLOR}	V_{IN} rising		5.0	5.4	V
$\overline{SHDN}$ CONTROL						
Input Voltage						
Low	V_{IL}				1.0	V
High	V_{IH}		2.0			V
Input Current	$I_{\overline{SHDN}}$	$\overline{SHDN}$ = 3.3 V		6		µA

[1] This specification is guaranteed by design.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 5.

Parameter	Rating
VIN	−0.3 V to +23 V
SW	−0.3 V to +50 V
$\overline{SHDN}$	−0.3 V to +6 V
ISET, FSLCT, COMP, R_FPWM, C_FPWM	−0.3 V to +3.5 V
SDA, SCL, PWMI	−0.3 V to +6 V
FB1, FB2, FB3, FB4, FB5, FB6, FB7, FB8	−0.3 V to +50 V
OVP	−0.3 V to +3 V
VDDIO	−0.3 V to +3.7 V
SEL1, SEL2	−0.3 V to +6 V
Maximum Junction Temperature (T_J max)	150°C
Operating Temperature Range (T_A)	−25°C to +85°C
Storage Temperature Range (T_S)	−65°C to +150°C
Reflow Peak Temperature (20 sec to 40 sec)	260°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 6. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
28-Lead LFCSP	32.6	1.4	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

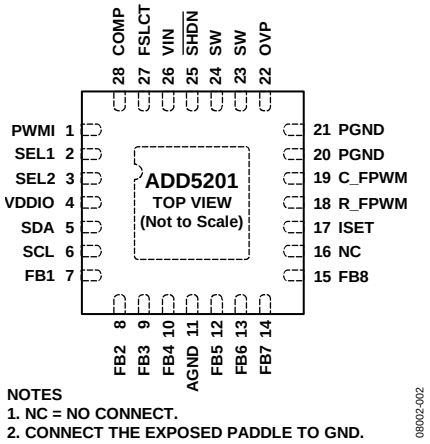

Figure 3. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	PWMI	PWM Signal Input. A 500 kΩ resistor is connected internally between this pin and AGND.
2	SEL1	Dimming Mode Selection 1.
3	SEL2	Dimming Mode Selection 2.
4	VDDIO	Internal Linear Regulator Output. This regulator provides power to the ADD5201.
5	SDA	Serial Data Input/Output.
6	SCL	Serial Clock.
7	FB1	Regulated Current Sink.
8	FB2	Regulated Current Sink.
9	FB3	Regulated Current Sink.
10	FB4	Regulated Current Sink.
11	AGND	Analog Ground.
12	FB5	Regulated Current Sink.
13	FB6	Regulated Current Sink.
14	FB7	Regulated Current Sink.
15	FB8	Regulated Current Sink.
16	NC	No Connect. This pin remains unconnected.
17	ISET	Full-Scale LED Current Setting. A resistor from this pin to ground sets the maximum LED current.
18	R_FPWM	Dimming Frequency Adjustment with an External Resistor.
19	C_FPWM	Dimming Frequency Adjustment with an External Capacitor.
20	PGND	Power Ground.
21	PGND	Power Ground.
22	OVP	Overvoltage Protection.
23	SW	Drain Connection of the Internal Power FET.
24	SW	Drain Connection of the Internal Power FET.
25	$\overline{\text{SHDN}}$	Shutdown Control for PWM Input Operation Mode. Active low. This pin can be left open for SMBus operation mode.
26	VIN	Supply Input.
27	FSLCT	Frequency Select. A resistor from this pin to ground sets the boost switching frequency from 350 kHz to 1 MHz.
28	COMP	Compensation for the Boost Converter. The capacitors and the resistor are connected in series between AGND and this pin for stable operation.
	EP	Exposed Paddle. Connect the exposed paddle to ground

TYPICAL PERFORMANCE CHARACTERISTICS

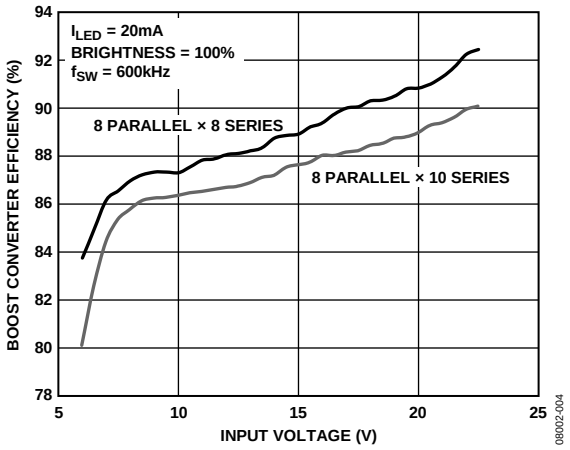

Figure 4. Boost Converter Efficiency vs. Input Voltage

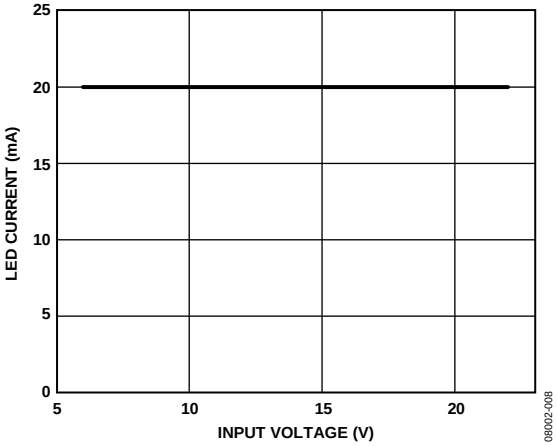

Figure 7. LED Current vs. Input Voltage (I_{LED} = 20 mA)

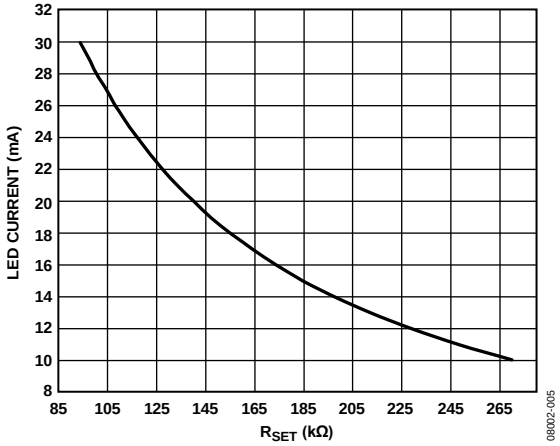

Figure 5. LED Current vs. R_{SET}

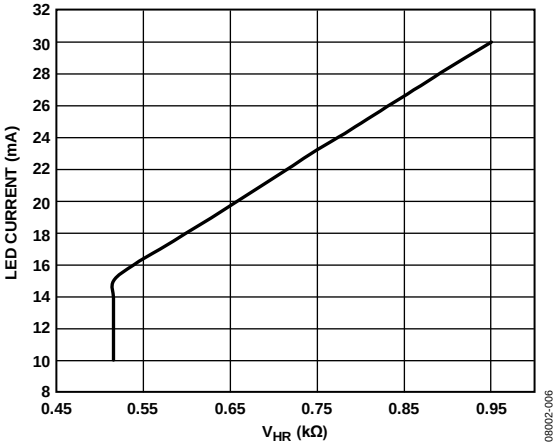

Figure 8. LED Current vs. Headroom Voltage

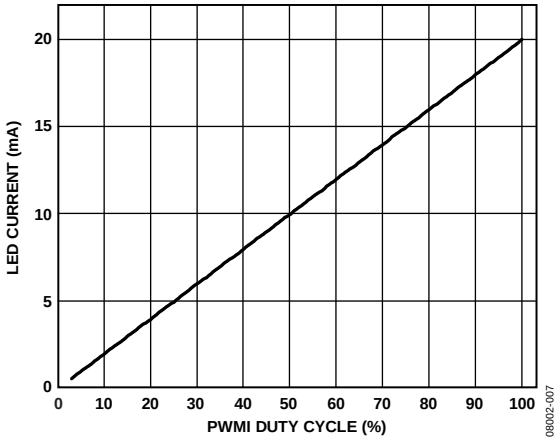

Figure 6. LED Current vs. PWM Input Duty Cycle

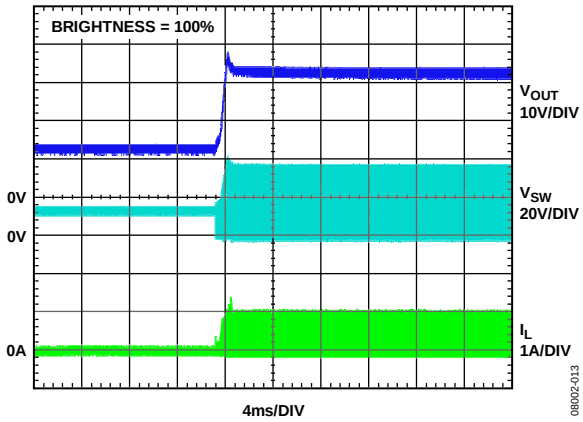

Figure 9. Start-Up Waveforms (Brightness = 100%)

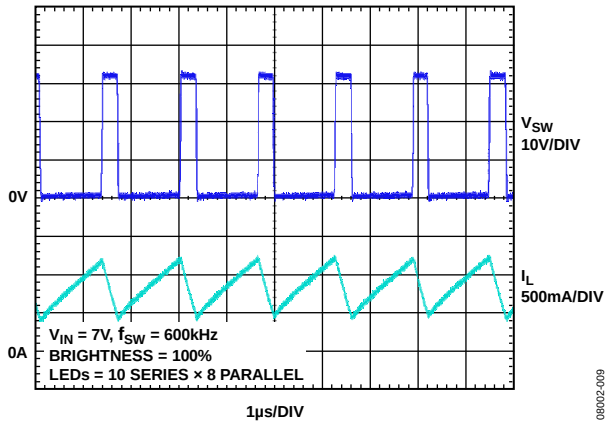

Figure 10. Switching Waveforms, V_{IN} = 7 V

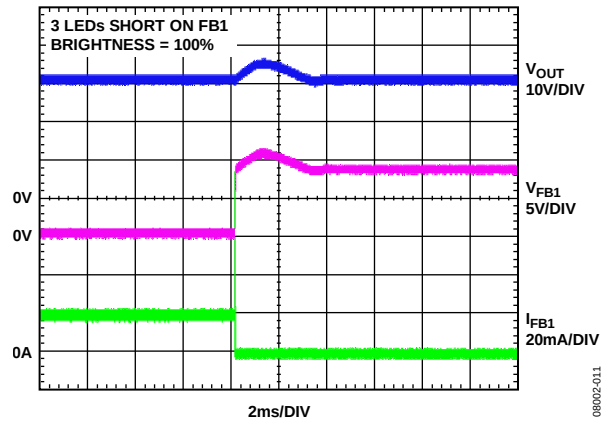

Figure 11. Short-Circuit Protection Waveforms

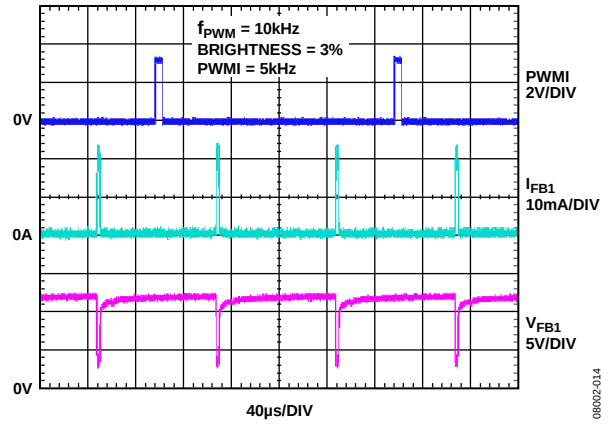

Figure 12. LED Current Waveforms

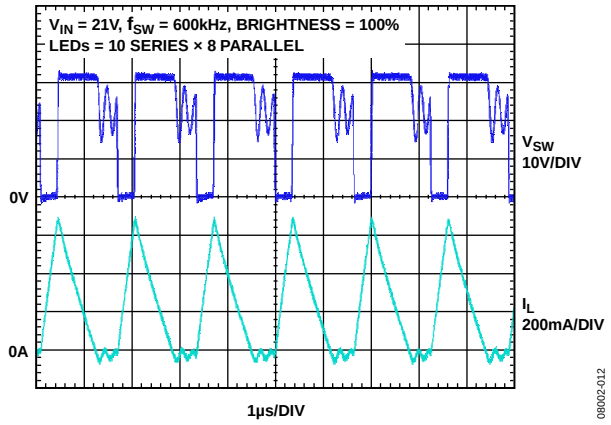

Figure 13. Switching Waveforms, V_{IN} = 21 V

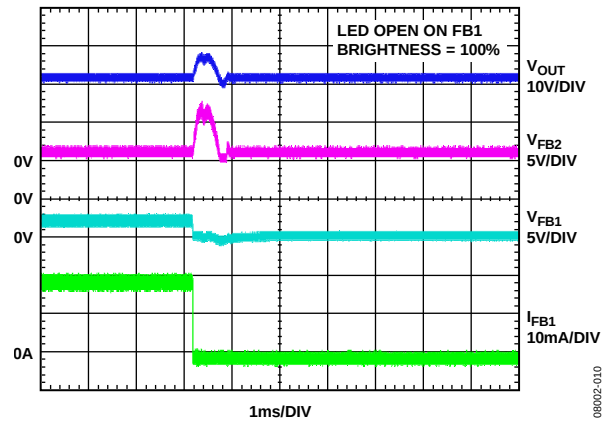

Figure 14. Open Load Protection Waveforms

THEORY OF OPERATION

CURRENT MODE, STEP-UP SWITCHING REGULATOR OPERATION

The ADD5201 uses a current mode PWM boost regulator to provide the minimal voltage needed to enable the LED string to drive at the programmed LED current. The current mode regulation system allows fast transient response while maintaining a stable output voltage. By selecting the proper resistor-capacitor network from COMP to AGND, the regulator response can be optimized for a wide range of input voltages, output voltages, and load conditions. The ADD5201 can provide a 45 V maximum output voltage and drive up to 13 LEDs (3.4 V/30 mA type of LEDs) for each channel.

INTERNAL 3.3 V REGULATOR

The ADD5201 contains a 3.3 V linear regulator. The regulator is used for biasing internal circuitry and the voltage levels of the SDA and SCL pins. The internal regulator requires a 1 µF bypass capacitor. Place this bypass capacitor between Pin VDDIO (Pin 4) and AGND, as close as possible to Pin VDDIO.

BOOST CONVERTER SWITCHING FREQUENCY

The ADD5201 boost converter switching frequency is adjustable, from 350 kHz to 1 MHz, by using an external resistor. A frequency of 350 kHz is recommended to optimize the regulator for high efficiency, and a frequency of 1 MHz is recommended for small external components. See Figure 15 for considerations when selecting a switching frequency and an adjustment resistor (R_F).

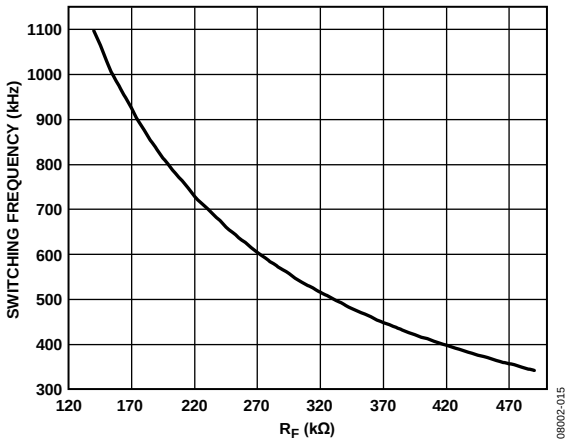

Figure 15. Switching Frequency vs. R_F

DIMMING FREQUENCY (f_{PWM}) ADJUSTMENT

The ADD5201 contains an internal oscillator to generate the PWM dimming signal for LED brightness control. The LED dimming frequency (f_{PWM}) is adjustable in the f_{PWM} range of 200 Hz to 10 kHz by using an external resistor (R_{FPWM}) and an external capacitor (C_{FPWM}). For all applications, maintain the R_{FPWM} range within 13 kΩ to 110 kΩ, and maintain the C_{FPWM} range within 20 pF to 390 pF. To reduce the output ripple, it is strongly recommended to choose an f_{PWM} greater than 5 kHz.

Table 8. R_{FPWM} and C_{FPWM} Recommendations

LED Dimming Frequency (f_{PWM})	R_{FPWM} (kΩ)	C_{FPWM} (pF)
200 Hz	110	390
500 Hz	75	200
1 kHz	50	150
5 kHz	18	47
10 kHz	13	20

CURRENT SOURCE

The ADD5201 contains eight current sources to provide accurate current sinking for each LED string. String-to-string tolerance is kept within ±1.5% at 20 mA. Each LED string current is adjusted by an external resistor in the LED current range of 0 mA to 30 mA.

The ADD5201 contains an LED open/short protection circuit for each channel. If the headroom voltage (V_{HR}) of each current source rises above 7.3 V during operation, the current source is disabled in the steady state condition. With the same conditions, if the headroom voltage of the current source remains below 200 mV while the boost converter output reaches the OVP level, the ADD5201 recognizes that the current source has an open load fault for the current source, and the current source is disabled.

For all PWM dimming operations, connect the LED strings in numerical order, starting with FB1. Tie any unused current to AGND.

For example, if an application requires four LED strings, connect each LED string using FB1 to FB4. Tie unused FB pins (FB5 to FB8) to AGND.

Programming the LED Current

As shown in the Figure 2, the ADD5201 has an LED current set pin (ISET). A resistor (R_{SET}) from this pin to ground adjusts the maximum LED current for f_{PWM} high in the LED current range of 0 mA to 30 mA (see Figure 16). The maximum LED current level can be set using the following equation:

$$I_{LED\ MAX} = \frac{2831}{R_{SET}}(\text{A})$$

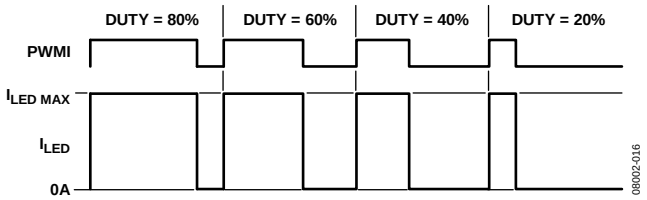

Figure 16. Maximum Current Setting for the LED Strings

BACKLIGHT BRIGHTNESS CONTROL

The ADD5201 mode of operation is selectable between the SMBus serial input and/or external PWM input. The LED brightness control method follows the method for selecting the mode of operation. For correct operation of the ADD5201, set the SEL1 and SEL2 mode selection pins based on the application conditions (see Table 9).

Table 9. Brightness Control Mode Selection

Mode Selection Settings			
SEL1	**SEL2**	**Dimming Mode**	**Interface**
High	High	Fixed delay PWM	SMBus
High	Open	Phase shift PWM	SMBus
High	Low	No delay PWM	SMBus
Open	High	Fixed delay PWM	PWMI
Open	Open	Phase shift PWM	PWMI
Open	Low	No delay PWM	PWMI
Low	High	DC current	SMBus
Low	Open	DC current	PWMI
Low	Low	Direct PWM	PWMI

PWM DIMMING MODE

The f_{PWM} duty is internally generated by 256 steps through the PWM input duty and/or the SMBus register setting value in the f_{PWM} duty range of 0% to 100%. Nevertheless, each current source has a minimum on time requirement for the LED current regulation such that the dimming is in the range of 3% to 100% when f_{PWM} is 5 kHz and when the boost converter switching frequency is in the range of 1 MHz to 600 kHz. In addition, the brightness controllable range is from 5% to 100% when the boost converter switching frequency is in the range of 350 kHz to 600 kHz.

Note that the ADD5201 has immunity when the PWM input duty cycle is converted to 256 steps even when the PWM input has ±0.195% jitter.

Fixed Delay PWM

Fixed delay PWM mode is selected when SEL1 = open and SEL2 = high for a PWMI application, or when SEL1 = high and SEL2 = high for an SMBus application. In fixed delay PWM mode, each current source has a fixed time delay from when the current source turns on and off with respect to the preceding current source. The fixed delay time is set by f_{PWM}. Each channel delay time is set by the following equation:

$$t_D = \frac{2 \times t_{FPWM}}{256}$$

where $t_{FPWM} = 1/f_{PWM}$, and f_{PWM} is the LED dimming frequency.

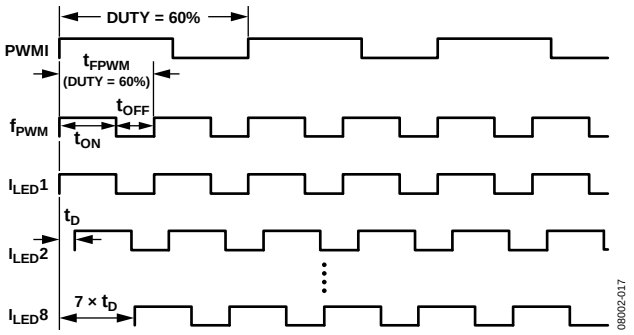

Figure 17. Fixed Delay PWM Dimming Timing

Phase Shift PWM

The phase shift PWM mode is selected when SEL1 = open and SEL2 = open for a PWMI application, or when SEL1 = high and SEL2 = open for an SMBus application. In the phase shift PWM mode, each current source phase delay is programmed by the number of current sources in operation and the f_{PWM} cycle. Each current source delay time is calculated by the following equation:

$$t_D = \frac{t_{FPWM}}{N}$$

where:
N is the number of operating current sources.
t_{FPWM} is the f_{PWM} cycle.

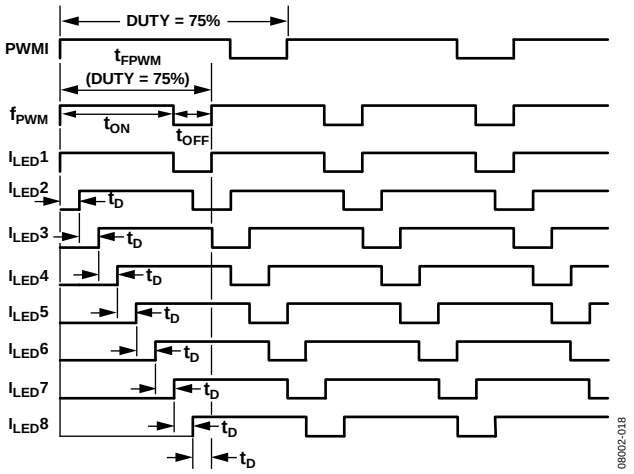

Figure 18. Phase Shift PWM Dimming Timing

No Delay PWM

The no delay PWM mode is selected when SEL1 = open and SEL2 = low for a PWMI application, or when SEL1 = high and SEL2 = low for an SMBus application. In the no delay PWM mode, all operating current sources turn on and off at the same time without any phase delay.

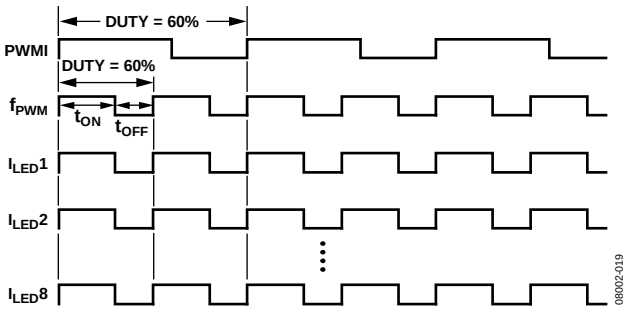

Figure 19. No Delay PWM Dimming Timing

Direct PWM

The direct PWM mode is selected when SEL1 = low and SEL2 = low. In the direct PWM mode, the PWM input controls the LED dimming logic of the ADD5201. It turns the current sources on and off without any modulation of the PWM input. In addition, each current source has no phase delay in this mode. The LED brightness is changed by the PWM input duty ratio.

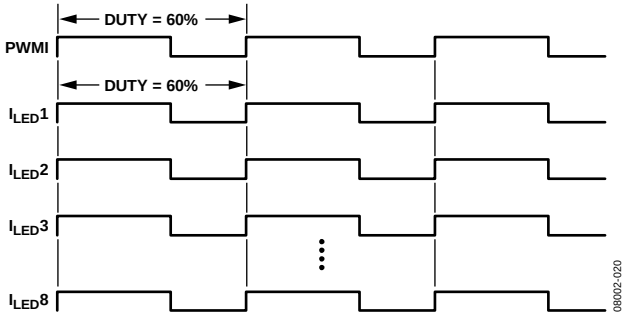

Figure 20. Direct PWM Dimming Timing

DC CURRENT DIMMING MODE

DC current mode is selected when SEL1 = low and SEL2 = open for a PWMI application, or when SEL1 = low and SEL2 = high for an SMBus application. In the dc current dimming mode, the maximum LED current is set by the value of R_{SET}. The PWM input or the SMBus can change the LED current in 256 steps between 0 mA and the maximum LED current.

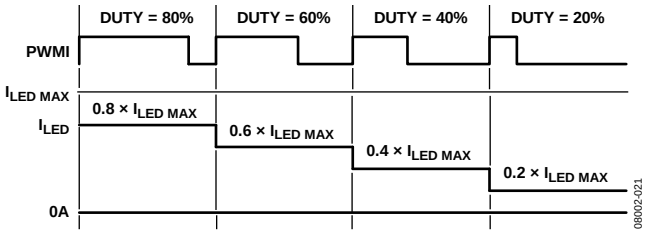

Figure 21. DC Current Dimming

SAFETY FEATURES

The ADD5201 contains many safety features to provide stable operation: soft start, overvoltage protection, open load protection, short-circuit protection, undervoltage lockout, and thermal protection.

Soft Start

The ADD5201 contains an internal soft start function to prevent inrush current at startup. The soft start time is typically 1.5 ms.

Overvoltage Protection (OVP)

The ADD5201 contains OVP circuits to prevent boost converter damage if the output voltage becomes excessive for any reason. To keep a safe output level, the integrated OVP circuit monitors the output voltage. When the OVP pin voltage is reached by the OVP rising threshold, the boost converter stops switching, causing the output voltage to drop. When the OVP pin voltage becomes lower than the OVP falling threshold, the boost converter resumes switching, causing the output to rise. There is about 7.5% hysteresis between the rising and falling thresholds.

The OVP level can be calculated using the following equation:

$$V_{OVP} = \frac{1.2\ V}{R1} \times (R1 + R2)$$

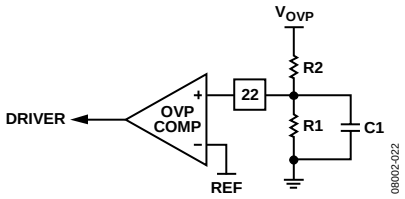

Figure 22. Overvoltage Protection Circuit

In general, the suitable OVP level is 5 V higher than the nominal boost switching regulator output. Large resistors, up to 1 MΩ, can be used for Resistor R2 to minimize power loss. In addition, some applications require C1 to prevent noise interference at the OVP pin in the range of 10 pF to 30 pF.

Open Load Protection (OLP)

The ADD5201 contains a dynamic headroom control circuit to minimize power loss at each current source. Therefore, the minimum feedback voltage is the reference for regulating the output voltage of the ADD5201 boost converter. If one or more LED strings is opened during normal operation, the current source headroom voltage (V_{HR}) is pulled to AGND. In this condition, OLP is active if V_{HR} is less than 200 mV until the boost converter output voltage rises to equal the OVP level.

Short-Circuit Protection (SCP)

The ADD5201 contains a short-circuit protection (SCP) circuit. If several LEDs are shorted in an LED string, a mismatched voltage is developed across the string. When the V_{HR} is higher than 7.3 V, the SCP circuit is activated and the current source is disabled. This protection starts to monitor each current source after the startup of the boost converter.

Undervoltage Lockout (UVLO)

A UVLO circuit is included with built-in hysteresis. The ADD5201 turns on when V_{IN} rises above 5.0 V and shuts down when V_{IN} falls below 4.6 V.

Thermal Protection

Thermal overload protection prevents excessive power dissipation from overheating the ADD5201. When the junction temperature (T_J) exceeds 160°C, a thermal sensor immediately activates the fault protection, which shuts down the device, allowing the IC to cool. The device self starts when the junction temperature (T_J) of the die falls below 130°C.

SMBus INTERFACE

When in SMBus mode, the ADD5201 can be controlled with an SMBus serial interface. Select the SMBus mode by using the SEL1 and SEL2 mode selection pins.

Read Byte

As shown in Figure 24, the read byte protocol is four bytes long and starts with the slave address followed by the command code, which translates to the register index. Next, the bus direction turns around with the rebroadcast of the slave address, with Bit 0 indicating a read cycle. The fourth byte contains the data being returned by the backlight controller. The byte value in the data byte should reflect the value of the register being queried at the command code index. Note the bus directions (shaded in Figure 24); these are used on cycles where the slaved backlight controller drives the data line. The host master drives all of the other cycles.

Write Byte

The write byte protocol is only three bytes long. The first byte starts with the slave address followed by the command code, which translates to the register index being written. The third byte contains the data byte that must be written into the register selected by the command code. Note the bus directions (shaded in Figure 25); these are used on cycles where the slaved backlight controller drives the data line. The host master drives all of the other cycles.

Slave Device Address

As shown in Figure 26, the ADD5201 address consists of seven address bits plus one read/write (R/$\overline{W}$) bit. If the device is in write mode, the LSB is set to 0 and the slave address byte is 0x58. If the device is in read mode, the LSB is set to 1 and the slave address byte is 0x59.

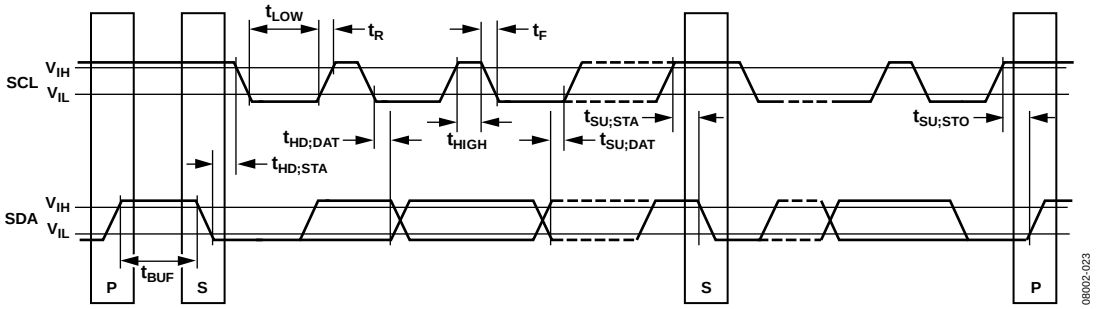

Figure 23. SMBus Interface

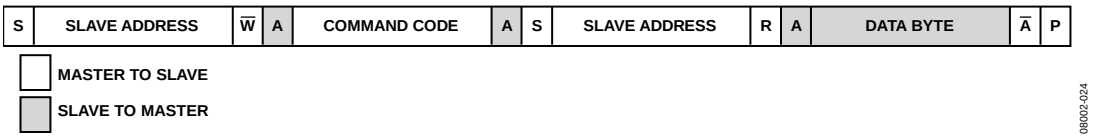

Figure 24. Read Byte Protocol

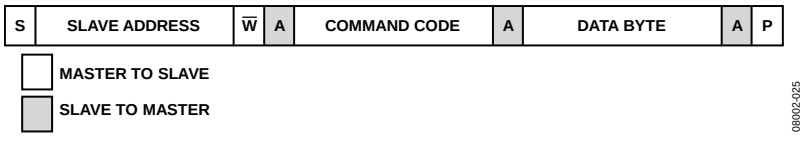

Figure 25. Write Byte Protocol

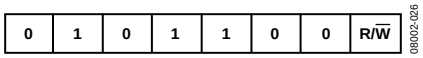

Figure 26. Slave Address Definition

SMBus REGISTER DESCRIPTION

The ADD5201 has four registers to control and monitor brightness, fault status, identifications, and operating modes. Those registers are 1-byte wide and accessible via the SMBus read/write byte protocols.

Brightness Control Register (Address 0x00)

The brightness control register consists of eight bits, BRT7 to BRT0, which are used to control the LED brightness level in 256 steps. An SMBus write byte cycle to this register sets the brightness level when the device is in SMBus mode. In addition, a write byte cycle to this register has no effect when the device is in a mode other than SMBus mode. Note that the operating mode is selected by the device control register (Address 0x01).

An SMBus read byte cycle to the brightness control register returns the current brightness level, regardless of the value of PWM_SEL. An SMBus setting of 0xFF for this register sets the device to the maximum brightness output, and a setting of 0x00 sets the device to the minimum brightness output.

This register is both readable and writable for all bits. The default value is 0xFF.

Device Control Register (Address 0x01)

This register has three bits. Two bits control the operation mode of the device, and a single bit controls the backlight on/off state. This register is both readable and writable for Bit 0 to Bit 2. Bit 0, named BL_CTL, is the on/off control for the output LEDs. Bit 1 and Bit 2, named PWM_SEL and PWM_MD, respectively, control the operating mode of the device. When the BL_CRT bit is set to 1, the device turns on the backlight within 10 ms after the write cycle. When the BL_CRT bit is set to 0, the device turns off the backlight immediately. The ADD5201 output operating mode is selected by the combination of Bit 1 and Bit 2 (see Table 10).

Table 10. Operating Modes Selected by Device Control Register, Bit 1 and Bit 2

PWM_MD	PWM_SEL	Mode
X[1]	1	PWM mode
1	0	SMBus mode
0	0	SMBus mode with DPST

[1] X = do not care.

The PWM_MD bit selects the manner in which the PWM input is to be interpreted. When this bit is 0, the PWM input reflects a percent change in the current brightness (that is, the Intel® Display Power Saving Technology, or DPST, mode) and should be as follows:

$$\text{DPST Brightness} = C_{BT} \times (\text{PWM})$$

where:
C_{BT} is the current brightness setting from SMBus without influence from the PWM.
PWM is the percent duty cycle.

The PWM signal starts from 100% when operating in DPST mode.

When PWM_MD is 1, the PWM input has no effect on the brightness setting, unless the ADD5201 is in PWM mode. In addition, when operating in PWM mode, this bit is a do not care (see Table 10). The PWM_SEL bit determines whether the SMBus or PWM input drives the brightness.

The relationship between these two control bits serves to specify an operating mode for the ADD5201. The defined modes are listed in Table 10. Note that, depending on the settings of some bits, other bits have no effect and are do not cares, shown as X in Table 10.

All reserved bits return to 0 when read, and the bits are ignored when written. This default value of the register is 0x00.

Table 11. Brightness Control Register (Address 0x00) Bit Map

Bit 7 (R/W)	Bit 6 (R/W)	Bit 5 (R/W)	Bit 4 (R/W)	Bit 3 (R/W)	Bit 2 (R/W)	Bit 1 (R/W)	Bit 0 (R/W)
BRT7	BRT6	BRT5	BRT4	BRT3	BRT2	BRT1	BRT0

Table 12. Brightness Control Register (Address 0x00) Bit Descriptions

Bit No.	Bit Name	Description
7:0	BRT	256 steps of brightness levels.

Table 13. Device Control Register (Address 0x01) Bit Map

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2 (R/W)	Bit 1 (R/W)	Bit 0 (R/W)
Reserved	Reserved	Reserved	Reserved	Reserved	PWM_MD	PWM_SEL	BL_CTL

Table 14. Device Control Register (Address 0x01) Bit Descriptions

Bit No.	Bit Name	Description
2	PWM_MD	PWM mode select. 1 = absolute brightness, 0 = percent change (default).
1	PWM_SEL	Brightness MUS select. 1 = PWM pin, 0 = SMBus value (default).
0	BL_CTL	Backlight on/off. 1= on, 0 = off (default).

Fault/Status Register (Address 0x02)

This register has six status bits that allow monitoring of the ADD5201 operating state. Bit 0, named fault, is a logical OR of all fault codes to simplify error detection. In the operation of the ADD5201, Bit 1, named THRM_SHDN, is set to 1 when a thermal shutdown event occurs. Bit 3, named BL_STAT, is the backlight status indicator. This bit is set to 1 whenever the backlight is on and is set to 0 whenever the backlight is off. Bit 4, named 1_CH_SD, is set to 1 when one or more current sources are disabled. In addition, Bit 5, named 2_CH_SD, is set to 1 when two or more current sources are disabled due to an LED open/short event during normal operation. All reserved bits return to 0 when read and ignore the bit value when written. All of the bits in this register are read only. The default value for Register 0x02 is 0x00.

Identification Register (Address 0x03)

The ID register contains two bit fields to denote the manufacturer and silicon revision of the ADD5201. The bit field widths were chosen to allow up to 16 vendors with up to eight silicon revisions each. To ensure that the number of silicon revisions remains low, the revision field should not be updated until the part is sent to the end customer's factory. Therefore, if during the engineering development process three silicon spins were needed before the device was released to the end customer's factory, the next available revision ID would be used for these three spins. The manufacturer ID of Analog Devices, Inc., is 6 (Bit[6:3] = 0110b). In addition, the initial value of REVx is 0, and subsequent REVx values increment by 1. This register is read only.

Table 15. Fault/Status Register (Address 0x02) Bit Map

Bit 7	Bit 6	Bit 5 (R)	Bit 4 (R)	Bit 3 (R)	Bit 2 (R)	Bit 1 (R)	Bit 0 (R)
Reserved	Reserved	2_CH_SD	1_CH_SD	BL_STAT	OV_CURR	THRM_SHDN	Fault

Table 16. Fault/Status Register (Address 0x02) Bit Descriptions

Bit No.	Bit Name	Description
5:4	2_CH_SD, 1_CH_SD	These bits report the number of faulted strings. 00 = no faults, 01 = one string fault, 11 = two or more strings faulted.
3	BL_STAT	Backlight status. 1 = backlight on, 0 = backlight off.
2	OV_CURR	Input overcurrent. 1= overcurrent condition, 0 = current okay.
1	THRM_SHDN	Thermal shutdown. 1 = thermal fault, 0 = thermal okay.
0	Fault	Fault occurred. Logic OR of all the fault conditions.

Table 17. Identification Register (Address 0x03) Bit Map

Bit 7	Bit 6 (R)	Bit 5 (R)	Bit 4 (R)	Bit 3 (R)	Bit 2 (R)	Bit 1 (R)	Bit 0 (R)
LED panel (Bit 7 = 1)	MFG3	MFG2	MFG1	MFG0	REV2	REV1	REV0

Table 18. Identification Register (Address 0x03) Bit Descriptions

Bit No.	Bit Name	Description
7	LED Panel	Display panel using LED backlight, Bit 7 = 1.
6:3	MFG[3:0]	Manufacturer ID. (Analog Devices ID is 6.)
2:0	REV[2:0]	Silicon revision. (Revision 0 to Revision 7 are allowed for silicon spins.)

EXTERNAL COMPONENT SELECTION GUIDE

Inductor Selection

The inductor is an integral part of the step-up converter. It stores energy during the switch-on time and transfers that energy to the output through the output diode during the switch-off time. An inductor in the range of 4.7 µH to 22 µH is recommended. In general, lower inductance values result in higher saturation current and lower series resistance for a given physical size. However, lower inductance results in higher peak current, which can lead to reduced efficiency and greater input and/or output ripple and noise. Peak-to-peak inductor ripple current at close to 30% of the maximum dc input current typically yields an optimal compromise.

For determining the inductor ripple current, the input (V_{IN}) and output (V_{OUT}) voltages determine the switch duty cycle (D) by the following equation:

$$D = \frac{V_{OUT} - V_{IN}}{V_{OUT}} \quad (1)$$

Using the duty cycle and switching frequency (f_{SW}) determines the on time in the following equation:

$$t_{ON} = \frac{D}{f_{SW}} \quad (2)$$

The inductor ripple current (ΔI_L) in steady state is

$$\Delta I_L = \frac{V_{IN} \times t_{ON}}{L}$$

Solving for the inductance value (L),

$$L = \frac{V_{IN} \times t_{ON}}{\Delta I_L}$$

Make sure that the peak inductor current (that is, the maximum input current plus half of the inductor ripple current) is less than the rated saturation current of the inductor. In addition, ensure that the maximum rated rms current of the inductor is greater than the maximum dc input current to the regulator.

For duty cycles greater than 50% that occur with input voltages greater than half the output voltage, slope compensation is required to maintain stability of the current mode regulator. For stable current mode operation, ensure that the selected inductance is equal to or greater than L_{MIN}:

$$L > L_{MIN} = \frac{V_{OUT} - V_{IN}}{2.9\ \text{A} \times f_{SW}}$$

Inductor manufacturers include Coilcraft, Inc.; Sumida Corporation; and Toko.

Input and Output Capacitors Selection

The ADD5201 requires input and output bypass capacitors to supply transient currents while maintaining a constant input and output voltage. Use a low effective series resistance (ESR) 10 µF or greater capacitor for the input capacitor to prevent noise at the ADD5201 input. Place the input and output capacitors between VIN and AGND, as close as possible to the ADD5201. Ceramic capacitors are preferred because of their low ESR characteristics. Alternatively, use a high value, medium ESR capacitor in parallel with a 0.1 µF low ESR capacitor as close as possible to the ADD5201.

The output capacitor maintains the output voltage and supplies current to the load while the ADD5201 switch is on. The value and characteristics of the output capacitor greatly affect the output voltage ripple and stability of the regulator. Use a low ESR output capacitor; ceramic dielectric capacitors are preferred.

For very low ESR capacitors, such as ceramic capacitors, the ripple current due to the capacitance is calculated as follows. Because the capacitor discharges during the on time (t_{ON}), the charge removed from the capacitor (Q_C) is the load current multiplied by the on time. Therefore, the output voltage ripple (ΔV_{OUT}) is

$$\Delta V_{OUT} = \frac{Q_C}{C_{OUT}} = \frac{I_L \times t_{ON}}{C_{OUT}}$$

where:
C_{OUT} is the output capacitance.
I_L is the average inductor current.

Using the duty cycle and switching frequency (f_{SW}), users can determine the on time by using Equation 2. The input (V_{IN}) and output (V_{OUT}) voltages determine the switch duty cycle (D) as shown in Equation 1.

Choose the output capacitor based on the following equation:

$$C_{OUT} \geq \frac{I_L \times (V_{OUT} - V_{IN})}{f_{SW} \times V_{OUT} \times \Delta V_{OUT}}$$

Capacitor manufacturers include Murata Manufacturing Co., Ltd.; AVX; Sanyo; and Taiyo Yuden Co., Ltd.

Diode Selection

The output diode conducts the inductor current to the output capacitor and load while the switch is off. For high efficiency, minimize the forward voltage drop of the diode. Schottky diodes are recommended. However, to maintain efficiency in high voltage, high temperature applications use an ultrafast junction diode to prevent significant reverse leakage current caused by the Schottky diode.

The output diode for a boost regulator must be chosen depending on the output voltage and the output current. The diode must be rated for a reverse voltage equal to or greater than the output voltage used. The average current rating must be greater than the maximum load current expected, and the peak current rating must be greater than the peak inductor current. Using Schottky diodes with lower forward voltage drop decreases power dissipation but increases efficiency. The diode must be rated to handle the average output load current. Many diode manufacturers derate the current capability of the diode as a function of the duty cycle. Verify that the output diode is rated

to handle the average output load current with the minimum duty cycle.

The minimum duty cycle of the ADD5201 is

$$D_{MIN} = \frac{V_{OUT} - V_{IN\_MAX}}{V_{OUT}}$$

where V_{IN_MAX} is the maximum input voltage.

For example, D_{MIN} is 0.5 when V_{OUT} is 40 V and V_{IN_MAX} is 20 V.

Schottky diode manufacturers include ON Semiconductor, Diodes Incorporated, Central Semiconductor Corp., and Sanyo.

Loop Compensation

Use of external components to compensate for the regulator loop allows optimization of the loop dynamics for a given application.

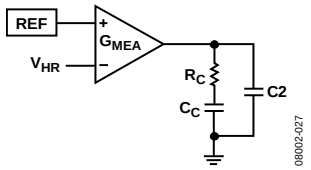

Figure 27. Compensation Components

Capacitor C2 is chosen to cancel the zero introduced by the output capacitance ESR.

Solving for C2

$$C2 = \frac{ESR \times C_{OUT}}{R_C}$$

For low ESR output capacitance, such as with a ceramic capacitor, C2 is optional. For optimal transient performance, R_C and C_C may need adjustment after observing the load transient response of the ADD5201. For most applications, maintain the compensation resistor within a range of 500 Ω to 30 kΩ, and maintain the compensation capacitor within a range of 100 pF to 330 nF.

LAYOUT GUIDELINES

When designing a high frequency, switching, regulated power supply, layout is very important. Using a good layout can solve many problems associated with these types of supplies. The main problems are loss of regulation at high output current and/or large input-to-output voltage differentials, excessive noise on the output and switch waveforms, and instability. Using the following guidelines can help minimize these problems.

Make all power (high current) traces as short, direct, and thick as possible. It is good practice on a standard printed circuit board (PCB) to make the traces an absolute minimum of 15 mil (0.381 mm) per ampere. Keep the inductor, output capacitors, and output diode as close to each other as possible to reduce the EMI radiated by the power traces that is caused by the high switching currents running through them. This also reduces lead inductance and resistance, which in turn reduce noise spikes, ringing, and resistive losses that produce voltage errors.

Connect the grounds of the IC, input capacitors, output capacitors, and output diode (if applicable) close together and directly to a ground plane. It is also best practice to have a ground plane on both sides of the PCB. This reduces noise by reducing ground-loop errors and by absorbing more of the EMI radiated by the inductor.

For multilayer boards of more than two layers, use a ground plane to separate the power plane (power traces and components) and the signal plane (feedback, compensation, and components) for improved performance. On multilayer boards, the use of vias is required to connect traces and different planes. If a trace needs to conduct a significant amount of current from one plane to the other, it is good practice to use one standard via per 200 mA of current. Arrange the components so that the switching current loops curl in the same direction.

Switching regulators have two operating power states: one state when the switch is on and one when the switch is off. During each state, there is a current loop made by the power components that are actively conducting. Place the power components so that the current loop is conducting in the same direction during each of the two states. This prevents magnetic field reversal caused by the traces between the two half cycles and reduces radiated EMI.

Layout Procedure

To achieve high efficiency, good regulation, and stability, a good PCB layout is required.

Use the following general guidelines when designing PCBs:

- Place C_{IN} close to the VIN and AGND leads of the ADD5201.
- Ensure that the high current path from C_{IN} (through L1) to the SW and PGND leads is as short as possible.
- Ensure that the high current path from C_{IN} (through L1), D1, and C_{OUT} is as short as possible.
- Make high current traces as short and wide as possible.
- Keep nodes that are connected to SW away from sensitive traces, such as COMP, to prevent coupling of the traces. If such traces need to be run near each other, place a ground trace between the two as a shield.
- Place the compensation components as close as possible to the COMP pin.
- Place the LED current setting resistors as close as possible to each pin to prevent noise pickup.
- Avoid routing noise sensitive traces near high current traces and components.
- Use a thermal pad size of the same dimensions as the exposed paddle on the bottom of the package.

Heat Sinking

When using a surface-mount power IC or external power switches, the PCB can often be used as the heat sink. This is achieved by simply using the copper area of the PCB to transfer heat from the device; maximizing this area optimizes thermal performance.

TYPICAL APPLICATION CIRCUITS

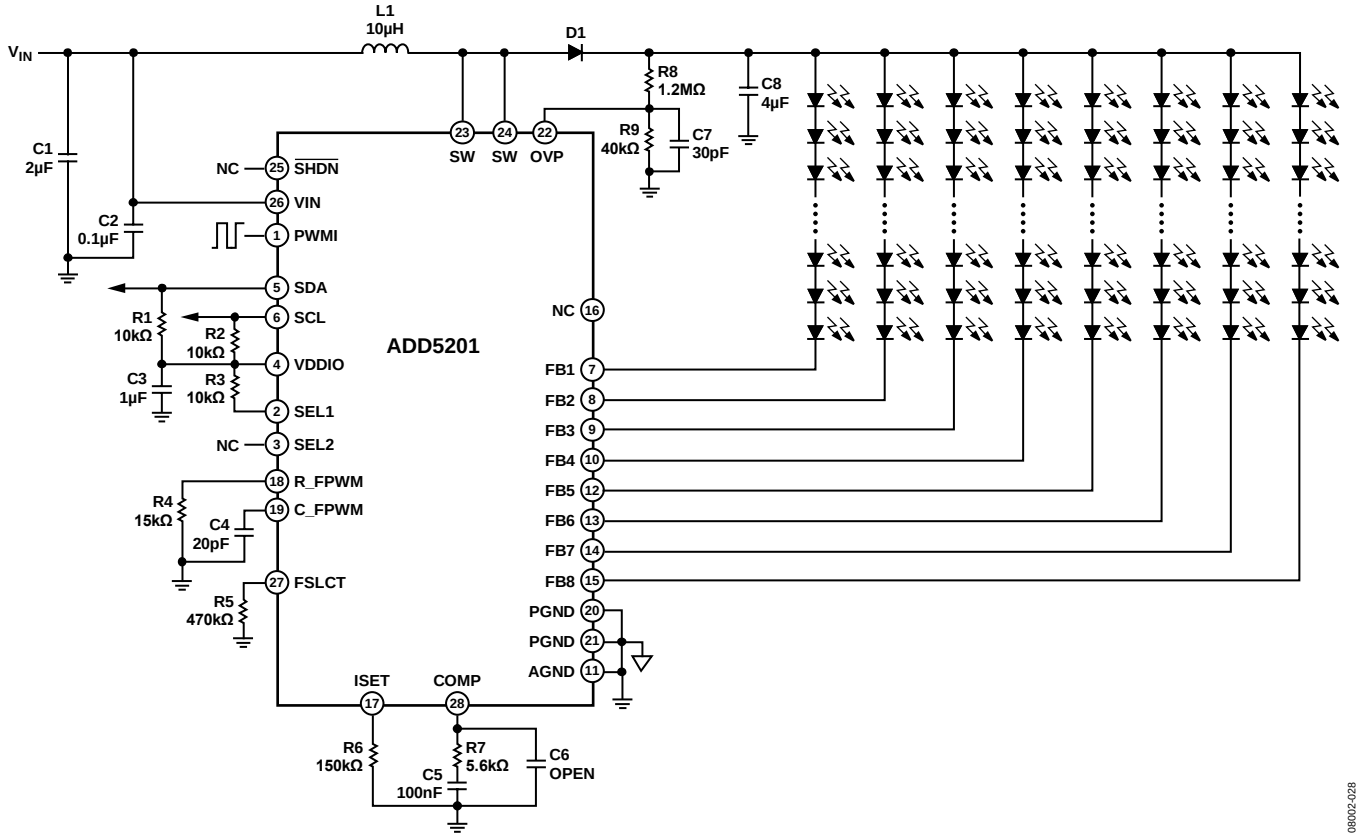

Figure 28. Typical Application Circuits for SMBus Interface with Phase Shift PWM Dimming Mode

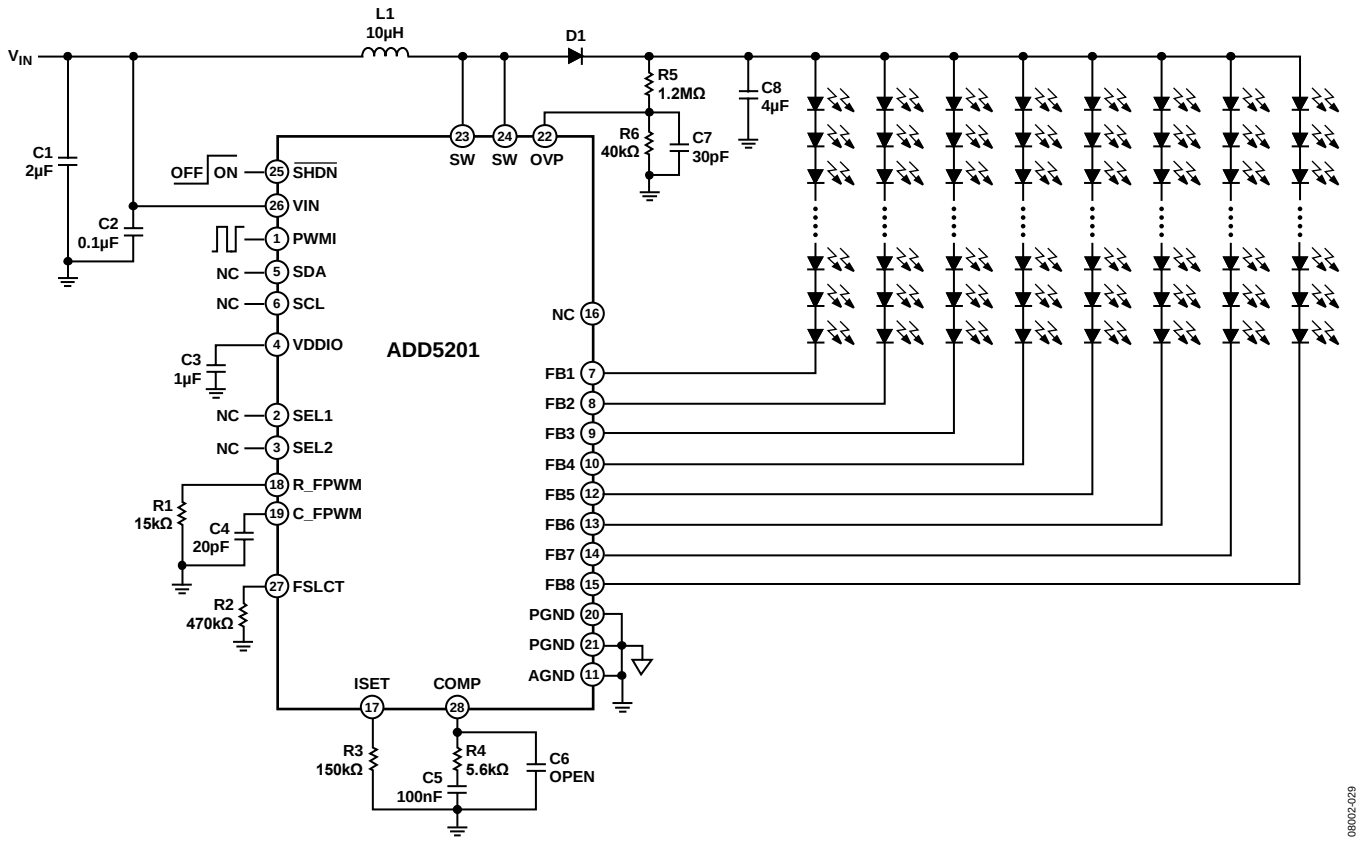

Figure 29. Typical Application Circuits for PWMI Interface with Phase Shift PWM Dimming Mode

OUTLINE DIMENSIONS

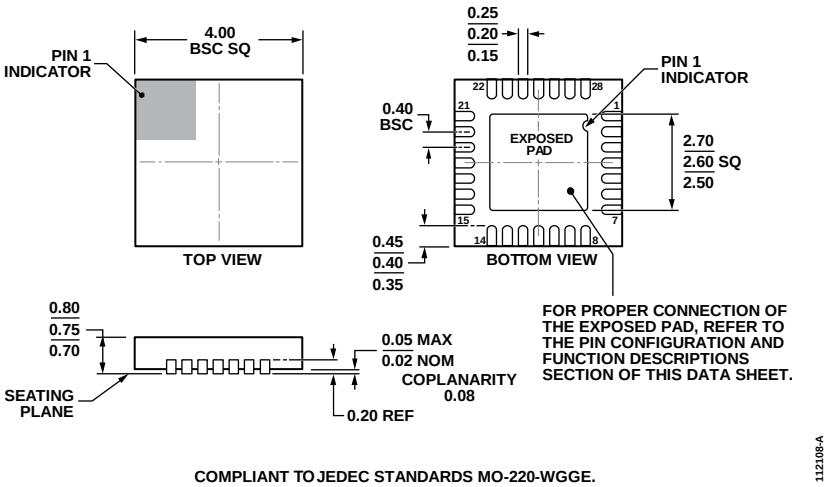

Figure 30. 28-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
4 mm × 4 mm Body, Very Very Thin Quad
(CP-28-5)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADD5201BCPZ-RL	−25°C to +85°C	28-Lead LFCSP_WQ	CP-28-5

[1] Z = RoHS Compliant Part.

D08002-0-4/12(A)