NAND Flash Memory

MT29F8G08ABABA, MT29F8G08ABCBB

Features

- Open NAND Flash Interface (ONFI) 2.0-compliant[1]
- Single-level cell (SLC) technology
- Organization
  - Page size x8: 4,320 bytes (4,096 + 224 bytes)
  - Block size: 128 pages (512K + 28K bytes)
  - Plane size: 2 planes x 1,024 blocks per plane
  - Device size: 8Gb: 2,048 blocks
- Synchronous I/O performance
  - Clock rate: 12ns (DDR)
  - Read/write throughput per pin: 166 MT/s
- Asynchronous I/O performance
  - ^{t}RC/^{t}WC: 25ns (MIN)
- Array performance
  - Read Page: 25µs (MAX)
  - Program Page: 200µs (TYP)
  - Erase Block: 700µs (TYP)
- Operating Voltage Range
  - Vcc: 2.7–3.6V
  - VccQ: 1.7–1.95V, 2.7–3.6V
- Command set: ONFI NAND Flash Protocol
- Advanced Command Set
  - Program Cache
  - Read Cache Sequential
  - Read Cache Random
  - One-time programmable (OTP) mode
  - Multi-plane commands
  - Multi-LUN operations
  - Read Unique ID
  - Copyback
- First block (block address 00h) is valid with ECC[2]
- RESET (FFh) required as first command after power-on
- Operation status byte provides software method for detecting
  - Operation completion
  - Pass/fail condition
  - Write-protect status
- Data strobe (DQS) signals provide a hardware method for synchronizing data I/O in the synchronous interface
- Copyback operations supported within the plane from which data is read
- Quality and reliability
  - Data retention: 10 years
  - Endurance: 100,000 PROGRAM/ERASE cycles[2]
- Operating temperature:
  - Commercial: 0°C to +70°C
  - Industrial: –40°C to +85°C
- Package
  - 48-pin TSOP
  - 52-pad LGA
  - 100-ball BGA

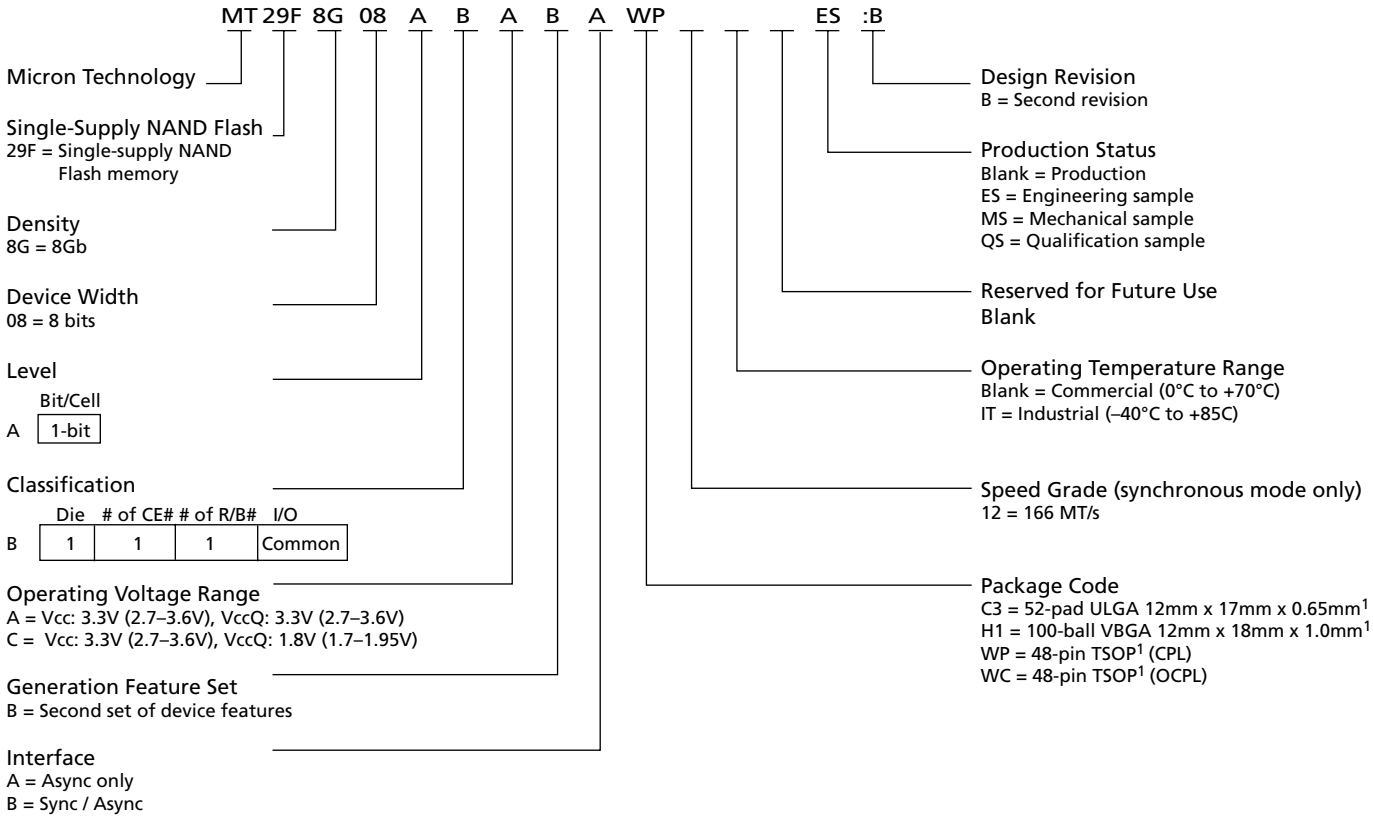
Notes: 1. The ONFI 2.0 specification is available at www.onfi.org.
2. For further details, see “Error Management” on page 95.

Draft 2/ 27/ 2009

Part Numbering Information

Micron NAND Flash devices are available in different configurations and densities (see Figure 1).

Figure 1: Marketing Part Number Chart



Notes: 1. Lead-free package.

Valid Part Number Combinations

After building the part number from the part numbering chart, verify that the part is offered and valid by using the Micron Parametric Part Search Web site at: www.micron.com/products/parametric. If the device required is not on this list, contact the factory.

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General Description

Micron NAND Flash technology provides high-performance NAND Flash memory with an interface that supports up to 166 MT/s data read and write throughput.

Micron NAND Flash devices include two data interfaces—a synchronous interface for high-performance I/O operations, and an asynchronous interface for legacy NAND Flash applications. These devices use a highly multiplexed 8-bit bus (I/O[7:0], DQ[7:0]) to transfer commands, addresses, and data. Data transfers in the synchronous interface include a bidirectional data strobe (DQS). Between the synchronous and asynchronous interfaces there are five control signals used to implement the NAND Flash protocol. In the synchronous interface these signals are CE#, CLE, ALE, CLK, and W/R#; in the asynchronous interface these signals are CE#, CLE, ALE, WE#, and RE#. Additional signals control hardware write protection (WP#) and monitor device status (R/B#).

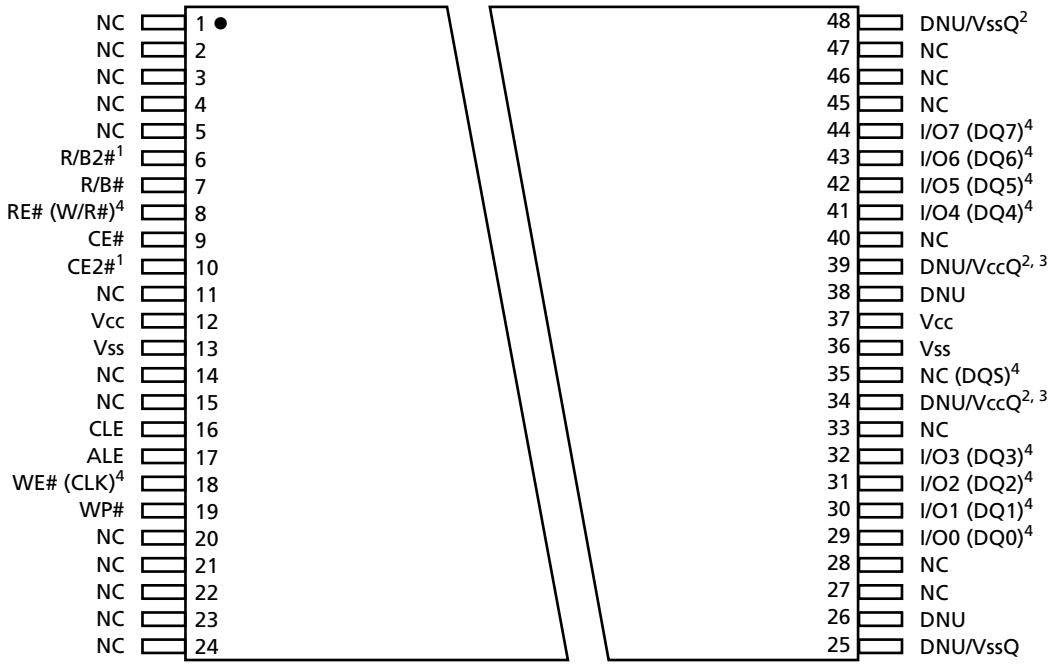
This hardware interface creates a low pin-count device with a standard pinout that remains the same from one density to another, enabling future upgrades to higher densities with no board redesign.

A logical unit (LUN), or die, is the minimum unit that can independently execute commands and report status. There is at least one LUN per CE#. Each LUN contains 2 planes. Each plane consists of 1,024 blocks. Each block is subdivided into 128 programmable pages.

The contents of each page can be programmed in ^{t}PROG, and an entire block can be erased in ^{t}BERS. PROGRAM/ERASE endurance is specified at 100,000 when using appropriate error correction code (ECC).

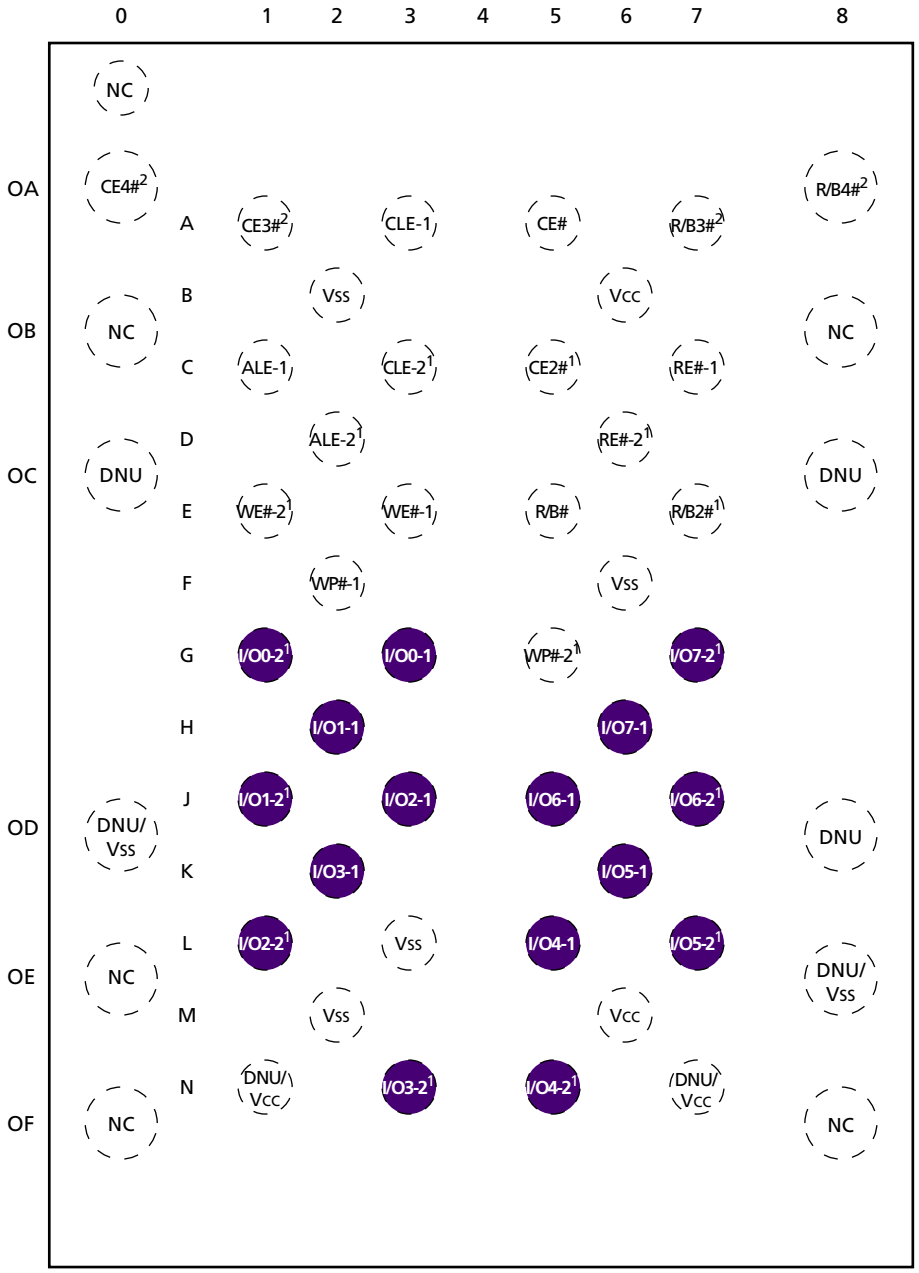
These NAND devices are ONFI 2.0-compliant. The ONFI 2.0 specification can be found at www.onfi.org.

Figure 2: Pin Assignment (Top View) 48-Pin TSOP Type 1



Notes:
1. CE2# and R/B2# on are not available and are treated as NC.
2. For asynchronous devices with VccQ = 3.3V, these signals can be treated as DNU.
3. For synchronous devices with VccQ = 1.8V, these signals must be supplied with a 1.8V voltage supply.
4. Signal names in parentheses are the signal names when the synchronous interface is active.

Figure 3: Pad Assignment (Top View) 52-Pad LGA



Top View, Pads Down

Notes: 1. These pads are currently NC and are shown for future placement
2. These pads are currently NC and are shown for future placement

Figure 4: Ball Assignment – 100-Ball VBGA

Ball-Down Top View

Notes:
1. N/A: This signal is tri-stated when the asynchronous interface is active.
2. Signal names in parentheses are the signal names when the synchronous interface is active.
3. These pads are currently NC and are shown for future placement.

Table 1: Signal Definitions

Symbol[1]		Type	Description[2]
Async	Sync		
ALE, ALE-1, (ALE-2)[3]	ALE, ALE-1, (ALE-2)[3]	Input	**Address latch enable:** Loads an address from I/O[7:0], DQ[7:0] into the address register.
CE#, (CE2#,CE3#,CE4#)[3]	CE#, (CE2#)[3]	Input	**Chip enable:** A signal that enables or disables one or more LUNs in a target[1].
CLE, CLE-1, (CLE-2)[3]	CLE, CLE-1, (CLE-2)[3]	Input	**Command latch enable:** Loads a command from I/O[7:0], DQ[7:0] into the command register.
I/O[7:0], I/O[7:0]-1, DQ[7:0] DQ[7:0]-1 (I/O[7:0]-2)[3] (DQ[7:0]-2)[3]	DQ[7:0], DQ[7:0]-1, (I/O[7:0]-2)[3] (DQ[7:0]-2)[3]	I/O	**Data inputs/outputs:** The bidirectional I/Os transfer address, data, and command information.
N/A	DQS, DQS-1, DQS-2	I/O	**Data strobe:** Provides a synchronous reference for data input and output.
RE#, RE#-1, (RE#-2)[3]	W/R#, W/R#-1, (W/R#-2)[3]	Input	**Read enable and write/read:** RE# transfers serial data from the NAND Flash to the host system when the asynchronous interface is active. When the synchronous interface is active, W/R# controls the direction of DQ[7:0] and DQS.
WE#, WE#-1, (WE#-2)[3]	CLK, CLK-1, (CLE-2)[3]	Input	**Write enable and clock:** WE# transfers commands, addresses, and serial data from the host system to the NAND Flash when the asynchronous interface is active. When the synchronous interface is active, CLK latches command and address cycles.
WP#, WP#-1, (WP#-2)[3]	WP#, WP#-1, (WP#-2)[3]	Input	**Write protect:** WP# is a signal that enables or disables array PROGRAM and ERASE operations.
R/B#, (R/B2#,R/B3#,R/B4#)[3]	R/B#, (R/B2#,R/B3#,R/B4#)[3]	Output	**Ready/busy:** An open-drain, active-low output that requires an external pull-up resistor. This signal indicates target array activity.
Vcc	Vcc	Supply	**Vcc:** Core power supply
VccQ	VccQ	Supply	**VccQ:** I/O power supply
Vss	Vss	Supply	**Vss:** Core ground connection
VssQ	VssQ	Supply	**VssQ:** I/O ground connection
NC	NC	–	**No connect:** NCs are not internally connected. They can be driven or left unconnected.
DNU	DNU	–	**Do not use:** DNUs must be left unconnected.
RFU	RFU	–	**Reserved for future use:** RFUs must be left unconnected.

Notes:
1. See "Device and Array Organization" on page 14 for detailed signal connections.
2. See "Bus Operation" on page 16 for detailed asynchronous and synchronous interface signal-use explanations.
3. These signals are currently NC and are shown for future placement.

Architecture

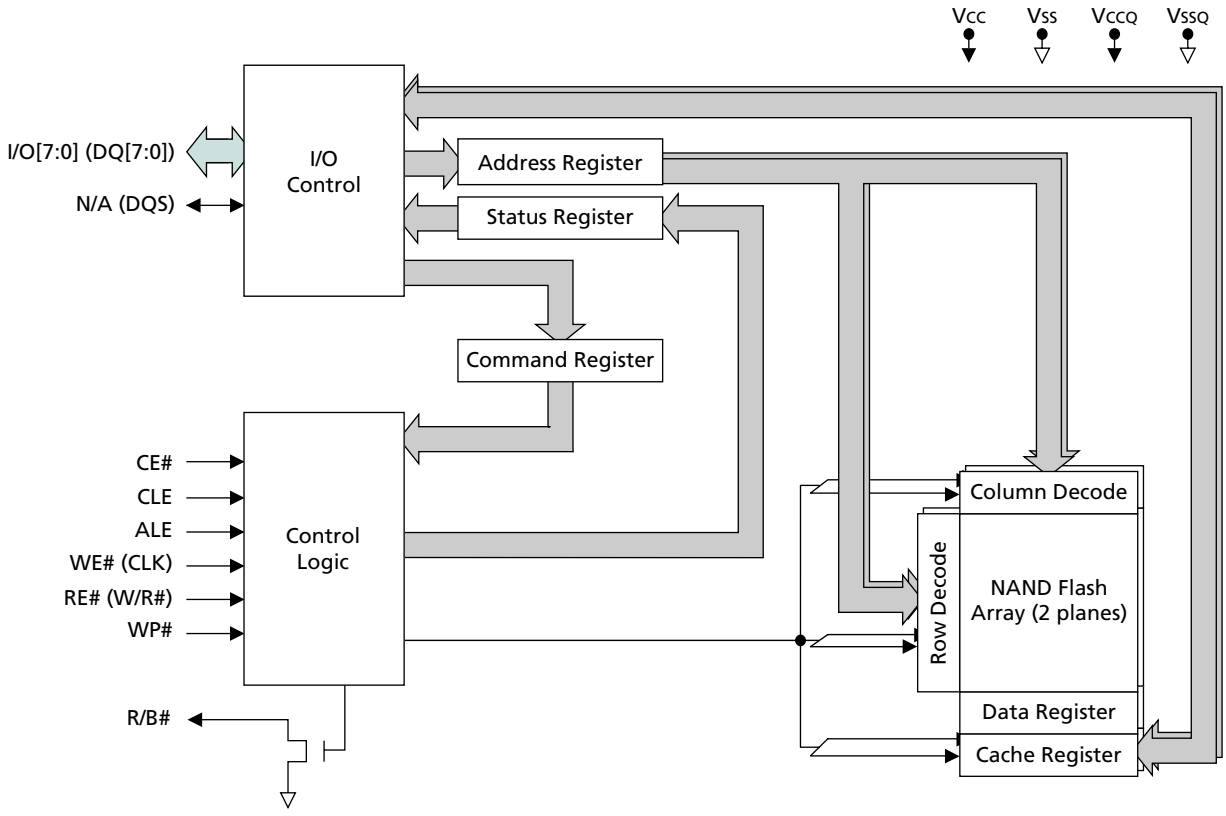
These devices use NAND Flash electrical and command interfaces. Data, commands, and addresses are multiplexed onto the same pins and received by I/O control circuits. The commands received at the I/O control circuits are latched by a command register and are transferred to control logic circuits for generating internal signals to control device operations. The addresses are latched by an address register and sent to a row decoder to select a row address, or to a column decoder to select a column address.

Data is transferred to or from the NAND Flash memory array, byte-by-byte, through a data register and a cache register. See Figure 5 for details.

The NAND Flash memory array is programmed and read using page-based operations and is erased using block-based operations. During normal page operations, the data and cache registers act as a single register. During cache operations, the data and cache registers operate independently to increase data throughput.

The status register reports the status of LUN operations.

Figure 5: NAND Flash LUN Functional Block Diagram



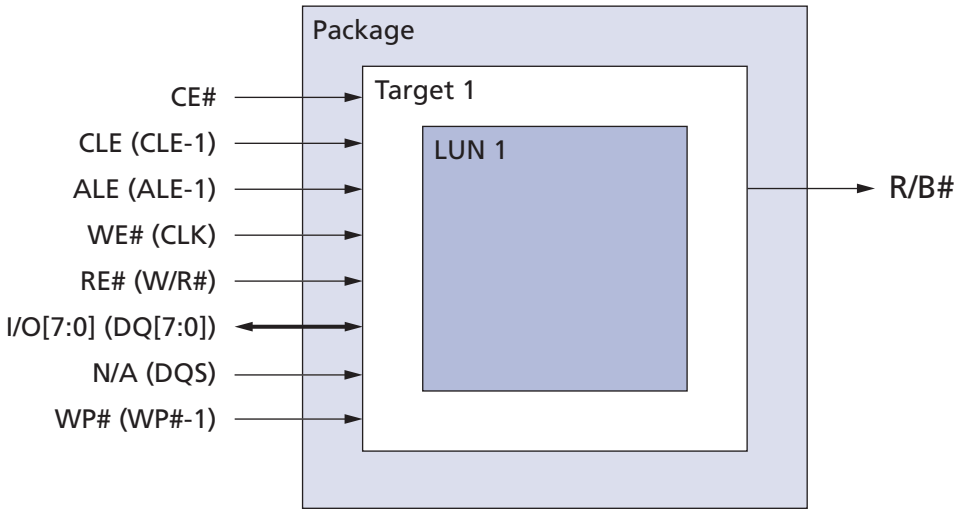
Notes:
1. N/A: This signal is tri-stated when the asynchronous interface is active.
2. Signal names in parentheses are the signal names when the synchronous interface is active.

Addressing and Memory Map

NAND Flash devices do not contain dedicated address pins. Addresses are loaded using a 5-cycle sequence shown in Table 2 on page 23.

Device and Array Organization

Figure 6: Device Organization for Single-Die Package (TSOP/BGA)



Notes: 1. Signal names not in parentheses are for TSOP packages. Signal names in parentheses are for BGA packages.

Figure 7: Device Organization for Single-Die Package (LGA)

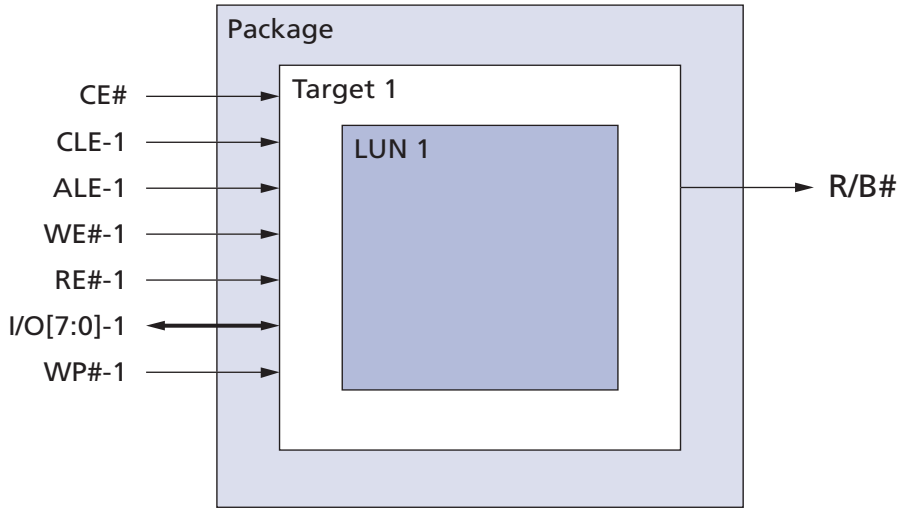


Figure 8: Array Organization for 8Gb Logical Unit (LUN)

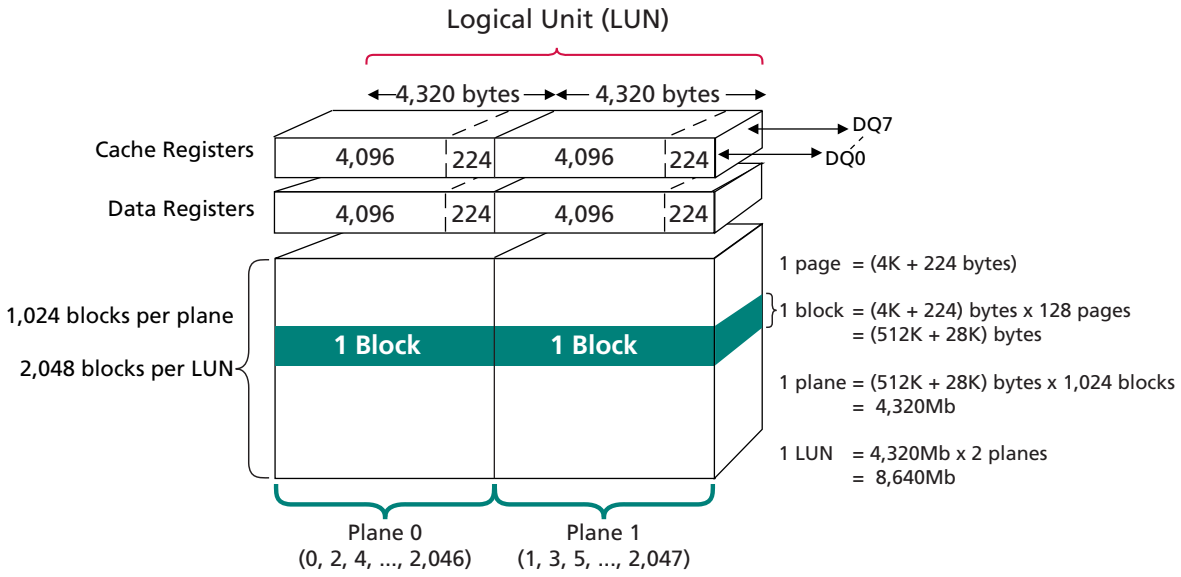


Table 2: Array Addressing for 8Gb Logical Unit (LUN)

Cycle	I/O7 (DQ7)	I/O6 (DQ6)	I/O5 (DQ5)	I/O4 (DQ4)	I/O3 (DQ3)	I/O2 (DQ2)	I/O1 (DQ1)	I/O0 (DQ0)
First	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0[2]
Second	LOW	LOW	LOW	CA12[3]	CA11	CA10	CA9	CA8
Third	BA7[4]	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Fourth	BA15	BA14	BA13	BA12	BA11	BA10	BA9	BA8
Fifth	LOW	LOW	LOW	LOW	LOW	LOW	BA17	BA16

Notes:
1. CAx = column address, PAx = page address, BAx = block address, LAx = LUN address; the page address, block address, and LUN address are collectively called the row address.
2. When using the synchronous interface, CA0 is forced to 0 internally; one data cycle always returns one even byte and one odd byte.
3. Column addresses 4,320 (10E0h) through 8,191 (1FFFh) are invalid, "out of bounds," do not exist in the device, and cannot by addressed.
4. BA[8] is the plane-select bit:
   Plane 0: BA[7] = "0"
   Plane 1: BA[7] = "1"

Bus Operation

These NAND Flash devices have two interfaces: a synchronous interface for fast data I/O transfer and an asynchronous interface that is backwards compatible with existing NAND Flash devices.

The NAND Flash command protocol for both the asynchronous and synchronous interfaces is identical. However, there are some differences between the asynchronous and synchronous interfaces when issuing command, address, and data I/O cycles using the NAND Flash signals.

Asynchronous Interface

The asynchronous interface is active when the NAND Flash device powers on to provide compatibility with existing NAND controllers that may not support the synchronous interface. The DQS signal is tri-stated when the asynchronous interface is active.

Asynchronous interface bus modes are summarized in Table 3 on page 16.

Table 3: Asynchronous Interface Mode Selection

Mode	CE#	CLE	ALE	WE#	RE#	DQS[1]	I/O[7:0] DQ[7:0]	WP#[2]
Standby	H	X	X	X	X	X	X	0V/VccQ[2]
Bus idle	L	X	X	H	H	X	X	X
Command input	L	H	L	⌐	H	X	X	H
Address input	L	L	H	⌐	H	X	X	H
Data input	L	L	L	⌐	H	X	X	H
Data output	L	L	L	H	⌙	X	X	X
Write protect	X	X	X	X	X	X	X	L

Notes:
1. DQS is tri-stated when the asynchronous interface is active.
2. WP# should be biased to CMOS LOW or HIGH for standby.
3. Mode selection settings for this table: H = Logic level HIGH; L = Logic level LOW; X = VIH or VIL.

Asynchronous Enable/Standby

A target is disabled when CE# is driven HIGH, even when the target is busy. When CE# is driven LOW, all of the signals for that target are enabled. With CE# LOW, the target can accept commands, addresses, and data I/O. There may be more than one target in a NAND Flash package. Each target is controlled by its own CE#; the first target is controlled by CE#; the second target (if present) is controlled by CE2#, etc.

A target is disabled when CE# is driven HIGH, even when the target is busy. All of the target's signals are disabled except CE#, WP#, and R/B#. This enables the NAND Flash to share the same memory bus with other Flash or SRAM devices. While the target is disabled, other devices on the memory bus can be accessed.

A target enters low-power standby when it is disabled and is not busy. If the target is busy when it is disabled, the target enters standby after all of the LUNs complete their operations. Standby helps reduce power consumption.

Asynchronous Bus Idle

A target's bus is idle when CE# is LOW, WE# is HIGH, and RE# is HIGH.

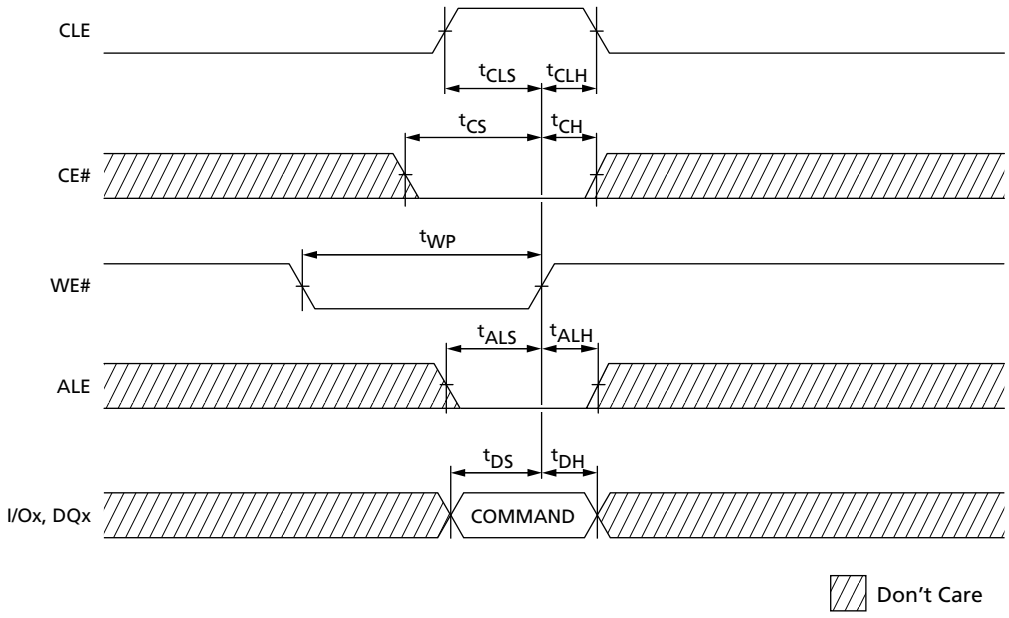
During bus idle, all of the signals are enabled except DQS, which is not used when the asynchronous interface is active. No commands, addresses, and data are latched into the target; no data is output.

Asynchronous Commands

An asynchronous command is written from I/O[7:0], DQ[7:0] to the command register on the rising edge of WE# when CE# is LOW, ALE is LOW, CLE is HIGH, andRE# is HIGH.

Commands are typically ignored by LUNs that are busy; however, some commands, including READ STATUS (70h) and SELECT LUN WITH STATUS (78h), are accepted by LUNs even when they are busy.

Figure 9: Asynchronous COMMAND LATCH Cycle



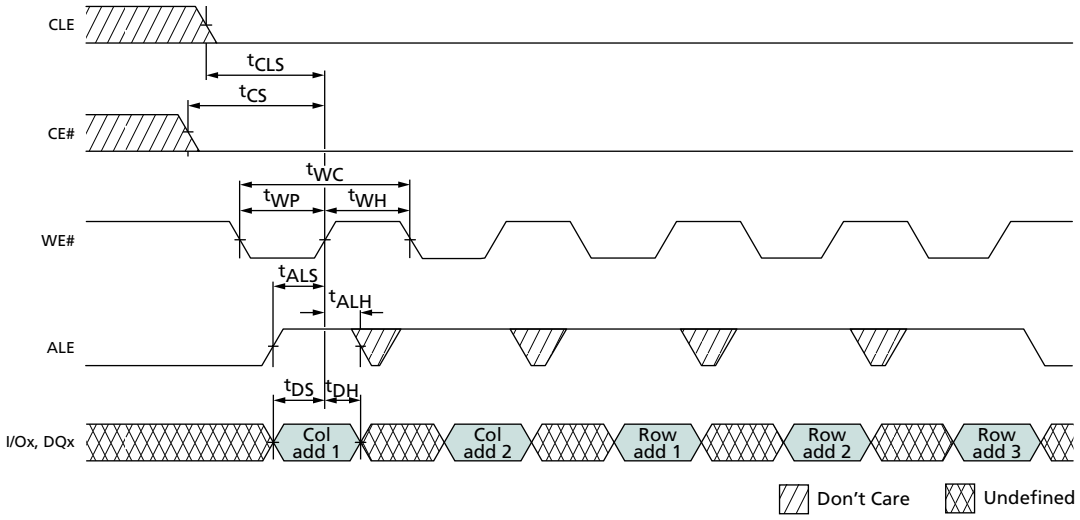
Asynchronous Addresses

An asynchronous address is written from I/O[7:0], DQ[7:0] to the address register on the rising edge of WE# when CE# is LOW, ALE is HIGH, CLE is LOW, and RE# is HIGH.

Bits that are not part of the address space must be LOW (see Table 2 on page 23). The number of cycles required for each command varies. Refer to the command descriptions to determine addressing requirements (see “Command Definitions” on page 39").

Addresses are typically ignored by LUNs that are busy; however, some addresses are accepted by LUNs even when they are busy; for example, like address cycles that follow the SELECT LUN WITH STATUS (78h) command.

Figure 10: Asynchronous ADDRESS LATCH Cycle



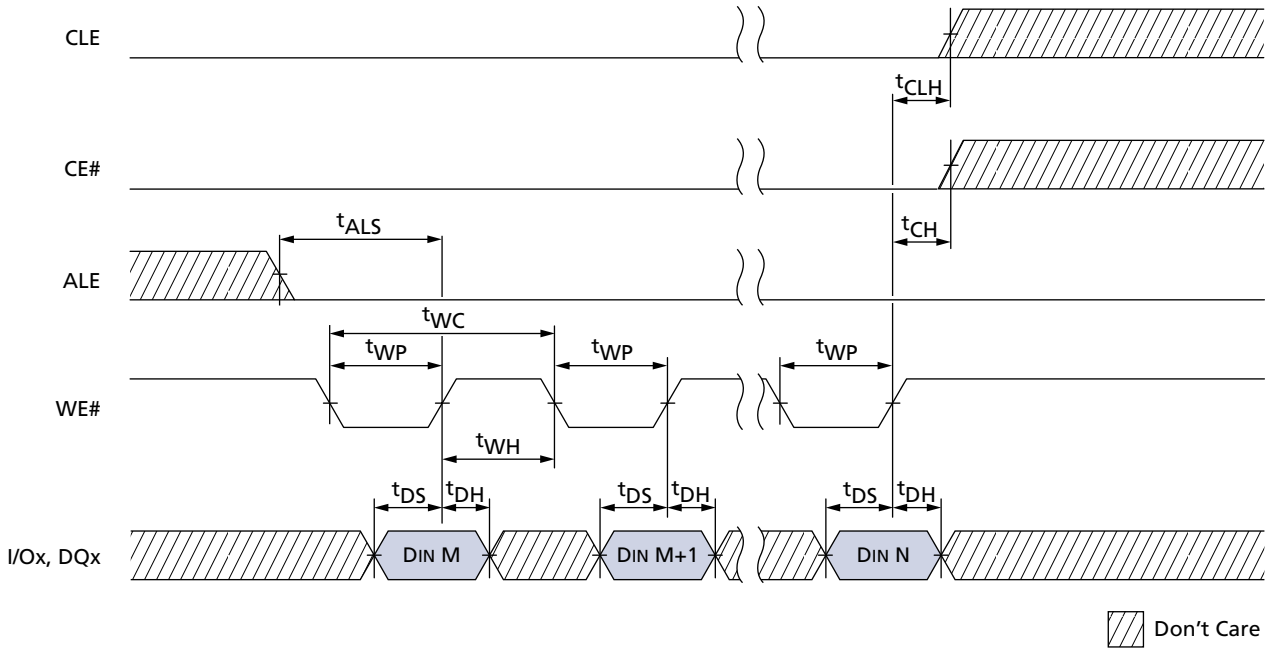
Asynchronous Data Input

Data is written from I/O[7:0], DQ[7:0] to the cache register of the selected LUN on the rising edge of WE# when:

- CE# is LOW,
- ALE is LOW,
- CLE is LOW, and
- RE# is HIGH.

Data input is ignored by LUNs that are not selected or are busy, except if the LUN is busy with a PROGRAM PAGE CACHE MODE operation.

Figure 11: Asynchronous Data Input Cycles



Asynchronous Data Output

Data can be output from a LUN if it is in a READY state. Data output is supported following a READ operation from the NAND Flash array.

Data is output from the cache register of the selected LUN to I/O[7:0], DQ[7:0] on the falling edge of RE# when:

- CE# is LOW,
- ALE is LOW,
- CLE is LOW, and
- WE# is HIGH.

If the host controller is using a ^{t}RC of 30ns or greater, the host can latch the data on the rising edge of RE# (see Figure 12 on page 20).

If the host controller is using a ^{t}RC of less than 30ns, the host can latch the data on the next falling edge of RE# [see Figure 13 on page 20 for extended data output (EDO) timing].

Using the SELECT LUN WITH STATUS (78h) command prevents data contention following a multi-LUN operation. Once a SELECT LUN WITH STATUS (78h) command has been issued to a LUN, then issue the READ MODE (00h) command. Data can now be output from the selected LUN.

Data output requests are typically ignored by a LUN that is busy; however, it is possible to output data from the status register even when a LUN is busy by first issuing the READ STATUS or SELECT LUN WITH STATUS (78h) command.

Figure 12: Asynchronous Data Output Cycles

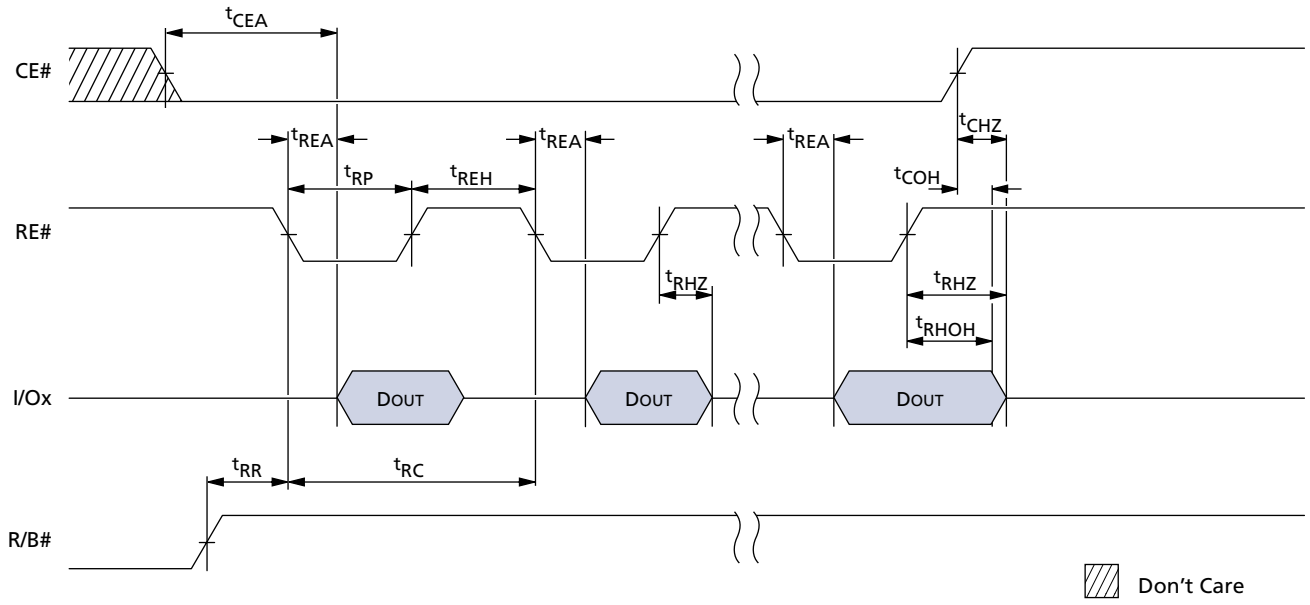
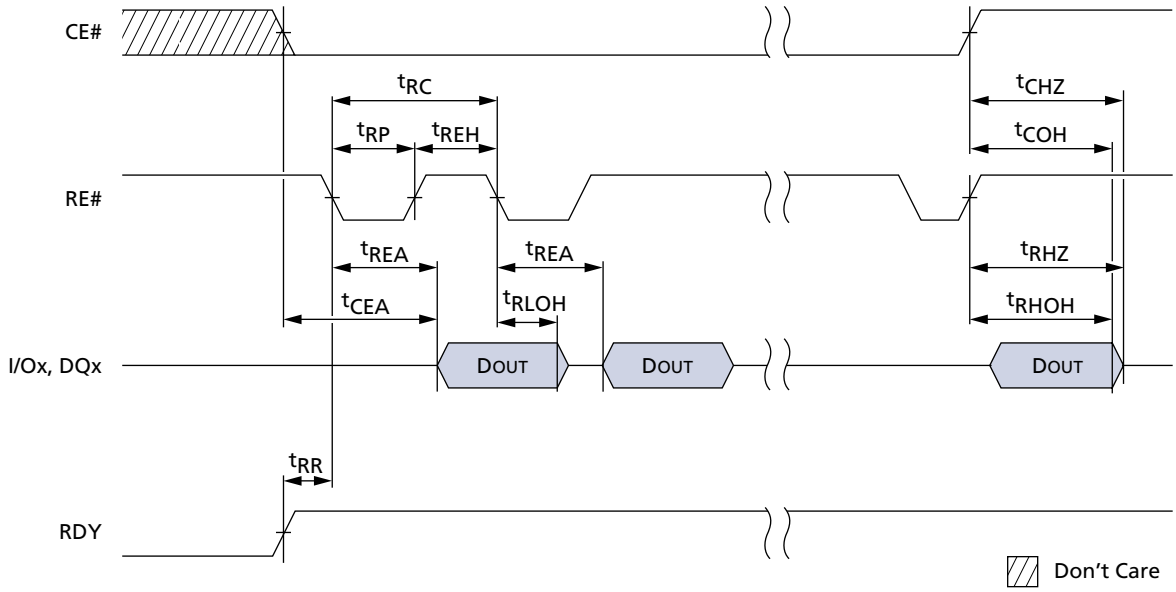


Figure 13: Asynchronous Data Output Cycles (EDO Mode)



Write Protect (WP#)

The WP# signal enables or disables PROGRAM and ERASE operations to a target. When WP# is LOW, PROGRAM and ERASE operations are disabled. When WP# is HIGH, PROGRAM and ERASE operations are enabled.

It is recommended that the host drive WP# LOW during power-on until Vcc and VccQ are stable to prevent inadvertent PROGRAM and ERASE operations (see "Vcc Power Cycling" on page 35 for additional details).

WP# must be transitioned only when the target is not busy and prior to beginning a command sequence. After a command sequence is complete and the target is ready, WP# can be transitioned. After WP# is transitioned the host must wait ^{t}WW before issuing a new command.

The WP# signal is always an active input, even when CE# is HIGH. This signal should not be multiplexed with other signals.

Ready/Busy# (R/B#)

The R/B# signal provides a hardware method of indicating whether a target is ready or busy. A target is busy when one or more of its LUNs are busy (RDY = "0"). A target is ready when all of its LUNs are ready (RDY = "1"). Because each LUN contains a status register, it is possible to determine the independent status of each LUN by polling its status register instead of using the R/B# signal (see "Status Operations" on page 56 for details regarding LUN status).

This signal requires a pull-up resistor, Rp, for proper operation. R/B# is HIGH when the target is ready, and transitions LOW when the target is busy. The signal's open-drain driver enables multiple R/B# outputs to be OR-tied. Typically, R/B# is connected to an interrupt pin on the system controller (see Figure 14 on page 22).

The combination of Rp and capacitive loading of the R/B# circuit determines the rise time of the R/B# signal. The actual value used for Rp depends on the system timing requirements. Large values of Rp cause R/B# to be delayed significantly. Between the 10- to 90-percent points on the R/B# waveform, the rise time is approximately two time constants (TC).

$$TC = R \times C$$

Where R = Rp (resistance of pull-up resistor), and C = total capacitive load.

The fall time of the R/B# signal is determined mainly by the output impedance of the R/B# signal and the total load capacitance. Approximate Rp values using a circuit load of 100pF are provided in Figure 19 on page 24.

The minimum value for Rp is determined by the output drive capability of the R/B# signal, the output voltage swing, and VCCQ.

$$Rp = \frac{VCC(MAX) - VOL(MAX)}{IOL + \Sigma IL}$$

Where ΣIL is the sum of the input currents of all devices tied to the R/B# pin.

Figure 14: READ/BUSY# Open Drain

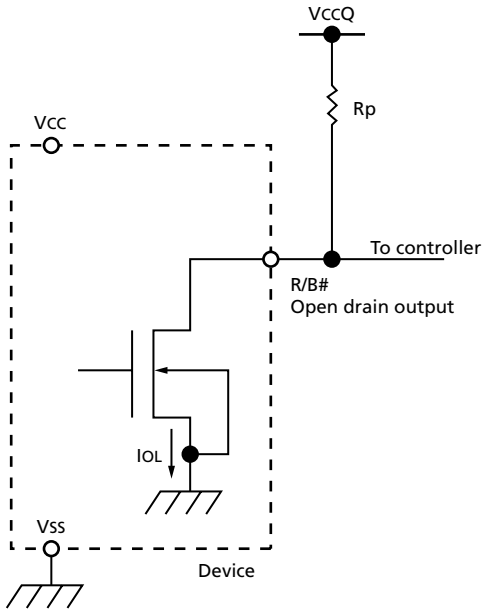
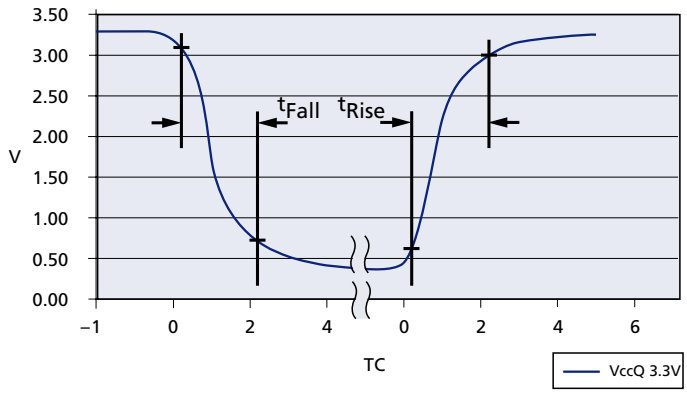
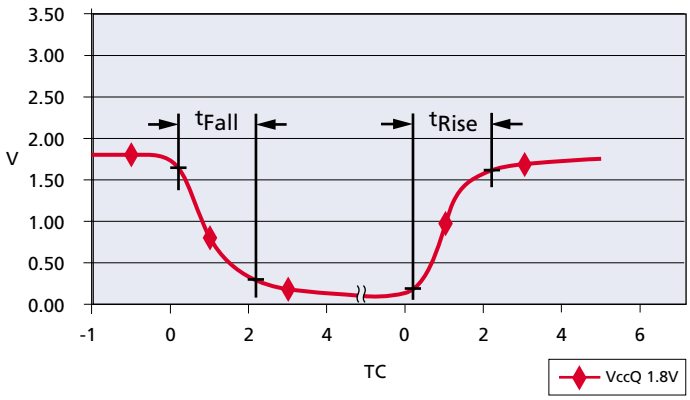


Figure 15: ^{t}Fall and ^{t}Rise (VccQ = 3.3V)



Notes:
1. ^{t}Fall and ^{t}Rise calculated at 10 percent.90 percent points.
2. ^{t}Rise dependent on external capacitance and resistive loading and output transistor impedance.
3. ^{t}Rise primarily dependent on external pull-up resistor and external capacitive loading.
4. ^{t}Fall =10ns at 3.3V
5. See TC values in Figure 19 on page 24 for approximate Rp value and TC.

Figure 16: ^{t}Fall and ^{t}Rise (VccQ = 1.8V)



Notes:
1. ^{t}Fall and ^{t}Rise are calculated at 10 percent and 90 percent points.
2. ^{t}Rise is primarily dependent on external pull-up resistor and external capacitive loading.
3. ^{t}Fall ≈ 7ns at 1.8V.
4. See TC values in Figure 19 on page 24 for TC and approximate Rp value.

Figure 17: IOL vs. Rp (VccQ = 3.3V)

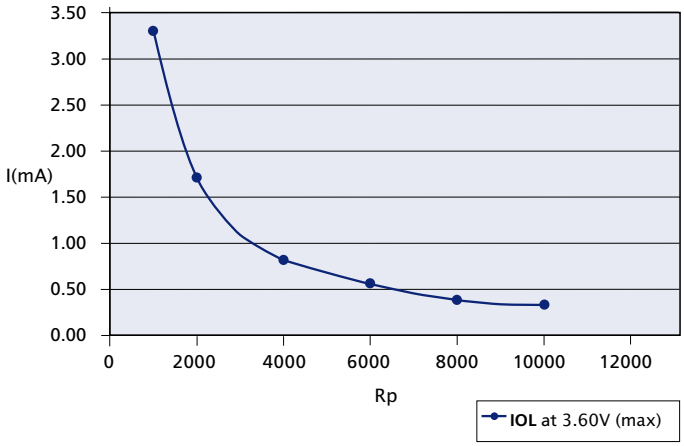


Figure 18: IOL vs. Rp (1.8V)

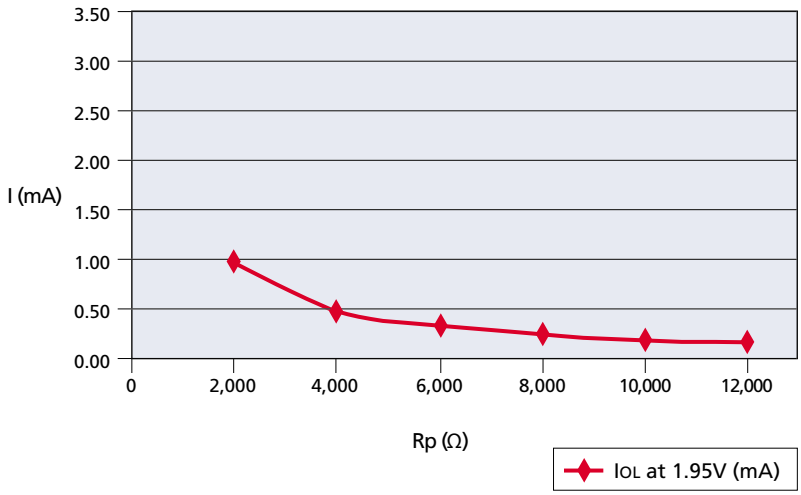
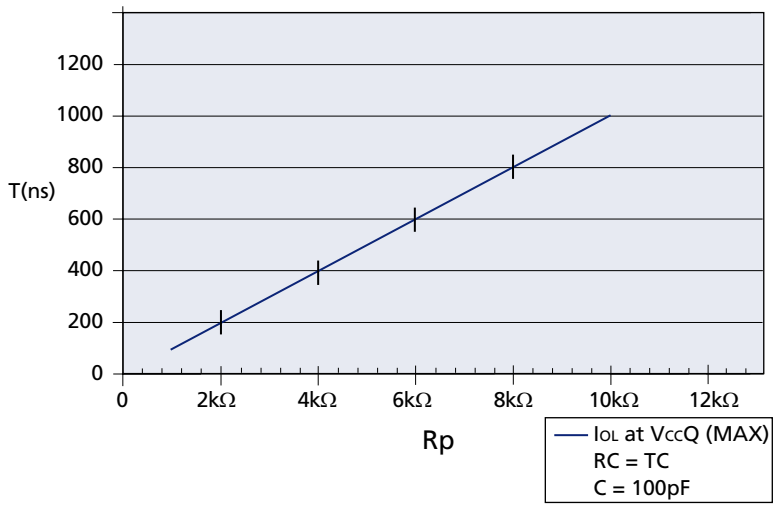


Figure 19: TC vs. Rp



Synchronous Interface

When the synchronous interface is activated on a target (see "Activating the Synchronous Interface" on page 37), the target is capable of high-speed DDR data transfers. Existing signals are redefined for high-speed DDR I/O. The WE# signal becomes CLK. DQS is enabled. The RE# signal becomes W/R#.

CLK provides a clock reference to the NAND Flash device.

DQS is a bidirectional data strobe. During data output, DQS is driven by the NAND Flash device. During data input, DQS is controlled by the host controller while inputting data on DQ[7:0].

The direction of DQS and DQ[7:0] is controlled by the W/R# signal. When the W/R# signal is latched HIGH, the controller is driving the DQ bus and DQS. When the W/R# is latched LOW, the NAND Flash is driving the DQ bus and DQS.

The synchronous interface bus modes are summarized in Table 4.

Table 4: Synchronous Interface Mode Selection

Mode	CE#	CLE	ALE	CLK[1]	W/R#	DQS	DQ[7:0]	WP#[2]	Notes
Standby	H	X	X	X	X	X	X	0V/VccQ	
Bus idle	L	L	L		H	X	X	X	
Bus driving	L	L	L		L	output	X	X	
Command input	L	H	L		H	X	X	H	3
Address input	L	L	H		H	X	X	H	3
Data input	L	H	H		H		X	H	4
Data output	L	H	H		L	note 5	X	X	5
Write protect	X	X	X	X	X	X	X	L	
Undefined	L	L	H		L	X	X	X	
Undefined	L	H	L		L	X	X	X	

Notes:
1. CLK can be stopped when the target is disabled, even when R/B# is LOW.
2. WP# should be biased to CMOS LOW or HIGH for standby.
3. Commands and addresses are latched on the rising edge of CLK.

4. During data input to the device, DQS is the "clock" that latches the data in the cache register.
5. During data output from the NAND Flash device, DQS is an output generated from CLK after ^{t}DQSCK delay.
6. Mode selection settings for this table: H = Logic level HIGH; L = Logic level LOW; X = V_{IH} or V_{IL}.

Synchronous Enable/Standby

In addition to the description in the section "Asynchronous Enable/Standby" on page 16, the following requirements also apply when the synchronous interface is active.

Before enabling a target, CLK must be running and ALE and CLE must be LOW. When CE# is driven LOW, all of the signals for the selected target are enabled. The target is not enabled until ^{t}CS completes; the target's bus is then idle.

Prior to disabling a target, the target's bus must be idle (see "Synchronous Bus Idle/Driving" on page 26). A target is disabled when CE# is driven HIGH, even when it is busy. All of the target's signals are disabled except CE#, WP#, and R/B#. After the target is disabled, CLK can be stopped.

A target enters low-power standby when it is disabled and is not busy. If the target is busy when it is disabled, the target enters standby after all of the LUNs complete their operations.

Synchronous Bus Idle/Driving

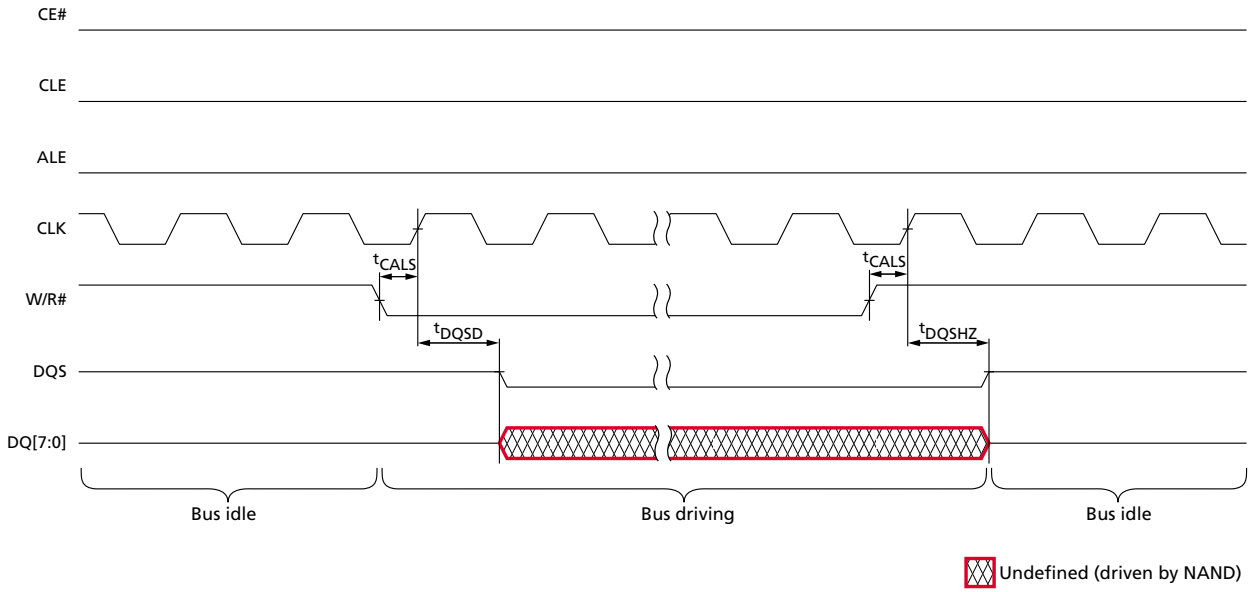
A target's bus is idle or driving when:

- CLK is running,
- CE# is LOW,
- ALE is LOW, and
- CLE is LOW.

The bus is idle when W/R# transitions HIGH and is latched by CLK. During the bus idle mode, all signals are enabled; DQS and DQ[7:0] are inputs. No commands, addresses, or data are latched into the target; no data is output. When entering the bus idle mode, the host must wait a minimum of ^{t}CAD before changing the bus mode. In the bus idle mode, the only valid bus modes supported are: bus driving, command, address, and DDR data input.

The bus is driving when W/R# transitions LOW and is latched by CLK. During the bus driving mode, all signals are enabled; DQS is LOW and DQ[7:0] is driven LOW or HIGH, but no valid data is output. Following the bus driving mode, the only valid bus modes supported are bus idle and DDR data output.

Figure 20: Synchronous Bus Idle/Driving Behavior



Notes: 1. Only the selected LUN drives DQS and DQ[7:0]. During a multi-LUN operation, the host must use the SELECT LUN WITH STATUS (78h) to prevent data output contention.

Synchronous Commands

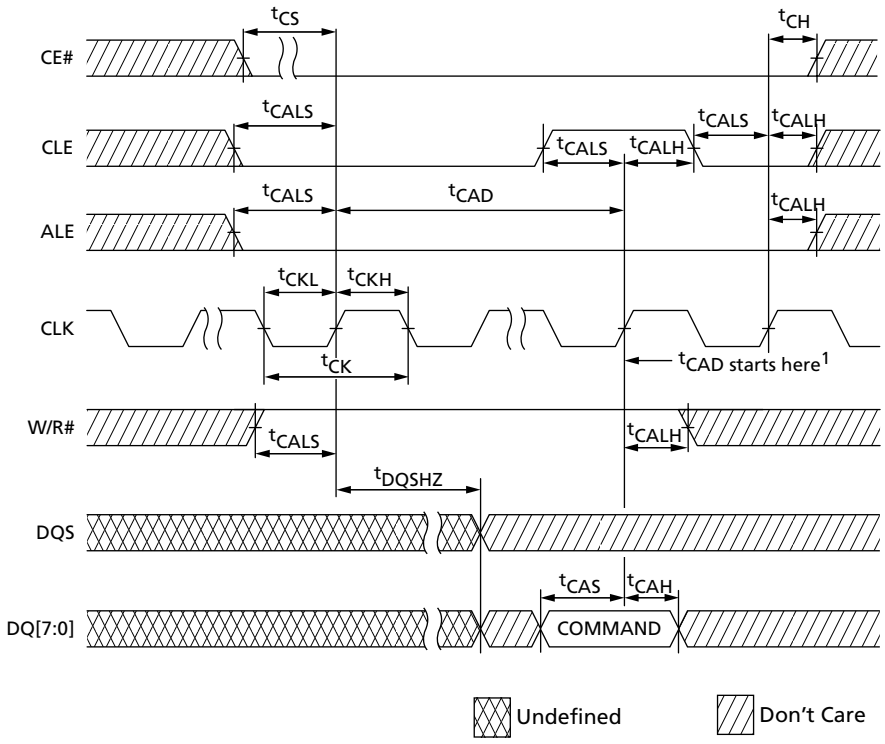
A command is written from DQ[7:0] to the command register on the rising edge of CLK when:

- CE# is LOW,
- ALE is LOW,
- CLE is HIGH, and
- W/R# is HIGH.

After a command is latched, and prior to issuing the next command, address, or data I/O, the bus must go to the bus idle mode on the next rising edge of CLK, except when the clock period, ^{t}CK, is greater than ^{t}CAD.

Commands are typically ignored by LUNs that are busy; however, some commands, such as READ STATUS (70h) and SELECT LUN WITH STATUS (78h), are accepted by LUNs, even when they are busy (see Table 5 on page 39).

Figure 21: Synchronous Command Cycle



Notes: 1. When CE# remains LOW, ^{t}CAD begins at the rising edge of the clock from which the command cycle is latched for subsequent command, address, data input, or data output cycle(s).

Synchronous Addresses

A synchronous address is written from DQ[7:0] to the address register on the rising edge of CLK when:

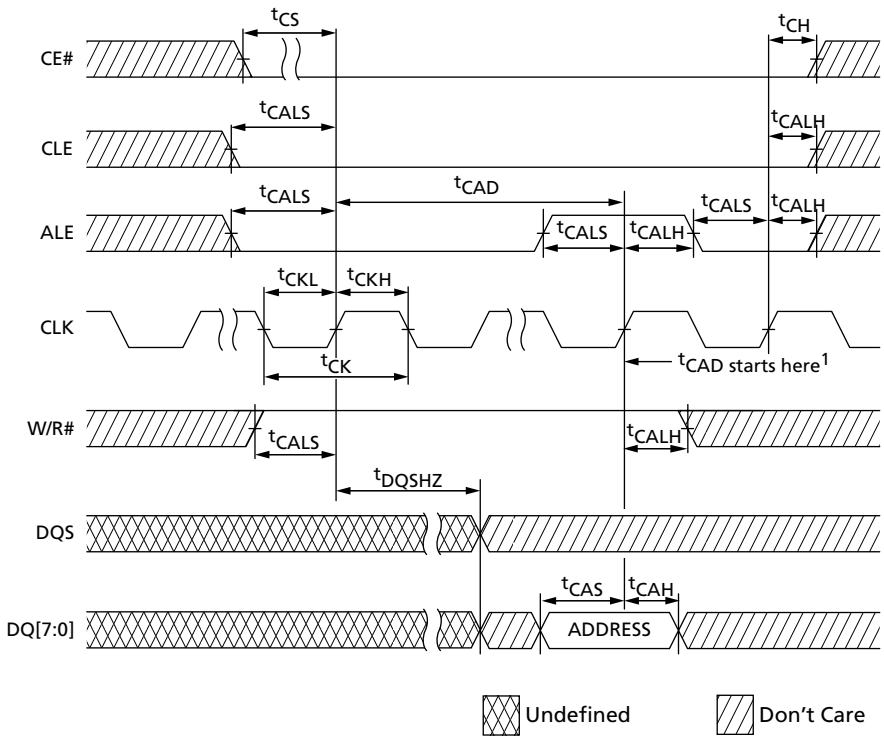
- CE# is LOW,
- ALE is HIGH,
- CLE is LOW, and
- W/R# is HIGH.

After an address is latched, and prior to issuing the next command, address, or data I/O, the bus must go to the bus idle mode on the next rising edge of CLK, except when the clock period, ^{t}CK, is greater than ^{t}CAD.

Bits not part of the address space must be LOW (see Table 2 on page 23). The number of ADDRESS cycles required for each command varies. Refer to the command descriptions to determine addressing requirements (see Table 5 on page 39).

Addresses are typically ignored by LUNs that are busy; however, some addresses such as address cycles that follow the SELECT LUN WITH STATUS (78h) command, are accepted by LUNs, even when they are busy (see Table 5 on page 39).

Figure 22: Synchronous Address Cycle



Notes: 1. When CE# remains LOW, ^{t}CAD begins at the rising edge of the clock from which the command cycle is latched for subsequent command, address, data input, or data output cycle(s).

Synchronous DDR Data Input

To enter the DDR data input mode, the following conditions must be met:

- CLK is running,
- CE# is LOW,
- W/R# is HIGH,
- ^{t}CAD is met,
- DQS is LOW, and
- ALE and CLE are HIGH on the rising edge of CLK.

Upon entering the DDR data input mode after ^{t}DQSS, data is written from DQ[7:0] to the cache register on each and every rising and falling edge of DQS (center-aligned) when:

- CLK is running and the DQS-to-CLK skew meets ^{t}DSH and ^{t}DSS,
- CE# is LOW,
- W/R# is HIGH, and
- ALE and CLE are HIGH on the rising edge of CLK.

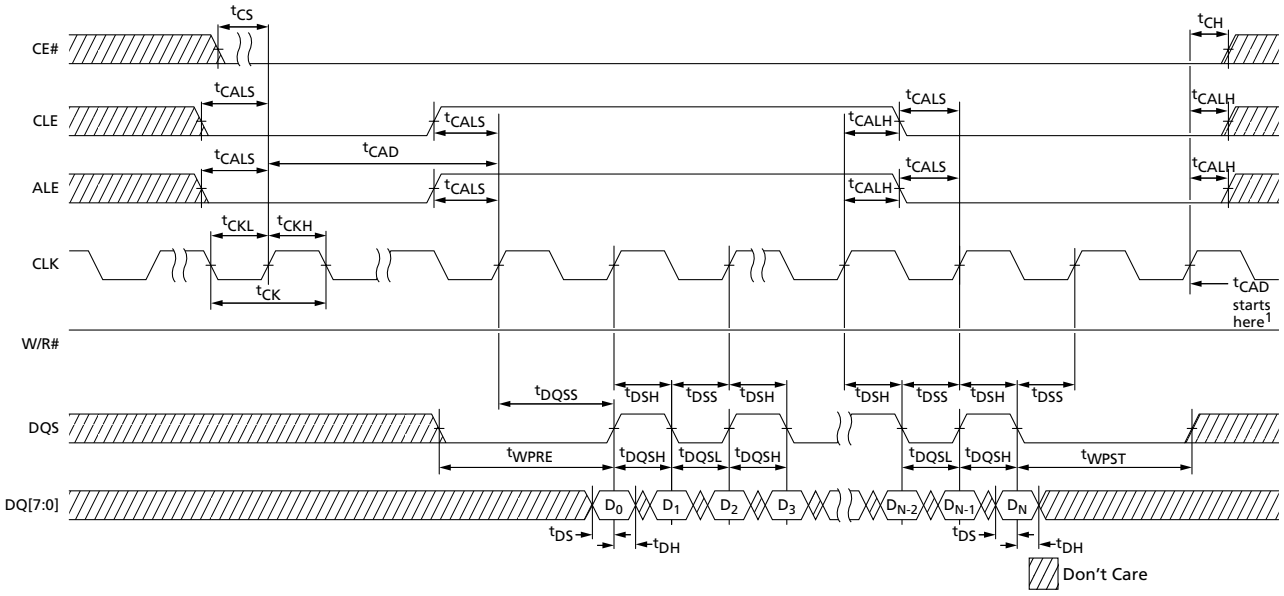
To exit DDR Data Input mode the following conditions must be met:

- CLK is running and the DQS-to-CLK skew meets ^{t}DSH and ^{t}DSS,
- CE# is LOW,
- W/R# is HIGH,
- ALE and CLE are latched LOW on the rising edge of CLK,
- The final two data bytes of the data input sequence are written from DQ[7:0] to the cache register on the final rising and falling edges of DQS after the last cycle in the data input sequence ALE and CLE are latched HIGH, and
- After the final falling edge of DQS, it is held low for ^{t}WPST.

Following ^{t}WPST, the bus enters bus idle mode and ^{t}CAD begins on the next rising edge of CLK. After ^{t}CAD starts, the host can disable the target if desired.

Data input is ignored by LUNs that are not selected or are busy.

Figure 23: Synchronous DDR Data Input Cycles



Notes:
1. When CE# remains LOW, ^{t}CAD begins at the first rising edge of the clock after ^{t}WPST completes.
2. ^{t}DSH (MIN) generally occurs during ^{t}DQSS (MIN).
3. ^{t}DSS (MIN) generally occurs during ^{t}DQSS (MAX).

Synchronous DDR Data Output

Data can be output from a LUN if it is ready. Data output is supported following a READ operation from the NAND Flash array.

To enter the DDR data output mode, the following conditions must be met:

- CLK is running,
- CE# is LOW,
- The host has released the DQ[7:0] bus and DQS,
- W/R# is latched LOW on the rising edge of CLK to enable the selected LUN to take ownership of the DQ[7:0] bus and DQS within ^{t}WRCK,
- ^{t}CAD is met, and
- ALE and CLE are HIGH on the rising edge of CLK.

Upon entering the DDR data output mode, DQS will toggle HIGH and LOW with a delay of ^{t}DQSCK from the respective rising and falling edges of CLK. DQ[7:0] will output data edge-aligned to the rising and falling edges of DQS, with the first transition delayed by no more than ^{t}AC.

DDR data output mode continues as long as:

- CLK is running,
- CE# is LOW,
- W/R# is LOW, and
- ALE and CLE are HIGH on the rising edge of CLK.

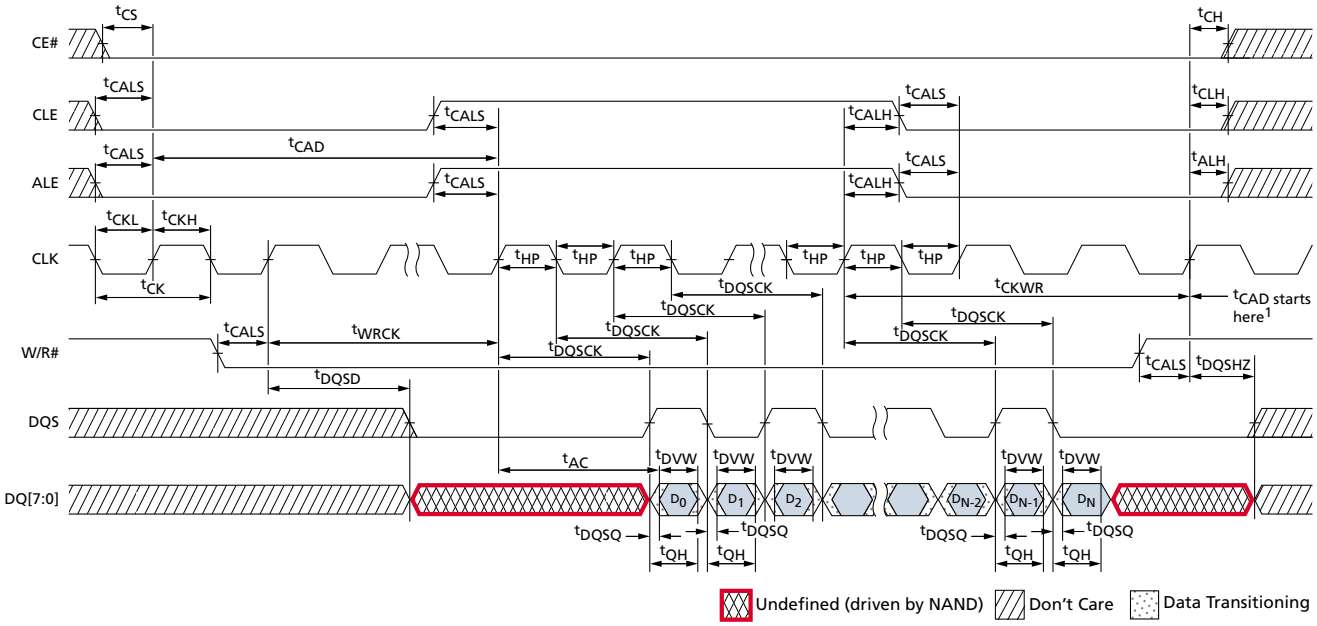
To exit DDR data output mode, the following conditions must be met:

- CLK is running,
- CE# is LOW,
- W/R# is LOW, and
- ALE and CLE are latched LOW on the rising edge of CLK.

The final two data bytes will be output on DQ[7:0] on the final rising and falling edges of DQS. The final rising and falling edges of DQS occur ^{t}DQSCK after the last cycle in the data output sequence where ALE and CLE are latched HIGH. After ^{t}CKWR, the bus enters bus idle mode, and ^{t}CAD begins on the next rising edge of CLK. After ^{t}CAD starts, the host can disable the target if desired.

Data output requests are typically ignored by a LUN that is busy; however, it is possible to output data from the status register even when a LUN is busy by issuing the READ STATUS (70h) or SELECT LUN WITH STATUS (78h) command.

Figure 24: Synchronous DDR Data Output Cycles



Notes:
1. When CE# remains LOW, tCAD begins at the rising edge of the clock after tCKWR for subsequent command or data output cycle(s).
2. See Figure 21 on page 28 for details of W/R# behavior.
3. tAC is the DQ output window relative to CLK and is the long-term component of DQ skew.
4. For W/R# transitioning HIGH: DQ[7:0] and DQS go to tri-state.
5. For W/R# transitioning LOW: DQ[7:0] drives current state and DQS goes LOW.
6. After final data output, DQ[7:0] is driven until W/R# goes HIGH, but is not valid.

Write Protect

See “Write Protect (WP#)” on page 21 under “Asynchronous Interface”.

Ready/Busy#

See “Ready/Busy# (R/B#)” on page 21 under “Asynchronous Interface”.

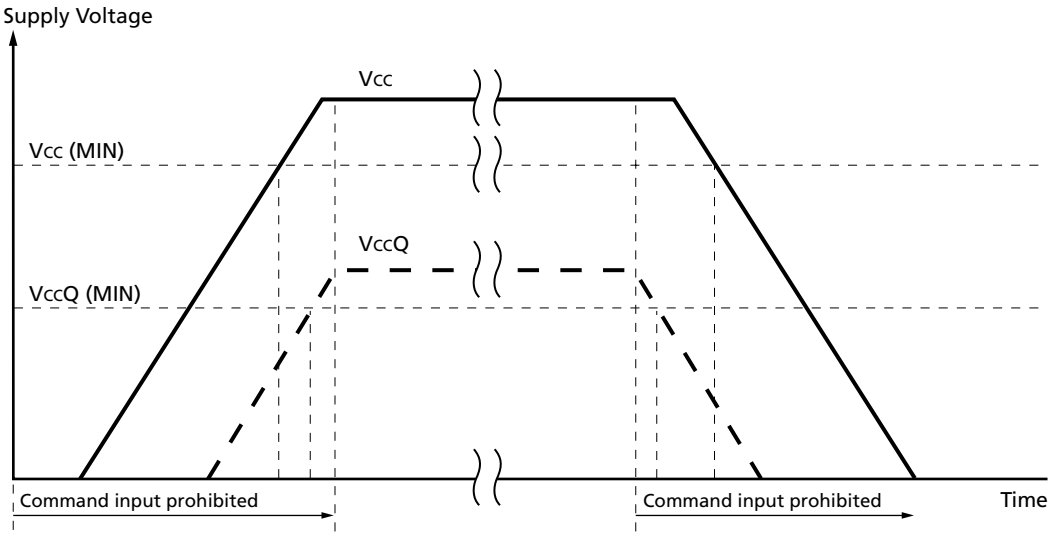
Vcc Power Cycling

High-Speed NAND Flash devices are designed to prevent data corruption during power transitions. Vcc is internally monitored. (The WP# signal supports additional hardware protection during power transitions.) When ramping VCC and VCCQ, use the following procedure to initialize the device:

1. Ramp VCC to 2.7–3.6V.
2. Ramp VCCQ to MIN-MAX no sooner than VCC. VCCQ and VCC may ramp at the same time.
3. The host must wait for R/B# to be valid and HIGH before issuing RESET (FFh) to any target (see Figure 26 on page 36). The R/B# signal becomes valid when:
   3a. 50µs has elapsed since the beginning the VCC ramp, and
   3b. 10µs has elapsed since VCC/VCCQ reached MIN.
4. If not monitoring R/B#, the host must wait at least 100µs after Vcc/VCCQ reaches MIN.
5. All of the targets on the device power on with the asynchronous interface active. Each NAND Flash LUN draws less than an average of 10mA (IST) measured over intervals of 1ms until the RESET (FFh) command is issued.
6. The RESET (FFh) command must be the first command issued to all targets (CE#s) after the NAND Flash device is powered on. Each target will be busy for a maximum of ^{t}POR after a RESET command is issued. The RESET busy time can be monitored by polling R/B# or issuing the READ STATUS (70h) command to poll the status register.
7. The device is now initialized and ready for normal operation.

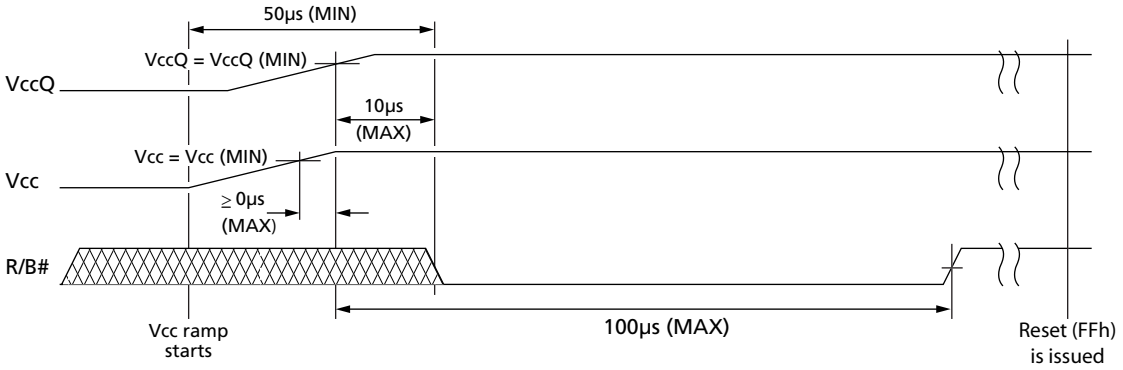
At power-down, VCCQ must go LOW, either before, or simultaneously with, VCC going LOW.

Figure 25: Power Cycle



Notes: 1. Vcc is exaggerated over VccQ in this figure for illustrative purposes.

Figure 26: R/B# Power-On Behavior



Activating Interfaces

After performing the steps under “Vcc Power Cycling” on page 35, the asynchronous interface is active for all targets on the device.

Each target's interface is independent of other targets, so the host is responsible for changing the interface for each target.

If the host and NAND Flash device, through error, are no longer using the same interface, then steps under "Activating the Asynchronous Interface" are performed to resynchronize the interfaces.

Activating the Asynchronous Interface

To activate the asynchronous NAND interface, the following steps are repeated for each target:

1. The host pulls CE# HIGH, disables its input to CLK, and enables its asynchronous interface.
2. The host pulls CE# LOW and issues the RESET (FFh) command, using an asynchronous command cycle.
3. R/B# goes LOW for ^{t}RST.
4. After ^{t}ITC, and during ^{t}RST, the device enters the asynchronous NAND interface. READ STATUS (70h) and SELECT LUN WITH STATUS (78h) are the only commands that can be issued.
5. After ^{t}RST, R/B# goes HIGH. TIMING MODE feature address (01h), sub-feature parameter P1 is set to 00h, indicating that the asynchronous NAND interface is active and that the device is set to timing mode 0.

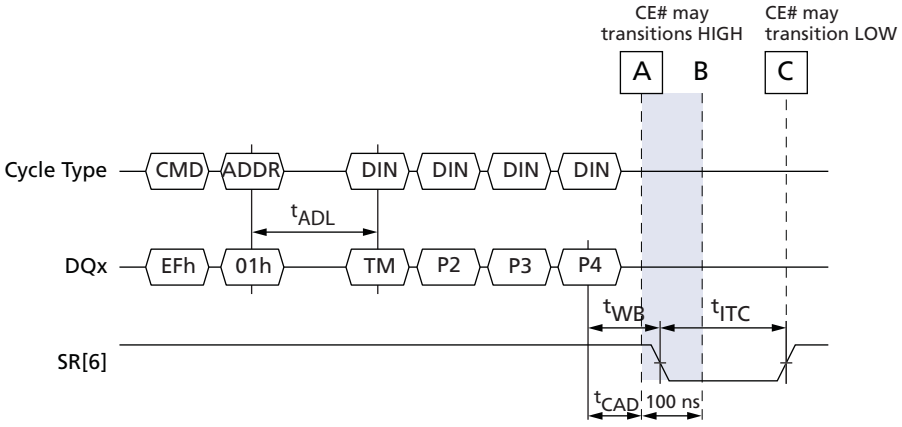
For further details, see “RESET (FFh)” on page 41.

Activating the Synchronous Interface

To activate the synchronous NAND Flash interface, the following steps are repeated for each target:

1. Issue the SET FEATURES (EFh) command.
2. Write address 01h, which selects the TIMING MODE.
3. Write P1 with 1Xh, where "X" is the timing mode used in the synchronous interface (see Table 10 on page 54).
4. Write P2–P4 as 00h-00h-00h.
5. R/B# goes LOW for ^{t}ITC. The host should pull CE# HIGH. During ^{t}ITC, the host should not issue any type of command, including status commands, to the NAND Flash device.
6. After ^{t}ITC, R/B# goes HIGH and the synchronous interface is enabled. Before pulling CE# LOW, the host should enable the clock.

Figure 27: Activating the Synchronous Interface



Notes: 1. TM = Timing mode.

Command Definitions

Table 5: Command Set

Command	Command Cycle #1	# Valid Address Cycles	Data Input Cycles	Command Cycle #2	Valid while Selected LUN is Busy[1]	Valid while Other LUNs are Busy[2]	Notes
RESET Operations							
RESET	FFh	0	—	—	Yes	Yes	
SYNCHRONOUS RESET	FCh	0	—	—	Yes	Yes	
Identification Operations							
READ ID	90h	1	—	—			3
READ PARAMETER PAGE	ECh	1	—	—			
READ UNIQUE ID	EDh	1	—	—			
Configuration Operations							
GET FEATURES	EEh	1	—	—			3
SET FEATURES	EFh	1	4	—			4
STATUS Operations							
READ STATUS	70h	0	—	—	Yes		
SELECT LUN WITH STATUS	78h	3	—	—	Yes	Yes	
Column Address Operations							
CHANGE READ COLUMN	05h	2	—	E0h		Yes	
SELECT CACHE REGISTER	06h	5	—	E0h		Yes	
CHANGE WRITE COLUMN	85h	2	Optional	—		Yes	
CHANGE ROW ADDRESS	85h	5	Optional	11h		Yes	8
READ Operations							
READ MODE	00h	0	—	—		Yes	
READ PAGE	00h	5	—	30h		Yes	5
READ PAGE MULTI-PLANE	00h	5	—	32h		Yes	
READ PAGE CACHE SEQUENTIAL	31h	0	—	—		Yes	6
READ PAGE CACHE RANDOM	00h	5	—	31h		Yes	5, 6
READ PAGE CACHE LAST	3Fh	0	—	—		Yes	6
PROGRAM Operations							
PROGRAM PAGE	80h	5	Yes	10h		Yes	
PROGRAM PAGE MULTI-PLANE	80h	5	Yes	11h		Yes	
PROGRAM PAGE CACHE	80h	5	Yes	15h		Yes	7
ERASE Operations							
ERASE BLOCK	60h	3	—	D0h		Yes	
ERASE BLOCK MULTI-PLANE	60h	3	—	D1h		Yes	
COPYBACK Operations							
COPYBACK READ	00h	5	—	35h		Yes	5
COPYBACK PROGRAM	85h	5	Optional	10h		Yes	

Table 5: Command Set (continued)

Command	Command Cycle #1	# Valid Address Cycles	Data Input Cycles	Command Cycle #2	Valid while Selected LUN is Busy[1]	Valid while Other LUNs are Busy[2]	Notes
COPYBACK PROGRAM MULTI-PLANE	85h	5	Optional	11h		Yes	

Notes:
1. Busy means RDY = "0".
2. These commands can be used for multi-LUN operations (see "Multi-LUN Operations" on page 86).
3. The READ ID (90h) and GET FEATURES (EEh) output identical data on rising and falling DQS edges.
4. The SET FEATURES (EFh) command requires data transition prior to the rising edge of CLK, with identical data for the rising and falling edges.
5. This command can be preceded by up to one READ PAGE MULTI-PLANE (00h-32h) command to accommodate a maximum simultaneous two-plane array operation.
6. Issuing a READ PAGE CACHE-series (31h, 00h-31h, 00h-32h, 3Fh) command when the array is busy (RDY = "1", ARDY = "0") is supported if the previous command was a READ PAGE (00h-30h) or READ PAGE CACHE-series command; otherwise it is prohibited.
7. Issuing a PROGRAM PAGE CACHE (80h-15h) command when the array is busy (RDY = "1", ARDY = "0") is supported if the previous command was a PROGRAM PAGE CACHE (80h-15h) command; otherwise it is prohibited.
8. Command cycle #2 of 11h is conditional. See "CHANGE ROW ADDRESS (85h)" for more details.

Reset Operations

RESET (FFh)

The RESET (FFh) command is used to put a target into a known condition and to abort command sequences in progress. This command is accepted by all LUNs, even when they are busy.

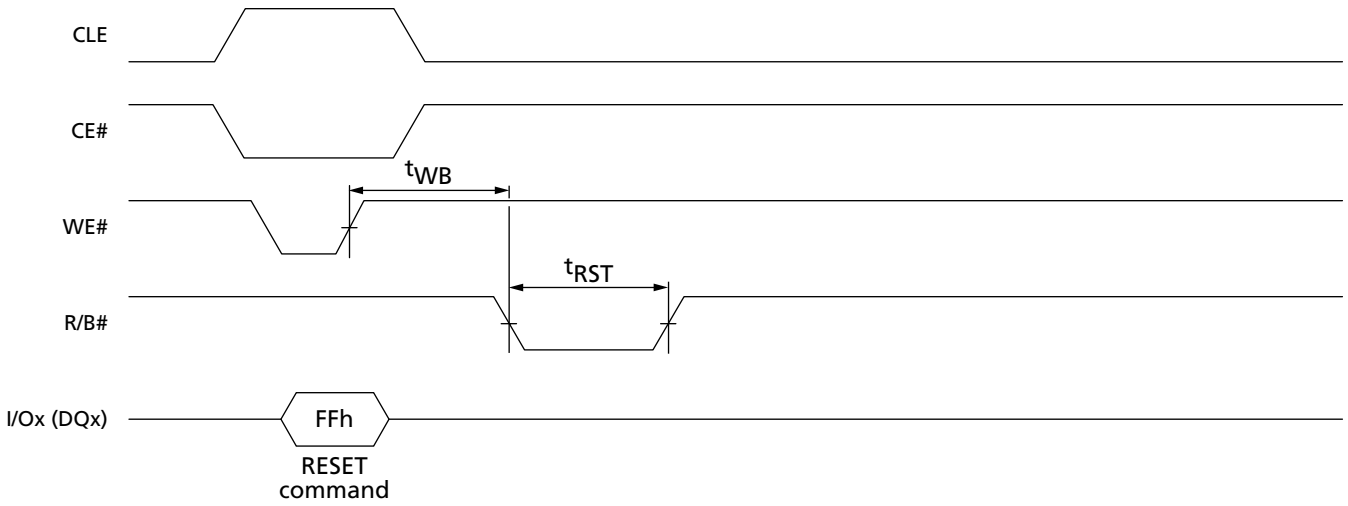
When FFh is written to the command register, the target goes busy for ^{t}RST. During ^{t}RST, the selected target (CE#) discontinues all array operations on all LUNs. All pending single-plane and multi-plane operations are cancelled. If this command is issued while a PROGRAM or ERASE operation is occurring on one or more LUNs, the data may be partially programmed or erased and is invalid. The command register is cleared and ready for the next command. The data register and cache register contents are invalid.

If the RESET (FFh) command is issued when the synchronous interface is enabled, the target's interface is changed to the asynchronous interface and the timing mode is set to "0". The RESET (FFh) command can be issued asynchronously when the synchronous interface is active, meaning that CLK does not need to be continuously running when CE# is transitioned LOW and FFh is latched on the rising edge of CLK. After this command is latched, the host should not issue any commands during ^{t}ITC. After ^{t}ITC, and during or after ^{t}RST, the host can poll each LUN's status register.

If the RESET (FFh) command is issued when the asynchronous interface is active, the target's asynchronous timing mode remains unchanged. During or after ^{t}RST, the host can poll each LUN's status register.

RESET must be issued as the first command to each target following power-up (see "Vcc Power Cycling" on page 35). Use of the SELECT LUN WITH STATUS (78h) command is prohibited during the power-on RESET. To determine when the target is ready, use READ STATUS (70h).

Figure 28: Asynchronous RESET (FFh) Cycle



SYNCHRONOUS RESET (FCh)

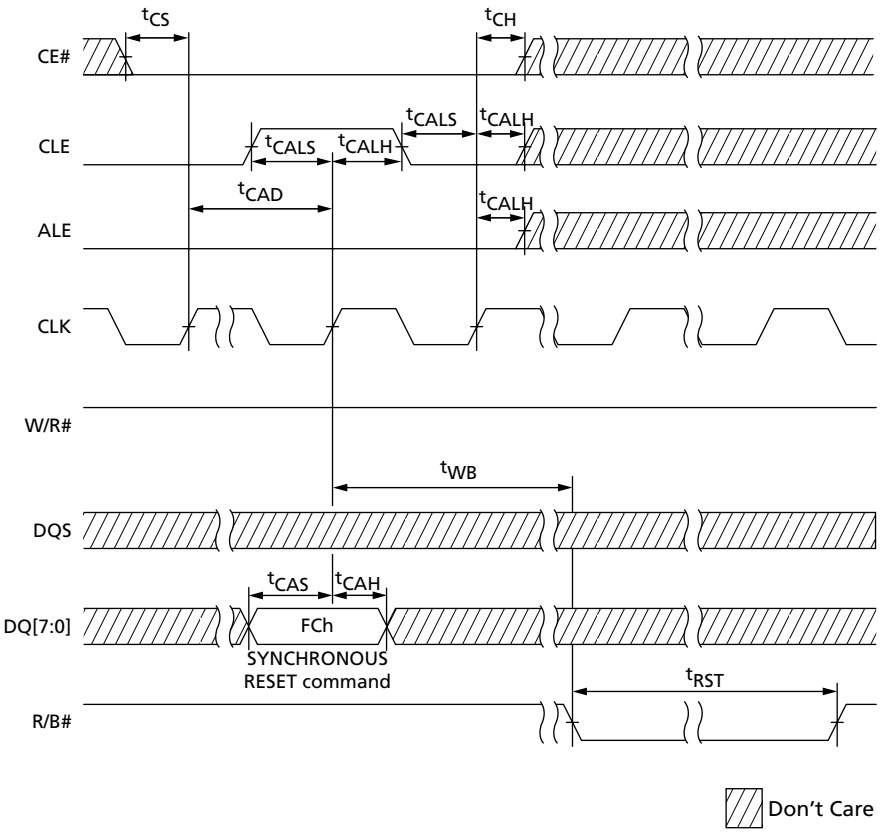
When the synchronous interface is active, the SYNCHRONOUS RESET (FCh) command is used to put a target into a known condition and to abort a command sequence in progress. This command is accepted by all LUNs, even when they are BUSY.

When FCh is written to the command register, the target goes busy for ^{t}RST. During ^{t}RST, the selected target (CE#) discontinues all array operations on all LUNs. All pending single-plane and multi-plane operations are cancelled. If this command is issued while a PROGRAM or ERASE operation is occurring on one or more LUNs, the data may be partially programmed or erased and is invalid. The command register is cleared and ready for the next command. The data register and cache register contents are invalid, and the synchronous interface remains active.

During or after ^{t}RST, the host can poll each LUN's status register.

SYNCHRONOUS RESET is only accepted while the synchronous interface is active. Its use is prohibited when the asynchronous interface is active.

Figure 29: SYNCHRONOUS RESET (FCh) Cycle



Identification Operations

READ ID (90h)

The READ ID (90h) command is used to read identifier codes programmed into the target. This command is accepted by the target only when all LUNs on the target are idle.

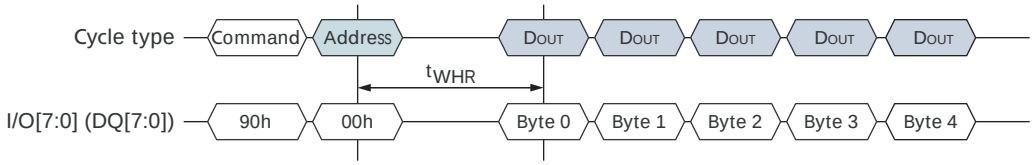
Writing 90h to the command register puts the target in read ID mode. The target stays in this mode until another valid command is issued.

When the 90h command is followed by an 00h address cycle, the target returns a 5-byte identifier code that includes the manufacturer's ID, device configuration, and part-specific information.

When the 90h command is followed by a 20h address cycle, the target returns the 4-byte ONFI identifier code.

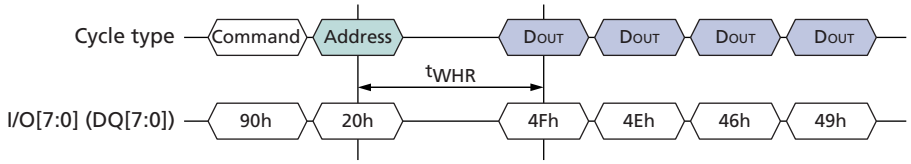
After the 90h and address cycle are written to the target, the host enables data output mode to read the identifier information. When the asynchronous interface is active, one data byte is output per RE# toggle. When the synchronous interface is active, one data byte is output per rising edge of DQS when ALE and CLE are HIGH; the data byte on the falling edge of DQS is identical to the data byte output on the previous rising edge of DQS.

Figure 30: READ ID (90h) with 00h Address Cycle Operation



Notes: 1. See Table 6 on page 43 for byte definitions.

Figure 31: READ ID (90h) with 20h Address Cycle Operation



Notes: 1. See Table 7 on page 44 for byte definitions.

Table 6: READ ID Parameters for Address 00h

	Options	I/O7 (DQ7)	I/O6 (DQ6)	I/O5 (DQ5)	I/O4 (DQ4)	I/O3 (DQ3)	I/O2 (DQ2)	I/O1 (DQ1)	I/O0 (DQ0)	Value	Notes
Byte 0 – Manufacturer ID											
Manufacturer	Micron	0	0	1	0	1	1	0	0	2Ch	1
Byte 1 – Device ID											
Vcc	3.3V					1	0	0	0		

Table 6: READ ID Parameters for Address 00h (continued)

	Options	I/O7 (DQ7)	I/O6 (DQ6)	I/O5 (DQ5)	I/O4 (DQ4)	I/O3 (DQ3)	I/O2 (DQ2)	I/O1 (DQ1)	I/O0 (DQ0)	Value	Notes
Density per CE#	8Gb	0	0	1	0						
Byte value	MT29F8G	0	0	1	0	1	0	0	0	28h	
Byte 2											
LUNs per CE#	1							0	0	00b	
Cell type	SLC					0	0			00b	
Reserved		0	0	0	0					0000b	
Byte value	MT29F8G	0	0	0	0	0	0	0	0	00h	
Byte 3											
Page size	4kB							1	0	10b	
Spare area size per 512B	28B					0	1			01b	
Pages per block	128		0	1	0					010b	
Multi-LUN operations	Not supported	0								0b	
	Supported	1								1b	
Byte value	MT29F8G	0	0	1	0	0	1	1	0	26h	
Byte 4											
Planes per LUN	2							0	1	01b	
Blocks per LUN	2,048				0	0	1			001b	
Timing mode: Asynchronous	4 (25ns)	1	0	0						100b	
Byte value	MT29F8G	1	0	0	0	0	1	0	1	85h	

Notes: 1. h = hexadecimal; b = binary

Table 7: READ ID Parameters for Address 20h

Byte	Options	I/O7 (DQ7)	I/O6 (DQ6)	I/O5 (DQ5)	I/O4 (DQ4)	I/O3 (DQ3)	I/O2 (DQ2)	I/O1 (DQ1)	I/O0 (DQ0)	Value	Notes
0	"O"	0	1	0	0	1	1	1	1	4Fh	1
1	"N"	0	1	0	0	1	1	1	0	4Eh	
2	"F"	0	1	0	0	0	1	1	0	46h	
3	"I"	0	1	0	0	1	0	0	1	49h	
4	Undefined	X	X	X	X	X	X	X	X	XXh	

Notes: 1. h = hexadecimal

READ PARAMETER PAGE (ECh)

The READ PARAMETER PAGE (ECh) command is used to read the ONFI parameter page programmed into the target. This command is accepted by the target only when all LUNs on the target are idle.

Writing ECh to the command register puts the target in read parameter page mode. The target stays in this mode until another valid command is issued.

When the ECh command is followed by an 00h address cycle, the target goes busy for ^{t}R. If the READ STATUS (70h) command is used to monitor for command completion, the READ MODE (00h) command must be used to re-enable data output mode. Use of the SELECT LUN WITH STATUS (78h) command is prohibited while the target is busy and during data output.

After ^{t}R completes, the host enables data output mode to read the parameter page. When the asynchronous interface is active, one data byte is output per RE# toggle. When the synchronous interface is active, one data byte is output for each rising or falling edge of DQS.

A minimum of seven copies of the parameter page are stored in the device. Each parameter page is 256 bytes. If desired, the CHANGE READ COLUMN (05h-E0h) command can be used to change the location of data output. Use of the SELECT CACHE REGISTER (06h-E0h) is prohibited.

Figure 32: READ PARAMETER PAGE (ECh) Operation

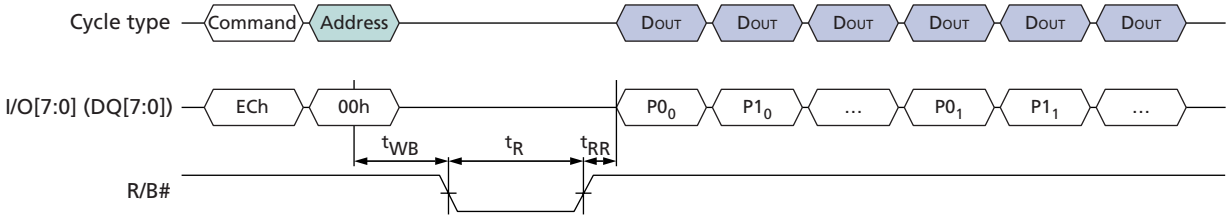


Table 8: Parameter Page Data Structure

Byte	Description	Device	Values
Revision information and features block			
0–3	Parameter page signature Byte 0: 4Fh, "O" Byte 1: 4Eh, "N" Byte 2: 46h, "F" Byte 3: 49h, "I"	–	4Fh, 4Eh, 46h, 49h
4–5	Revision number Bit[15:3]: Reserved (0) Bit 2: 1 = supports ONFI version 2.0 Bit 1: 1 = supports ONFI version 1.0 Bit 0: Reserved (0)	–	06h, 00h
6–7	Features supported Bit[15:6]: Reserved (0) Bit 5: 1 = supports synchronous interface Bit 4: 1 = supports odd-to-even page copyback Bit 3: 1 = supports interleaved (multi-plane) operations Bit 2: 1 = supports non-sequential page programming Bit 1: 1 = supports multiple LUN operations Bit 0: 1 = supports 16-bit data bus width	MT29F8G08CBABA	18h, 00h
		MT29F8G08CBCBB	38h, 00h
8–9	Optional commands supported Bit[15:6]: Reserved (0) Bit 5: 1 = supports READ UNIQUE ID Bit 4: 1 = supports INTERNAL DATA MOVE Bit 3: 1 = supports TWO-PLANE/MULTIPLE-DIE READ STATUS Bit 2: 1 = supports GET FEATURES and SET FEATURES Bit 1: 1 = supports read cache commands Bit 0: 1 = supports PROGRAM PAGE CACHE MODE command	–	3Fh, 00h
10–31	Reserved (0)	–	All 00h
Manufacturer information block			
32–43	Device manufacturer (12 ASCII characters) Micron	–	4Dh, 49h, 43h, 52h, 4Fh, 4Eh, 20h, 20h, 20h, 20h, 20h, 20h
44–63	Device model (20 ASCII characters) Note: For TSOP packaged devices with WP or WC package codes, only the WP package code will be referenced in the Read Parameter Page.	MT29F8G08ABABAWP	4Dh, 54h, 32h, 39h, 46h, 38h, 47h, 30h, 38h, 41h, 42h, 41h, 42h, 41h, 57h, 50h, 20h, 20h, 20h, 20h
		MT29F8G08ABCBBWP	4Dh, 54h, 32h, 39h, 46h, 38h, 47h, 30h, 38h, 41h, 42h, 43h, 42h, 42h, 57h, 50h, 20h, 20h, 20h, 20h
		MT29F8G08ABABAC3	4Dh, 54h, 32h, 39h, 46h, 38h, 47h, 30h, 38h, 41h, 42h, 41h, 42h, 41h, 43h, 32h, 20h, 20h, 20h, 20h
		MT29F8G08ABCBBH1	4Dh, 54h, 32h, 39h, 46h, 38h, 47h, 30h, 38h, 41h, 42h, 43h, 42h, 42h, 48h, 31h, 20h, 20h, 20h, 20h

Table 8: Parameter Page Data Structure (continued)

Byte	Description	Device	Values
64	JEDEC manufacturer ID	–	2Ch
65–66	Date code	–	00h, 00h
67–79	Reserved (0)	–	All 00h
Memory organization block			
80–83	Number of data bytes per page	–	00h, 10h, 00h, 00h
84–85	Number of spare bytes per page	–	E0h, 00h
86–89	Number of data bytes per partial page	–	00h, 02h, 00h, 00h
90–91	Number of spare bytes per partial page	–	1Ch, 00h
92–95	Number of pages per block	–	80h, 00h, 00h, 00h
96–99	Number of blocks per LUN	–	00h, 08h, 00h, 00h
100	Number of LUNs per chip enable	–	01h
101	Number of address cycles Bit[7:4]: Column address cycles Bit[3:0]: Row address cycles	–	23h
102	Number of bits per cell	–	01h
103–104	Bad blocks maximum per LUN	–	28h, 00h
105–106	Block endurance	–	01h, 05h
107	Guaranteed valid blocks at beginning of target	–	01h
108–109	Block endurance for guaranteed valid blocks	–	00h, 00h
110	Number of programs per page	–	04h
111	Partial programming attributes Bit[7:5]: Reserved Bit 4: 1 = partial page layout is partial page data followed by partial page spare Bits [3:1]: Reserved Bit 0: 1 = partial page programming has constraints	–	00h
112	Number of bits ECC correctability	–	04h
113	Number of interleaved address bits Bit[7:4]: Reserved (0) Bit[3:0]: Number of interleaved address bits	–	01h
114	Interleaved operation attributes Bit[7:4]: Reserved (0) Bit 3: Address restrictions for program cache Bit 2: 1 = program cache supported Bit 1: 1 = no block address restrictions Bit 0: Overlapped/concurrent interleaving support	–	0Eh
115–127	Reserved (0)	–	All 00h
Electrical parameters block			
128	I/O pin capacitance per chip enable	–	05h

Table 8: Parameter Page Data Structure (continued)

Byte	Description	Device	Values
129–130	Timing mode support Bit[15:6]: Reserved (0) Bit 5: 1 = supports timing mode 5 Bit 4: 1 = supports timing mode 4 Bit 3: 1 = supports timing mode 3 Bit 2: 1 = supports timing mode 2 Bit 1: 1 = supports timing mode 1 Bit 0: 1 = supports timing mode 0, shall be 1	–	1Fh, 00h
131–132	Program cache timing mode support Bit[15:6]: Reserved (0) Bit 5: 1 = supports timing mode 5 Bit 4: 1 = supports timing mode 4 Bit 3: 1 = supports timing mode 3 Bit 2: 1 = supports timing mode 2 Bit 1: 1 = supports timing mode 1 Bit 0: 1 = supports timing mode 0	–	1Fh, 00h
133–134	^{t}PROG Maximum PROGRAM PAGE time (µs)	–	F4h, 01h
135–136	^{t}BERS Maximum BLOCK ERASE time (µs)	–	B8h, 0Bh
137–138	^{t}R Maximum PAGE READ time (µs)	–	19h, 00h
139–140	^{t}CCS Minimum change column setup time (ns)	–	C8h, 00h
141–142	Source synchronous timing mode support Bit[15:5]: Reserved (0) Bit 4: 1 = supports timing mode 4 Bit 3: 1 = supports timing mode 3 Bit 2: 1 = supports timing mode 2 Bit 1: 1 = supports timing mode 1 Bit 0: 1 = supports timing mode 0	MT29F8G08ABABA	00h, 00h
		MT29F8G08ABCBB	1Fh, 00h
143	Source synchronous features Bit[7:2]: Reserved (0) Bit 1: 1 = typical capacitance values present Bit 0: 0 = use ^{t}CAD MIN value	MT29F8G08ABABA	00h
		MT29F8G08ABCBB	02h
144–145	CLK input pin capacitance per chip enable, typical	MT29F8G08ABABAWP	00h, 00h
		MT29F8G08ABABAC3	
		MT29F8G08ABCBBWP	3Fh, 00h
		MT29F8G08ABCBBH1	24h, 00h
146–147	I/O pin capacitance per chip enable, typical	MT29F8G08ABABAWP	00h, 00h
		MT29F8G08ABABAC3	
		MT29F8G08ABCBBWP	1Ch, 00h
		MT29F8G08ABCBBH1	2Dh, 00h
148–149	Input capacitance per chip enable, typical	MT29F8G08ABABAWP	00h, 00h
		MT29F8G08ABABAC3	
		MT29F8G08ABCBBWP	3Fh, 00h
		MT29F8G08ABCBBH1	28h, 00h
150	Input pin capacitance per chip enable, maximum	MT29F8G08ABABAWP	0Ah
		MT29F8G08ABABAC3	
		MT29F8G08ABCBBWP	
		MT29F8G08ABCBBH1	05h

Table 8: Parameter Page Data Structure (continued)

Byte	Description	Device	Values
151	Driver strength support Bit[7:3]: Reserved (0) Bit 2: 1 = Supports overdrive (2 drive strength) Bit 1: 1 = Supports overdrive (1 drive strength) Bit 0: 1 = Supports driver strength settings	–	07h
152-163	Reserved (0)	–	All 00h
Vendor block			
164–165	Vendor-specific revision number	–	01h, 00h
166	TWO-PLANE PAGE READ support Bit[7:1]: Reserved (0) Bit 0: 1 = Support for TWO-PLANE PAGE READ	–	01h
167	Read cache support Bit[7:1]: Reserved (0) Bit 0: 0 = Does not support Micron-specific read cache function	–	00h
168	READ UNIQUE ID support Bit[7:1]: Reserved (0) Bit 0: 0 = Does not support Micron-specific READ UNIQUE ID	–	00h
169	Programmable I/O drive strength support Bit[7:1]: Reserved (0) Bit 0: 0 = No support for programmable I/O drive strength by B8h command	–	00h
170	Number of programmable I/O drive strength settings Bit[7:3]: Reserved (0) Bit [2:0] = Number of programmable I/O drive strength settings	–	04h
171	Programmable I/O drive strength feature address Bit[7:0] = Programmable I/O drive strength feature address	–	10h
172	Programmable R/B# pull-down strength support Bit[7:1]: Reserved (0) Bit 0: 1 = Support programmable R/B# pull-down strength	–	01h
173	Programmable R/B# pull-down strength feature address Bit[7:0] = Feature address used with programmable R/B# pull-down strength	–	81h
174	Number of programmable R/B# pull-down strength settings Bit[7:3]: Reserved (0) Bit[2:0] = Number of programmable R/B# pull-down strength settings	–	04h
175	OTP mode support Bit[7:2]: Reserved (0) Bit 0: 0 = Does not support OTP mode Bit 1: 1 = Supports Get/Set Features command set Bit 0: 0 = Does not support A5h/A0h/AFh OTP command set	–	02h

Table 8: Parameter Page Data Structure (continued)

Byte	Description	Device	Values
176	OTP page start Bit[7:0] = Page where OTP page space begins	–	02h
177	OTP DATA PROTECT address Bit[7:0] = Page address to use when issuing OTP DATA PROTECT command	–	01h
178	Number of OTP pages Bit[15:4]: Reserved (0) Bit[3:0] = Number of OTP pages	–	1Eh
179	OTP Feature Address	–	90h
180–252	Reserved (0)	–	All 00h
253	Parameter page revision	–	01h
254–255	Integrity CRC	MT29F8G08ABABAWP	92h, 15h
		MT29F8G08ABABAC3	46h, 07h
		MT29F8G08ABCBBWP	A9h, 1Fh
		MT29F8G08ABCBBH1	A7h, 20h
Redundant parameter pages			
256–511	Value of bytes 0–255	–	See bytes 0–255
512–767	Value of bytes 0–255	–	See bytes 0–255
768–1,023	Value of bytes 0–255	–	See bytes 0–255
1,024–1,279	Value of bytes 0–255	–	See bytes 0–255
1,278–1,535	Value of bytes 0–255	–	See bytes 0–255
1,536–1,791	Value of bytes 0–255	–	See bytes 0–255
1,792–2,047	Value of bytes 0–255	–	See bytes 0–255
2,048–2,303	Value of bytes 0–255	–	See bytes 0–255
2,304–2,559	Value of bytes 0–255	–	See bytes 0–255
2,560–2,815	Value of bytes 0–255	–	See bytes 0–255
2,816–3,071	Value of bytes 0–255	–	See bytes 0–255
3,072–3,327	Value of bytes 0–255	–	See bytes 0–255
3,328–3,583	Value of bytes 0–255	–	See bytes 0–255
3,584–4,095	Value of bytes 0–255	–	See bytes 0–255
4,096–4,319	Reserved (FFh)	–	All FFh

READ UNIQUE ID (EDh)

The READ UNIQUE ID (EDh) command is used to read a unique identifier programmed into the target. This command is accepted by the target only when all LUNs on the target are idle.

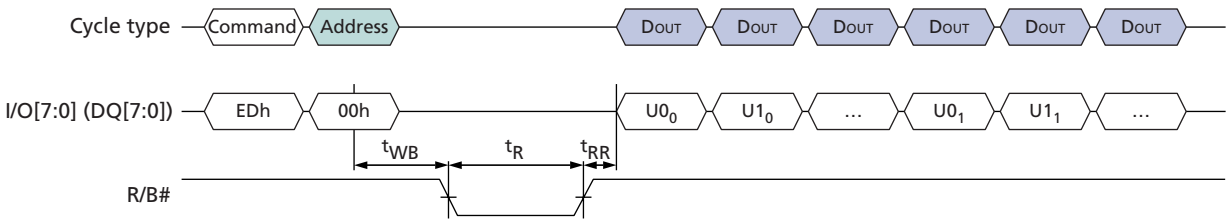
Writing EDh to the command register puts the target in read unique ID mode. The target stays in this mode until another valid command is issued.

When the EDh command is followed by an 00h address cycle, the target goes busy for ^{t}R. If the READ STATUS (70h) command is used to monitor for command completion, the READ MODE (00h) command must be used to re-enable data output mode.

After ^{t}R completes, the host enables data output mode to read the unique ID. When the asynchronous interface is active, one data byte is output per RE# toggle. When the synchronous interface is active, two data bytes are output, one byte for each rising or falling edge of DQS.

Sixteen copies of the unique ID data are stored in the device. Each copy is 32 bytes. The first 16 bytes of a 32-byte copy are unique data, and the second 16 bytes are the complement of the first 16 bytes. The host should XOR the first 16 bytes with the second 16 bytes. If the result is 16 bytes of FFh, then that copy of the unique ID data is correct. In the event that a non-FFh result is returned, the host can repeat the XOR operation on a subsequent copy of the unique ID data. If desired, the CHANGE READ COLUMN (05h-E0h) command can be used to change the data output location. Use of the SELECT CACHE REGISTER (06h-E0h) command is prohibited.

Figure 33: READ UNIQUE ID (EDh) Operation



Configuration Operations

The GET FEATURES (EEh) and SET FEATURES (EFh) commands are used to modify the target's default power-on behavior. These commands use a one-byte feature address to determine which sub-feature parameters will be read or modified. Each feature address (in the 00h to FFh range) is defined in Table 9. The GET FEATURES command reads the sub-feature parameters (P1-P4) at the specified feature address. The SET FEATURES (EFh) command writes sub-feature parameters (P1-P4) to the specified feature address.

Table 9: Feature Address Definitions

Feature Address	Definition
00h	Reserved
01h	Timing mode
02h–0Fh	Reserved
10h	Programmable output drive strength
11h–7Fh	Reserved
80h	Programmable output drive strength
81h	Programmable RB# pull-down strength
82h–8Fh	Reserved
90h	Array operation mode
91h–FFh	Reserved

SET FEATURES EFh

The SET FEATURES (EFh) command writes the sub-feature parameters (P1-P4) to the specified feature address to enable or disable target-specific features. This command is accepted by the target only when all LUNs on the target are idle.

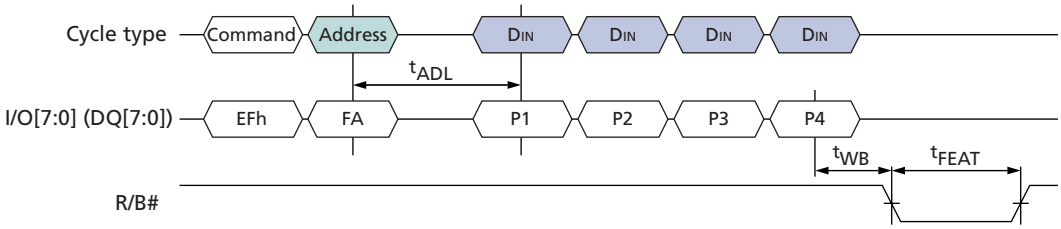
Writing EFh to the command register puts the target in the set features mode. The target stays in this mode until another command is issued.

The EFh command is followed by a valid feature address as specified in Table 9 on page 52. The host waits for ^{t}ADL before the sub-feature parameters are input. When the asynchronous interface is active, one sub-feature parameter is latched per rising edge of WE#. When the synchronous interface is active, one sub-feature parameter is latched per rising edge of DQS. The data on the falling edge of DQS should be identical to the sub-feature parameter input on the previous rising edge of DQS.

After all four sub-feature parameters are input, the target goes busy for ^{t}FEAT. The READ STATUS (70h) command can be used to monitor for command completion.

Feature address 01h (timing mode) operation is unique. If SET FEATURES is used to modify the interface type, the target will be busy for ^{t}ITC. See “Activating Interfaces” on page 37 for details.

Figure 34: SET FEATURES (EFh) Operation



GET FEATURES (EEh)

The GET FEATURES (EEh) command reads the sub-feature parameters (P1-P4) from the specified feature address. This command is accepted by the target only when all LUNs on the target are idle.

Writing EEh to the command register puts the target in get features mode. The target stays in this mode until another valid command is issued.

When the EEh command is followed by a feature address, the target goes busy for tFEAT. If the READ STATUS (70h) command is used to monitor for command completion, the READ MODE (00h) command must be used to re-enable data output mode. During and prior to data output, use of the SELECT LUN WITH STATUS (78h) command is prohibited prior to and during data output.

After tFEAT completes, the host enables data output mode to read the sub-feature parameters. When the asynchronous interface is active, one data byte is output per RE# toggle. When the synchronous interface is active, two data bytes are output per toggle, one byte for each rising or falling edge of DQS.

Figure 35: GET FEATURES (EEh) Operation

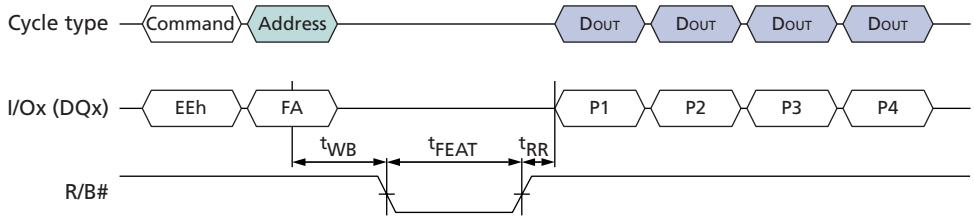


Table 10: Feature Address 01h: Timing Mode

Sub-Feature Parameter	Options	I/O7 (DQ7)	I/O6 (DQ6)	I/O5 (DQ5)	I/O4 (DQ4)	I/O3 (DQ3)	I/O2 (DQ2)	I/O1 (DQ1)	I/O0 (DQ0)	Value	Notes
P1											
Timing mode	Mode 0 (default)					0	0	0	0	x0h	1
	Mode 1					0	0	0	1	x1h	
	Mode 2					0	0	1	0	x2h	
	Mode 3					0	0	1	1	x3h	
	Mode 4					0	1	0	0	x4h	
Data interface	Asynchronous (default)			0	0					0xh	1
	Synchronous DDR			0	1					1xh	
	Reserved			1	x					2xh	
Reserved		0	0							00b	
P2											
Reserved		0	0	0	0	0	0	0	0	00h	
P3											
Reserved		0	0	0	0	0	0	0	0	00h	
P4											
Reserved		0	0	0	0	0	0	0	0	00h	

Notes: 1. Asynchronous timing mode 0 is the default, power-on value.

Table 11: Feature Addresses 10h and 80h: Programmable Output Drive Strength

Sub-Feature Parameter	Options	I/O7 (DQ7)	I/O6 (DQ6)	I/O5 (DQ5)	I/O4 (DQ4)	I/O3 (DQ3)	I/O2 (DQ2)	I/O1 (DQ1)	I/O0 (DQ0)	Value	Notes
P1											
Output drive strength	Overdrive 2							0	0	00h	1
	Overdrive 1							0	1	01h	
	Nominal (default)							1	0	02h	
	Underdrive							1	1	03h	
Reserved		0	0	0	0	0	0			00h	
P2											
Reserved		0	0	0	0	0	0	0	0	00h	
P3											
Reserved		0	0	0	0	0	0	0	0	00h	
P4											
Reserved		0	0	0	0	0	0	0	0	00h	

Notes: 1. See "Output Drive Strength" on page 89 for details.

Table 12: Feature Addresses 81h: Programmable R/B# Pull-Down Strength

Sub-Feature Parameter	Options	I/O7 (DQ7)	I/O6 (DQ6)	I/O5 (DQ5)	I/O4 (DQ4)	I/O3 (DQ3)	I/O2 (DQ2)	I/O1 (DQ1)	I/O0 (DQ0)	Value	Notes
P1											
R/B# pull-down strength	Full (default)							0	0	00h	1
	Three-quarter							0	1	01h	
	One-half							1	0	02h	
	One-quarter							1	1	03h	
Reserved		0	0	0	0	0	0			00h	
P2											
Reserved		0	0	0	0	0	0	0	0	00h	
P3											
Reserved		0	0	0	0	0	0	0	0	00h	
P4											
Reserved		0	0	0	0	0	0	0	0	00h	

Notes: 1. This feature address is used to change the default R/B# pull-down strength. Its strength should be selected based on the expected loading of R/B#. Full strength is the default, power-on value.

Table 13: Feature Addresses 90h: Array Operation Mode

Sub-Feature Parameter	Options	I/O7 (DQ7)	I/O6 (DQ6)	I/O5 (DQ5)	I/O4 (DQ4)	I/O3 (DQ3)	I/O2 (DQ2)	I/O1 (DQ1)	I/O0 (DQ0)	Value	Notes
P1											
Array Operation Mode	Normal (default)								0	00h	
	OTP Block								1	01h	1
Reserved		0	0	0	0	0	0	0		00h	
P2											
Reserved		0	0	0	0	0	0	0	0	00h	
P3											
Reserved		0	0	0	0	0	0	0	0	00h	
P4											
Reserved		0	0	0	0	0	0	0	0	00h	

Notes: 1. See "One-Time Programmable (OTP) Operations" on page 82 for details.

Status Operations

Each LUN provides its status independently of other LUNs on the same target through its 8-bit status register.

After the READ STATUS (70h) or SELECT LUN WITH STATUS (78h) command is issued, status register output is enabled. The contents of the status register are returned on I/O[7:0], DQ[7:0] for each data output request.

When the asynchronous interface is active and status register output is enabled, changes in the status register are seen on I/O[7:0], DQ[7:0] as long as CE# and RE# are LOW; it is not necessary to toggle RE# to see the status register update.

When the synchronous interface is active and status register output is enabled, changes in the status register are seen on I/O[7:0], DQ[7:0] as long as CE# and W/R# are LOW and ALE and CLE are HIGH. DQS also toggles while ALE and CLE are HIGH.

While monitoring the status register to determine when a data transfer from the Flash array to the data register (^{t}R) is complete, the host must issue the READ MODE (00h) command to disable the status register and enable data output (see READ MODE 00h on page 55).

The READ STATUS (70h) command returns the status of the most recently selected LUN. To prevent data contention during or following a multi-LUN operation, the host must enable only one LUN for status output by using the SELECT LUN WITH STATUS (78h) command (see “Multi-LUN Operations” on page 86).

Table 14: Status Register Definition

SR Bit	Definition	Independent per Plane[1]	Description
7	WP#	–	Write Protect: "0" = Protected "1" = Not protected In the normal array mode, this bit indicates the value of the WP# signal. In OTP mode this bit is set to "0" if a PROGRAM OTP PAGE operation is attempted and the OTP area is protected.
6	RDY	–	Ready/Busy I/O: "0" = Busy "1" = Ready This bit indicates that the selected LUN is not available to accept new commands, address, or data I/O cycles with the exception of RESET (FFh), SYNCHRONOUS RESET (FCh), READ STATUS (70h), and SELECT LUN WITH STATUS (78h). This bit applies only to the selected LUN.
5	ARDY	–	Ready/Busy Array: "0" = Busy "1" = Ready This bit goes LOW (busy) when an array operation is occurring on any plane of the selected LUN. It goes HIGH when all array operations on the selected LUN finish. This bit applies only to the selected LUN.
4	–	–	Reserved (0)
3	–	–	Reserved (0)
2	–	–	Reserved (0)

Table 14: Status Register Definition (continued)

SR Bit	Definition	Independent per Plane[1]	Description
1	FAILC	Yes	Pass/Fail (N-1): "0" = Pass "1" = Fail This bit is set if the previous operation on the selected LUN failed. This bit is valid only when RDY (SR bit 6) is "1." It applies to PROGRAM-, ERASE-, and COPYBACK PROGRAM-series operations (80h-10h, 80h-15h, 60h-D0h, 85h-10h). This bit is not valid following a READ-series operation.
0	FAIL	Yes	Pass/Fail (N): "0" = Pass "1" = Fail This bit is set if the most recently finished operation on the selected LUN failed. This bit is valid only when ARDY (SR bit 5) is "1." It applies to PROGRAM-, ERASE-, and COPYBACK PROGRAM-series operations (80h-10h, 80h-15h, 60h-D0h, 85h-10h). This bit is not valid following a READ-series operation.

Notes: 1. After a multi-plane operation begins, the FAILC and FAIL bits are ORed together for the active planes when the READ STATUS (70h) command is issued. After the SELECT LUN WITH STATUS (78h) command is issued, the FAILC and FAIL bits reflect the status of the plane selected.

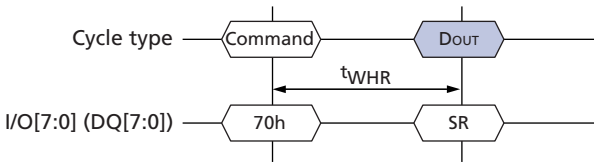
READ STATUS (70h)

The READ STATUS (70h) command returns the status of the last-selected LUN on a target. This command is accepted by the last-selected LUN even when it is busy (RDY = 0).

If there is only one LUN per target, the READ STATUS (70h) command can be used to return status following any NAND command.

In devices that have more than one LUN per target, during and following multi-LUN operations, the SELECT LUN WITH STATUS (78h) command must be used to select the LUN that should report status. In this situation, using the READ STATUS (70h) command will result in bus contention, as two or more LUNs could respond until the next operation is issued. The READ STATUS (70h) command can be used following all single-LUN operations.

Figure 36: READ STATUS (70h) Operation



SELECT LUN WITH STATUS (78h)

The SELECT LUN WITH STATUS (78h) command returns the status of the addressed LUN on a target even when it is busy (RDY = 0). This command is accepted by all LUNs, even when they are BUSY (RDY = 0).

Writing 78h to the command register, followed by three row address cycles containing the page, block, and LUN addresses, puts the selected LUN into read status mode

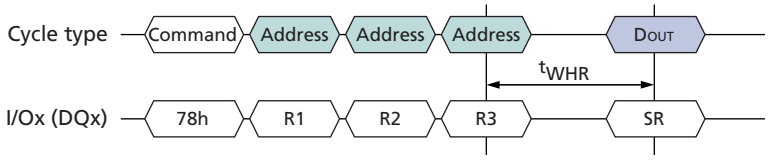
The selected LUN stays in this mode until another valid command is issued. LUNs that are not addressed are deselected to avoid bus contention.

The selected LUN's status is returned when the host requests data output. The RDY and ARDY bits of the status register are shared for all of the planes of the selected LUN. The FAILC and FAIL bits are specific to the plane specified in the row address.

The SELECT LUN WITH STATUS (78h) command also enables the selected LUN for data output. To begin data output following a READ-series operation after the selected LUN is ready (RDY = 1), issue the READ MODE (00h) command, then begin data output. If the host needs to change the cache register that will output data, use the SELECT CACHE REGISTER (06h-E0h) command after the LUN is ready (see "SELECT CACHE REGISTER (06h-E0h)" on page 59).

Use of the SELECT LUN WITH STATUS (78h) command is prohibited during the power-on RESET (FFh) command and when OTP mode is enabled. It is also prohibited following some of the other RESET, identification, and configuration operations. See individual operations for specific details.

Figure 37: SELECT LUN WITH STATUS (78h) Operation



Column Address Operations

The column address operations affect how data is input to and output from the cache registers within the target LUNs. These features provide host flexibility for managing data, especially when the host internal buffer is smaller than the number of data bytes or words in the cache register.

When the asynchronous interface is active, column address operations can address any byte in the selected cache register.

When the synchronous interface is active, column address operations are aligned to word boundaries (CA0 is forced to "0"), because as data is transferred on DQ[7:0] in two-byte units.

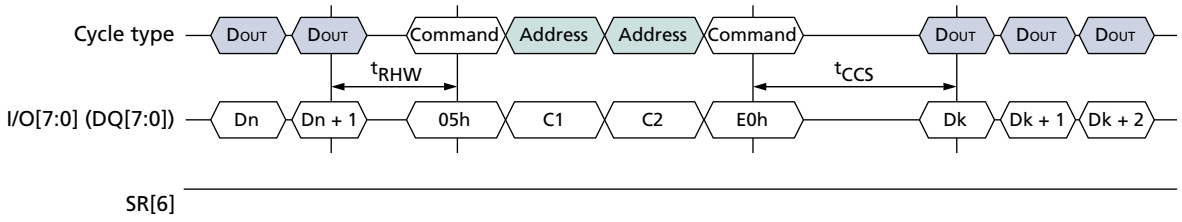
CHANGE READ COLUMN (05h-E0h)

The CHANGE READ COLUMN (05h-E0h) command changes the column address of the selected cache register and enables data output from the last selected LUN. This command is accepted by the selected LUN when it is ready (RDY = 1; ARDY = 1). It is also accepted by the selected LUN during CACHE READ operations (RDY = 1; ARDY = 0).

Writing 05h to the command register, followed by two column address cycles containing the column address, followed by the E0h command, puts the selected LUN into data output mode. After the E0h command cycle is issued, the host must wait at least ^{t}CCS before requesting data output. The selected LUN stays in data output mode until another valid command is issued.

In devices with more than one LUN per target, during and following multi-LUN operations, the SELECT LUN WITH STATUS (78h) command must be issued prior to issuing the CHANGE READ COLUMN (05h-E0h). In this situation, using the CHANGE READ COLUMN (05h-E0h) command without the SELECT LUN STATUS (78h) command will result in bus contention, as two or more LUNs could output data.

Figure 38: CHANGE READ COLUMN (05h–E0h) Operation



SELECT CACHE REGISTER (06h-E0h)

The SELECT CACHE REGISTER (06h-E0h) command enables data output on the addressed LUN's cache register at the specified column address. This command is accepted by a LUN when it is ready (RDY = 1; ARDY = 1).

Writing 06h to the command register, followed by two column address cycles and three row address cycles, followed by E0h, enables data output mode on the address LUN's cache register at the specified column address. After the E0h command cycle is issued, the host must wait at least ^{t}CCS before requesting data output. The selected LUN stays in data output mode until another valid command is issued.

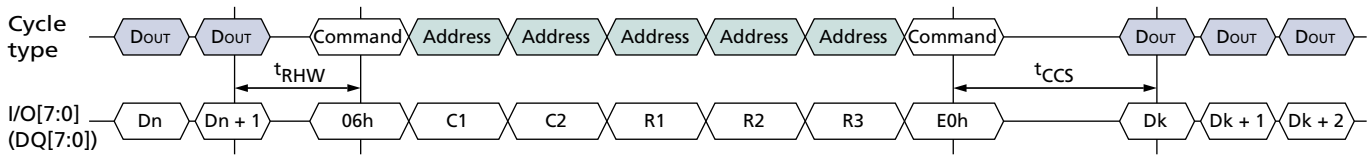
Following a multi-plane read page operation, the SELECT CACHE REGISTER (06h-E0h) command is used to select the cache register to be enabled for data output. After data output is complete on the selected plane, the command can be issued again to begin data output on another plane.

In devices with more than one LUN per target, after all of the LUNs on the target are ready (RDY = 1), the SELECT CACHE REGISTER (06h-E0h) command can be used following a multi-LUN read operation. LUNs that are not addressed are deselected to avoid bus contention.

In devices with more than one LUN per target, during multi-LUN operations where more than one or more LUNs are busy (RDY = 1; ARDY = 0 or RDY = 0; ARDY = 0), the SELECT LUN WITH STATUS (78h) command must be issued to the target LUN prior to issuing the SELECT CACHE REGISTER (06h-E0h). In this situation, using the SELECT CACHE REGISTER (06h-E0h) command without the SELECT LUN STATUS (78h) command will result in bus contention, as two or more LUNs could output data.

If there is a need to update the column address without selecting a new cache register or LUN, the CHANGE READ COLUMN (05h-E0h) command can be used instead.

Figure 39: SELECT CACHE REGISTER (06h–E0h) Operation



CHANGE WRITE COLUMN (85h)

The CHANGE WRITE COLUMN (85h) command changes the column address of the selected cache register and enables data input on the last-selected LUN. This command is accepted by the selected LUN when it is ready (RDY = 1; ARDY = 1). It is also accepted by the selected LUN during cache program operations (RDY = 1; ARDY = 0).

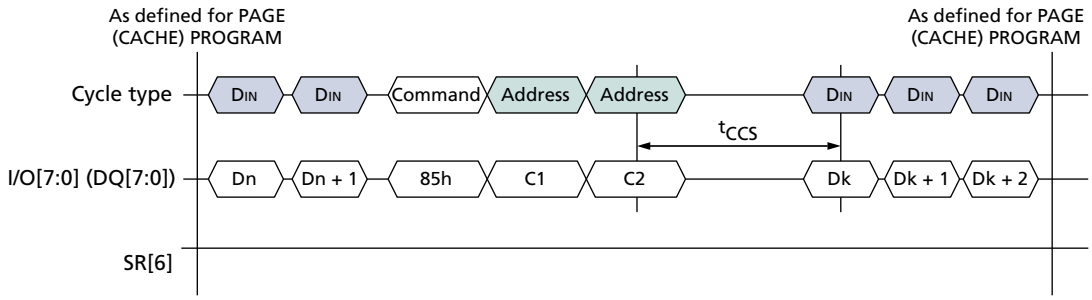
Writing 85h to the command register, followed by two column address cycles containing the column address, puts the selected LUN into data input mode. After the second address cycle is issued, the host must wait at least ^{t}CCS before inputting data. The selected LUN stays in data input mode until another valid command is issued. Though data input mode is enabled, data input from the host is optional. Data input begins at the column address specified.

The CHANGE WRITE COLUMN (85h) command is supported prior to the final command cycle (10h, 11h, 15h) of the following commands:

- PROGRAM PAGE (80h-10h)
- PROGRAM PAGE MULTI-PLANE (80h-11h)
- PROGRAM PAGE CACHE (80h-15h)
- COPYBACK PROGRAM (85h-10h)
- COPYBACK PROGRAM MULTI-PLANE (85h-11h)

In devices that have more than one LUN per target, the CHANGE WRITE COLUMN (85h) command can be used with other commands that support multi-LUN operations.

Figure 40: CHANGE WRITE COLUMN (85h) Operation



CHANGE ROW ADDRESS (85h)

The CHANGE ROW ADDRESS (85h) command changes the row address (block and page) where the cache register contents will be programmed in the NAND Flash array. It also changes the column address of the selected cache register and enables data input on the specified LUN. This command is accepted by the selected LUN when it is ready (RDY = 1; ARDY = 1). It is also accepted by the selected LUN during cache programming operations (RDY = 1; ARDY = 0).

Writing 85h to the command register, then writing two column address cycles and three row address cycles, updates the page and block destination of the selected plane for the addressed LUN, and puts the cache register into data input mode. After the fifth address cycle is issued, the host must wait at least ^{t}CCS before inputting data. The selected LUN stays in data-input mode until another valid command is issued. Though data-input mode is enabled, data input from the host is optional. Data input begins at the column address specified.

The CHANGE ROW ADDRESS (85h) command is supported prior to the final command cycle (10h, 11h, 15h) of the following commands[1]:

- PROGRAM PAGE (80h-10h)
- PROGRAM PAGE MULTI-PLANE (80h-11h)
- PROGRAM PAGE CACHE (80h-15h)
- COPYBACK PROGRAM (85h-10h)
- COPYBACK PROGRAM MULTI-PLANE (85h-11h).

Notes: **1.** When used with these commands, the LUN address and plane-select bits must be identical to the LUN address and plane-select bits originally specified.

The CHANGE ROW ADDRESS (85h) command enables the host to modify the original page and block address for the data in the cache register to a new page and block address.

The CHANGE ROW ADDRESS (85h) command can be used with the CHANGE READ COLUMN (05h-E0h) or CHANGE READ COLUMN ENHANCED (06h-E0h) commands to read and modify cache register contents in small sections prior to programming cache register contents to the NAND Flash array. This capability can reduce the amount of buffer memory used in the host controller.

To modify the cache register contents in small sections, first issue a PAGE READ (00h-30h) or COPYBACK READ (00h-35h) operation. When data output is enabled, the host can output a portion of the cache register contents. To modify the cache register contents, issue the 85h command, the column and row addresses, and input the new

data. The host can re-enable data output by issuing the 11h command, waiting ^{t}DBSY, and then issuing the CHANGE READ COLUMN (05h-E0h) or CHANGE READ COLUMN ENHANCED (06h-E0h) command. It is possible toggle between data output and data input multiple times. After the final CHANGE ROW ADDRESS (85h) operation is complete, issue the 10h command to program the cache register to the NAND Flash array.

In devices that have more than one LUN per target, the CHANGE ROW ADDRESS (85h) command can be used with other commands that support multi-LUN operations.

READ Operations

READ operations are used to copy data from the NAND Flash array of one or more of the planes to their respective cache registers, and to enable data output from the cache registers to the host through the DQ bus.

READ Operations

The READ PAGE (00h-30h) command, when issued by itself, reads one page from the NAND Flash array to its cache register and enables data output for that cache register.

During data output the following commands can be used to read and modify the data in the cache registers: CHANGE READ COLUMN (05h-E0h), CHANGE ROW ADDRESS (85h).

READ MULTI-PLANE Operations

READ MULTI-PLANE PAGE operations improve data throughput by copying data from multiple planes to the specified cache registers simultaneously. This is done by prepending one or more READ PAGE MULTI-PLANE (00h-32h) commands in front of the READ PAGE (00h-30h) command.

When the LUN is ready, the SELECT CACHE REGISTER (06h-E0h) command determines which plane outputs data. During data output the following commands can be used to read and modify the data in the cache registers: CHANGE READ COLUMN (05h-E0h), CHANGE ROW ADDRESS (85h).

See “Multi-Plane Operations” on page 86 for details.

READ PAGE CACHE Operations

For the highest sustainable level of data throughput, the READ PAGE CACHE-series (31h, 00h-31h) commands can be used to output data from the cache register while concurrently copying a page from the NAND Flash array to the data register.

A READ PAGE CACHE command sequence is started when the READ PAGE (00h-30h) command is used to read a page from the NAND Flash array to its corresponding cache register. R/B# goes LOW during ^{t}R and the selected LUN is busy (RDY = 0, ARDY = 0). After ^{t}R (R/B# is HIGH and RDY = 1, ARDY = 1), either of the following commands can be issued:

- READ PAGE CACHE SEQUENTIAL (31h)—starts copying the next sequential page from the NAND Flash array to the data register.
- READ PAGE CACHE RANDOM (00h-31h)—starts copying the page specified in this command from the NAND Flash array (any plane) to its corresponding data register.

After the READ PAGE CACHE-series (31h, 00h-31h) command has been issued, R/B# goes LOW on the target, RDY = 0 and ARDY = 0 on the LUN for ^{t}RCBSY, and the next page begins copying data from the array to the data register. After ^{t}RCBSY, R/B# goes HIGH and the LUN’s status register bits indicate the device is busy with a cache operation (RDY

= 1, ARDY = 0). The cache register becomes available and the page requested in the READ PAGE CACHE operation is transferred to the data register. At this point, data can be output from the cache register, beginning at column address 0. The CHANGE READ COLUMN (05h-E0h) command can be used to change the column address of the data output by the LUN.

After outputting the desired number of bytes from the cache register, either an additional READ PAGE CACHE-series (31h, 00h-31h) operation can be started or the READ PAGE CACHE LAST (3Fh) command can be issued.

If an additional READ PAGE CACHE-series (31h, 00h-31h) command is issued, R/B# goes LOW on the target, RDY = 0 and ARDY = 0 on the LUN for ^{t}RCBSY, the data register is copied to the cache register, then the next page begins copying into the data register. After ^{t}RCBSY, R/B# goes HIGH, RDY = 1 and ARDY = 0, indicating that the cache register is available for data output and that the specified page is copying from the NAND Flash array to the data register. Data can then be output from the cache register, beginning at column address 0. The CHANGE READ COLUMN (05h-E0h) command can be used to change the column address of the data being output by the cache register.

If the READ PAGE CACHE LAST (3Fh) command is issued, R/B# goes LOW on the target, RDY = 0 and ARDY = 0 on the LUN for ^{t}RCBSY, and the data register is copied into the cache register. After ^{t}RCBSY, R/B# goes HIGH, RDY = 1 and ARDY = 1, indicating that the cache register is available and that the LUN is ready. Data can then be output from the cache register, beginning at column address 0. The CHANGE READ COLUMN (05h-E0h) command can be used to change the column address of the data being output.

For READ PAGE CACHE-series (31h, 00h-31h, 3Fh), during the LUN busy time, ^{t}RCBSY, when RDY = 0 and ARDY = 0, the only valid commands are status operations (70h, 78h) and RESET (FFh, FCh). When RDY = 1 and ARDY = 0, the only valid commands during READ PAGE CACHE-series (31h, 00h-31h) operations are status operations (70h, 78h), READ MODE (00h), READ PAGE CACHE-series (31h, 00h-31h), CHANGE READ COLUMN (05h-E0h), and RESET (FFh, FCh).

PAGE READ MULTI-PLANE Operations Using Cache Operations

PAGE READ MULTI-PLANE Operations Using Cache improve data throughput by copying data from multiple planes to the specified cache registers simultaneously then queuing additional planes to be read from the NAND array while the pervious data read from the NAND array is outputted. This is done by prepending READ PAGE MULTI-PLANE (00h-32h) commands in front of the PAGE READ CACHE RANDOM (00h-31h) command.

When the LUN is ready, the SELECT CACHE REGSITER (06h-E0h) command determines which plane outputs data. During data output the following commands can be used to read and modify the data in the cache registers: CHANGE READ COLUMN (05h-E0h), CHANGE ROW ADDRESS (85h).

See “Multi-Plane Operations” on page 86 for additional multi-plane addressing requirements.

READ MODE (00h)

The READ MODE (00h) command disables status output, and enables data output for the last-selected LUN and cache register, after a READ operation (00h-30h, 00h-35h) has been monitored with a STATUS operation (70h, 78h). This command is accepted by the LUN when it is ready (RDY = 1, ARDY = 1). It is also accepted by the LUN during READ PAGE CACHE (31h, 3F, 00h-31h) operations (RDY = 1 and ARDY = 0).

In devices that have more than one LUN per target, during and following multi-LUN operations, the SELECT LUN WITH STATUS (78h) command must be used to select only one LUN prior to issuing the READ MODE (00h) command. This prevents bus contention.

READ PAGE (00h–30h)

The READ PAGE (00h–30h) command copies a page from the NAND Flash array to its respective cache register and enables data output. This command is accepted by the LUN when it is ready (RDY = 1, ARDY = 1).

A page from the NAND Flash array is read when the following sequence is performed:

1. The 00h command is written to the command register.
2. Five address cycles are written to the address registers.
3. A READ PAGE (30h) command is issued.
4. The selected LUN goes busy (RDY = 0, ARDY = 0) for ^{t}R as data is transferred.

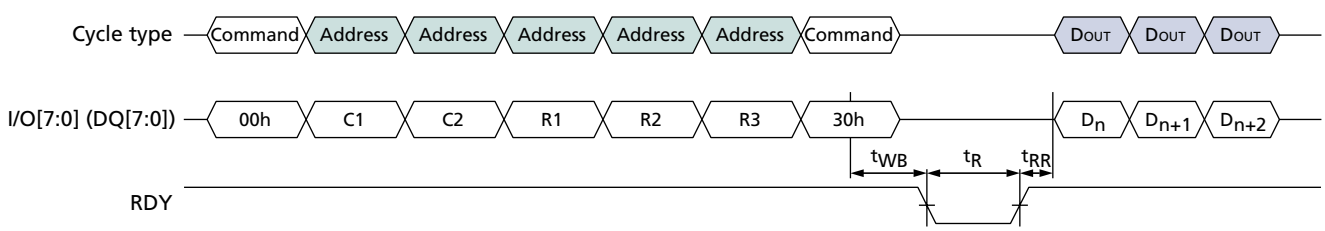
To determine the progress of the data transfer, the host can monitor the target's R/B# signal, or alternatively, the status operations (70h, 78h) can be used. If the status operations are used to monitor the LUN's status, when the LUN is ready (RDY = 1, ARDY = 1), the host disables status output and enables data output by issuing the READ MODE (00h) command. When the host requests data output, output begins at the column address specified.

During data output the following commands can be used to read and modify the data in the cache registers: CHANGE READ COLUMN (05h-E0h), CHANGE ROW ADDRESS (85h).

In devices that have more than one LUN per target, during and following multi-LUN operations the SELECT LUN WITH STATUS (78h) command must be used to select only one LUN prior to the issue of the READ MODE (00h) command. This prevents bus contention.

The READ PAGE (00h-30h) command is used as the final command of a multi-plane read operation. It is preceded by one or more READ PAGE MULTI-PLANE (00h-32h) commands. Data is transferred from the NAND Flash array for all of the addressed planes to their respective cache registers. When the LUN is ready (RDY = 1, ARDY = 1), data output is enabled for the cache register linked to the plane addressed in the READ PAGE (00h-30h) command. When the host requests data output, output begins at the column address last specified in the READ PAGE (00h-30h) command. The SELECT CACHE REGISTER (06h-E0h) command is used to enable data output in the other cache registers. See “Multi-Plane Addressing” on page 86 for additional multi-plane addressing requirements.

Figure 41: READ PAGE (00h–30h) Operation



READ PAGE CACHE SEQUENTIAL (31h)

The READ PAGE CACHE SEQUENTIAL (31h) command reads the next page in sequence within a block into the data register, while the previous page is output from the cache register. This command is accepted by the LUN when it is ready (RDY = 1, ARDY = 1). It is also accepted by the LUN during READ PAGE CACHE (31h, 00h-31h) operations (RDY = 1 and ARDY = 0).

This command is issued when 31h is written to the command register. After the command is issued, the following sequence occurs:

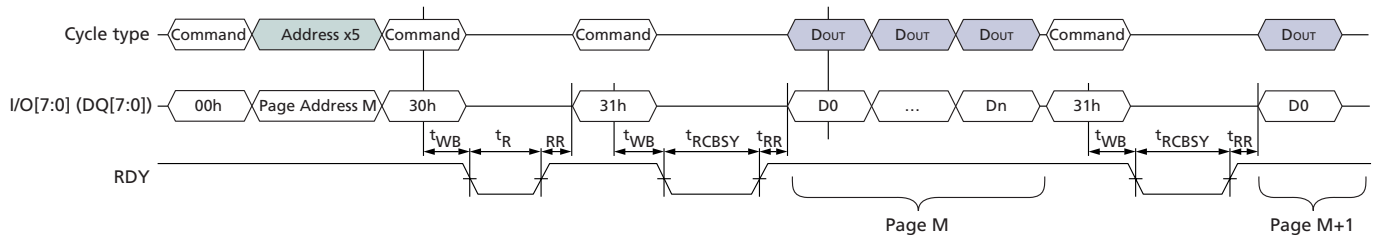
1. R/B# goes LOW and the LUN is busy (RDY = 0, ARDY = 0) for ^{t}RCBSY.
2. R/B# goes HIGH and the LUN is busy with a cache operation (RDY = 1, ARDY = 0), indicating that the cache register is available and that the specified page is copying from the NAND Flash array to the data register.
3. Data can be output from the cache register, beginning at column address 0. The CHANGE READ COLUMN (05h-E0h) command can be used to change the column address of the data being output from the cache register.

Caution The READ PAGE CACHE SEQUENTIAL (31h) command can be used to cross block boundaries. If the READ PAGE CACHE SEQUENTIAL (31h) command is issued after the last page of a block is read into the data register, the next page read will be the next logical block in the plane which the 31h command was issued. Do no issue the READ PAGE CACHE SEQUENTIAL (31h) command to cross LUN boundaries. Instead issue the READ PAGE CACHE LAST (3Fh) command for the last page of a LUN.

In devices that have more than one LUN per target, during and following multi-LUN operations, this sequence is followed to select only one LUN and prevent bus contention:

1. The SELECT LUN WITH STATUS (78h) command is issued.
2. The READ MODE (00h) command is issued.

Figure 42: READ PAGE CACHE SEQUENTIAL (31h) Operation



READ PAGE CACHE RANDOM (00h–31h)

The READ PAGE CACHE RANDOM (00h-31h) command reads the specified block and page into the data register while the previous page is output from the cache register. This command is accepted by the LUN when it is ready (RDY = 1, ARDY = 1). It is also accepted by the LUN during READ PAGE CACHE (31h, 00h-31h) operations (RDY = 1, ARDY = 0).

This command is issued in the following sequence:

1. 00h is written to the command register.
2. Five address cycles are written to the address register.
3. 31h is written to the command register.

The LUN address must match the same LUN address as the previous READ PAGE (00h-31h) command or, if applicable, the previous READ PAGE CACHE RANDOM (00h-31h) command. There is no restriction on the plane address.

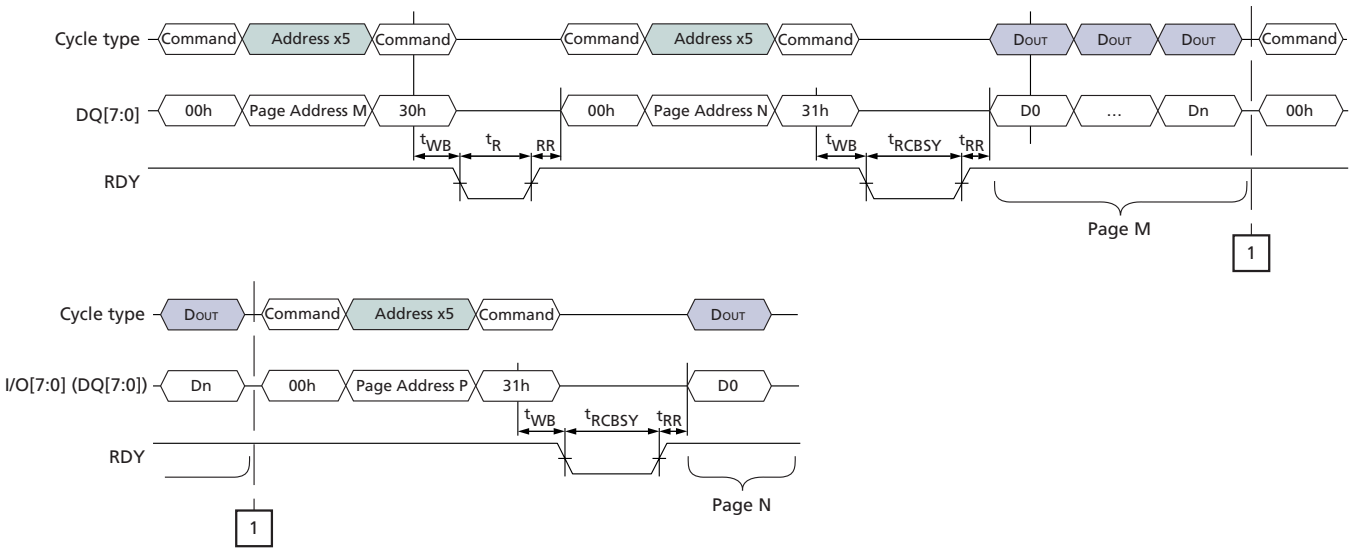
After this command is issued, the following sequence occurs:

1. R/B# goes LOW and the LUN is busy (RDY = 0, ARDY = 0) for ^{t}RCBSY.
2. R/B# goes HIGH and the LUN is busy with a cache operation (RDY = 1, ARDY = 0), indicating that the cache register is available and that the specified page is copying from the NAND Flash array to the data register.
3. Data can be output from the cache register beginning at column address 0. The CHANGE READ COLUMN (05h-E0h) command can be used to change the column address of the data being output from the cache register.

In devices that have more than one LUN per target, during and following multi-LUN operations, this sequence is followed to select only one LUN and prevent bus contention:

1. The SELECT LUN WITH STATUS (78h) command is issued.
2. The READ MODE (00h) command is issued.

Figure 43: READ PAGE CACHE RANDOM (00h–31h) Operation



READ PAGE CACHE LAST (3Fh)

The READ PAGE CACHE LAST (3Fh) command ends the READ PAGE CACHE sequence and copies a page from the data register to the cache register. This command is accepted by the LUN when it is ready (RDY = 1, ARDY = 1). It is also accepted by the LUN during READ PAGE CACHE (31h, 00h-31h) operations (RDY = 1, ARDY = 0).

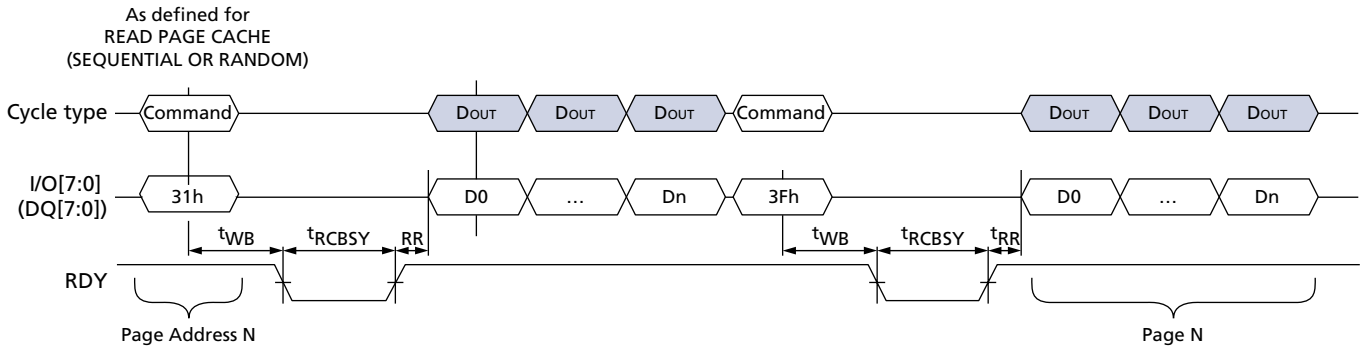
This command is issued when 3Fh is written to the command register. After the command is issued, the following sequence occurs:

1. R/B# goes LOW and the LUN is busy (RDY = 0, ARDY = 0) for ^{t}RCBSY.
2. R/B# goes HIGH and the LUN is ready (RDY = 1, ARDY = 1).
3. Data can be output from the cache register beginning at column address 0. The CHANGE READ COLUMN (05h-E0h) command can be used to change the column address of the data being output from the cache register.

In devices that have more than one LUN per target, during and following multi-LUN operations, this sequence is followed to select only one LUN and prevent bus contention:

1. The SELECT LUN WITH STATUS (78h) command is issued.
2. The READ MODE (00h) command is issued.

Figure 44: READ PAGE CACHE LAST (3Fh) Operation



PAGE READ MULTI-PLANE (00h-32h) using Cache

The READ PAGE MULTI-PLANE (00h-32h) can be used to setup multi-plane cache read operations. The READ PAGE MULTI-PLANE (00h-32h) command queues a plane to transfer data from the NAND flash array to its cache register. This command can be issued one or more times. Each time a new plane address is specified, that pane is also queued for data transfer. The command is issued to select the final plane and to begin the read operation for all previously queued planes.

This command is issued in the following sequence:

1. 00h is written to the command register.
2. Five address cycles are written to the address register.
3. 32h is written to the command register. (The column address in the address specified is ignored.)

After this command is issued, the following sequence occurs:

1. R/B# goes LOW and the LUN is busy (RDY = 0, ARDY = 0) for ^{t}DBSY.

Note: During ^{t}DBSY, the only valid commands during READ PAGE MULTI-PLANE (00h-32h) are status operations (70h, 78h) and reset commands (FFh, FCh). Following ^{t}DBSY, to continue the multi-plane read operation, the only valid commands are status operations (70h, 78h), READ PAGE MULTI-PLANE (00h-32h), and READ PAGE (00h-30h).

2. R/B# goes HIGH and the LUN is ready (RDY = 1, ARDY = 1).
3. The LUN and block are queued for data transfer from the array to the cache register for the addressed plane.

Note: Additional READ PAGE MULTI-PLANE (00h-32h) commands can be issued to queue additional planes for data transfer.

4. The READ PAGE (00h-30h) command is issued.
5. Data is transferred from the NAND Flash array for all of the addressed planes to their respective cache registers.
6. When the LUN is ready (RDY = 1, ARDY = 1), data output is enabled for the cache register linked to the even plane.
7. When the host requests data output, it begins at the column address specified in the READ PAGE (00h-30h) command.

Note: To enable data output in the other cache registers, the SELECT CACHE REGISTER (06h-E0h) command can be issued. Also, to change the column address within the currently selected plane, the CHANGE READ COLUMN (05h-E0h) command can be issued.

After the first sequence of READ PAGE MULTI-PLANE (00h-32h) and READ PAGE (00h-30h) has been issued to the NAND device addition cache read commands can be issued to the NAND device. To begin cache read operations to other blocks before outputting data from the previous read operations, there are two options.

The first option is to begin issuing the READ PAGE CACHE SEQUENTIAL (31h) command. Issuing the READ PAGE CACHE SEQUENTIAL (31h) command will cause the next consecutive page within each block for each plane that was addressed in steps 1 - 7 to be read. In the case issuing the READ PAGE CACHE SEQUENTIAL (31h) after the last page in a block has already been addressed, the first page in the next sequential block in that plane will be the next page read.

The following shows this sequence:

8. The READ PAGE CACHE SEQUNTIAL (31h) is issued.
9. R/B# goes LOW and the LUN is busy (RDY = 0, ARDY = 0) for ^{t}RCBSY

After R/B# goes HIGH and the LUN reports in the status register RDY = 1 and ARDY = 0, that signals that the internal array read is ongoing and the cache register is ready to output data from the previous read operation. When a READ PAGE CACHE SEQUENTIAL (31h) command is issued the column address defaults to 0.

Steps 8 and 9 can be repeated to continue reading consecutive pages. After issuing the last page address to be read, issue the READ PAGE CACHE LAST (3Fh) to finish the cache reading operation.

After R/B# goes HIGH and the LUN reports in the status register RDY = 1 and ARDY = 0, that signals that the internal array read is ongoing and the cache register is ready to output data from the previous read operation. The SELECT CACHE REGISTER (06h-E0h) command is required prior to outputting data. After the SELECT CACHE REGISTER (06h-E0h) command is issued, the CHANGE READ COLUMN (05h-E0h) command can also be issued.

Note: To enable data output in the other cache register or change the column address, the SELECT CACHE REGISTER (06h-E0h) command can be issued. Also, to change the column address within the currently selected plane (after the SELECT CACHE REGISTER (06h-E0h) command is issued), the CHANGE READ COLUMN (05h-E0h) command can be issued.

The second option is to issue the READ PAGE MULTI-PLANE (00h-32h) command followed by the READ PAGE CACHE RANDOM (00h-31h) command. By using READ PAGE MULTI-PLANE (00h-32h) command and the READ PAGE CACHE RANDOM (00h-31h) random page addresses within the NAND device can be selected instead of just the next sequential page address as with the READ PAGE CACHE SEQUENTIAL (31h) command. The column address with the READ PAGE MULTI-PLANE is ignored, data will come from byte 0 of subsequent pages read.

The following shows this sequence:

1. The READ PAGE MULTI-PLANE (00h-32) is issued. The column address in the address specified is ignored.
2. R/B# goes LOW and the LUN is busy (RDY = 0, ARDY = 0) for ^{t}DBSY.
3. The READ PAGE CACHE RANDOM (00h-31h) is issued. The column address in the address specified is ignored.
4. R/B# goes LOW and the LUN is busy (RDY = 0, ARDY = 0) for ^{t}RCBSY.

After R/B# goes HIGH and the LUN reports in the status register RDY = 1 and ARDY = 0, that signals that the internal array read is ongoing and the cache register is ready to output data from the previous read operation. The SELECT CACHE REGISTER (06h-E0h) command is required prior to outputting data. After the SELECT CACHE REGISTER (06h-E0h) command is issued, the CHANGE READ COLUMN (05h-E0h) command can also be issued.

Note: To enable data output in the other cache register or change the column address, the SELECT CACHE REGISTER (06h-E0h) command can be issued. Also, to change the column address within the currently selected plane (after the SELECT CACHE REGISTER (06h-E0h) command is issued), the CHANGE READ COLUMN (05h-E0h) command can be issued.

After issuing the last page address to be read, issue the READ PAGE CACHE LAST (3Fh) to finish the cache reading operation. Data output is similar to the previous cache read operations, requiring the SELECT CACHE REGISTER (06h-E0h) command to be issued first.

See “Multi-Plane Addressing” on page 86 for additional multi-plane addressing requirements

READ PAGE MULTI-PLANE (00h–32h)

The READ PAGE MULTI-PLANE (00h-32h) command queues a plane to transfer data from the NAND flash array to its cache register. This command can be issued one or more times. Each time a new plane address is specified, that plane is also queued for data transfer. The READ PAGE (00h-30h) command is issued to select the final plane and to begin the read operation for all previously queued planes. All queued planes will transfer data from the NAND Flash array to their cache registers.

This command is issued in the following sequence:

1. 00h is written to the command register.
2. Five address cycles are written to the address register.

3. 32h is written to the command register. (The column address in the address specified is ignored.)

After this command is issued, the following sequence occurs:

1. R/B# goes LOW and the LUN is busy (RDY = 0, ARDY = 0) for ^{t}DBSY.

Note: During ^{t}DBSY, the only valid commands are status operations (70h, 78h) and reset commands (FFh, FCh). Following ^{t}DBSY, to continue the multi-plane read operation, the only valid commands are status operations (70h, 78h), READ PAGE MULTI-PLANE (00h-32h), and READ PAGE (00h-30h).

2. R/B# goes HIGH and the LUN is ready (RDY = 1, ARDY = 1).
3. The LUN and block are queued for data transfer from the array to the cache register for the addressed plane.

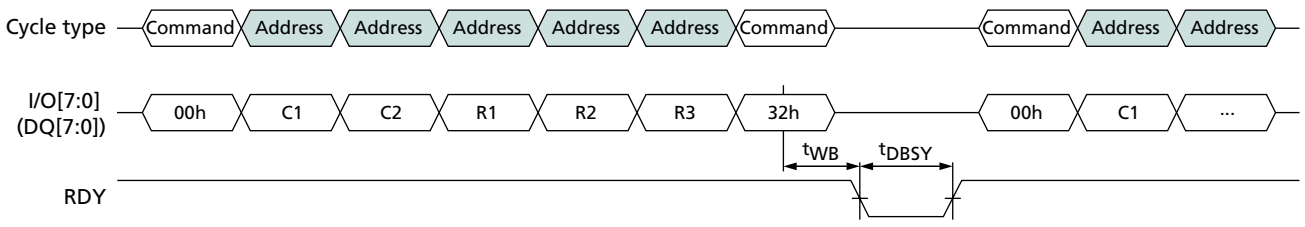
Note: Additional READ PAGE MULTI-PLANE (00h-32h) commands can be issued to queue additional planes for data transfer.

4. The READ PAGE (00h-30h) command is issued.
5. Data is transferred from the NAND Flash array for all of the addressed planes to their respective cache registers.
6. When the LUN is ready (RDY = 1, ARDY = 1), data output is enabled for the cache register linked to the even plane.
7. When the host requests data output, it begins at the column address specified in the READ PAGE (00h-30h) command.

Note: To enable data output in the other cache registers, the SELECT CACHE REGISTER (06h-E0h) command can be issued. Also, to change the column address within the currently selected plane, the CHANGE READ COLUMN (05h-E0h) command can be issued.

See “Multi-Plane Addressing” on page 86 for additional multi-plane addressing requirements.

Figure 45: READ PAGE MULTI-PLANE (00h–32h) Operation



Program Operations

Within a block, pages must be programmed sequentially from the least significant page address to the most significant page address (i.e. 0, 1, 2, ….., 127). During a program operation, the contents of the cache and/or data registers are modified by the internal control logic.

PROGRAM PAGE Operations

The PROGRAM PAGE (80h-10h) command, when not preceded by the PROGRAM PAGE MULTI-PLANE (80h-11h) command, programs one page from the cache register to the NAND Flash array. When the LUN is ready (RDY = 1, ARDY = 1), the host should check the FAIL bit to verify that the operation has completed successfully.

PROGRAM PAGE CACHE Operations

The PROGRAM PAGE CACHE (80h-15h) command can be used to improve program operation system performance. When this command is issued, the LUN goes busy (RDY = 0, ARDY = 0) while the cache register contents are copied to the data register, and the LUN is busy with a program cache operation (RDY = 1, ARDY = 0). While the contents of the data register are moved to the NAND Flash array, the cache register is available for an additional PROGRAM PAGE CACHE (80h-15h) or PROGRAM PAGE (80h-10h) command.

Note: For PROGRAM PAGE CACHE-series (80h-15h) operations, during the LUN busy times, ^{t}CBSY and ^{t}LPROG, when RDY = 0 and ARDY = 0, the only valid commands are status operations (70h, 78h) and RESET (FFh, FCh). When RDY = 1 and ARDY = 0, the only valid commands during PROGRAM PAGE CACHE-series (80h-15h) operations are status operations (70h, 78h), PROGRAM PAGE CACHE (80h-15h), PROGRAM PAGE (80h-10h), CHANGE WRITE COLUMN (85h), CHANGE ROW ADDRESS (85h), and RESET (FFh, FCh).

PROGRAM PAGE MULTI-PLANE Program Operations

The PROGRAM PAGE MULTI-PLANE (80h-11h) command can be used to improve program operation system performance by enabling multiple pages to be moved from the cache registers to different planes of the NAND Flash array. This is done by prepending one or more PROGRAM PAGE MULTI-PLANE (80h-11h) commands in front of the PROGRAM PAGE (80h-10h) command. See “Multi-Plane Operations” on page 86 for details.

PROGRAM PAGE MULTI-PLANE Program Cache Operations

The PROGRAM PAGE MULTI-PLANE (80h-11h) command can be used to improve program cache operation system performance by enabling multiple pages to be moved from the cache registers to the data registers and, while the pages are being transferred from the data registers to different planes of the NAND Flash array, free the cache registers to receive data input from the host. This is done by prepending one or more PROGRAM PAGE MULTI-PLANE (80h-11h) commands in front of the PROGRAM PAGE CACHE (80h-15h) command. See “Multi-Plane Operations” on page 86 for details.

PROGRAM PAGE (80h–10h)

The PROGRAM PAGE (80h-10h) command enables the host to input data to a cache register, and moves the data from the cache register to the specified block and page address in the array of the selected LUN. This command is accepted by the LUN when it is ready (RDY = 1, ARDY = 1). It is also accepted by the LUN when it is busy with a PROGRAM PAGE CACHE (80h-15h) operation (RDY = 1, ARDY = 0).

This command is issued in the following sequence:

1. 80h is written to the command register.

Note: Unless this command has been preceded by a PROGRAM PAGE MULTI-PLANE (80h-11h) command, issuing 80h to the command register clears all of the cache register contents on the selected target.

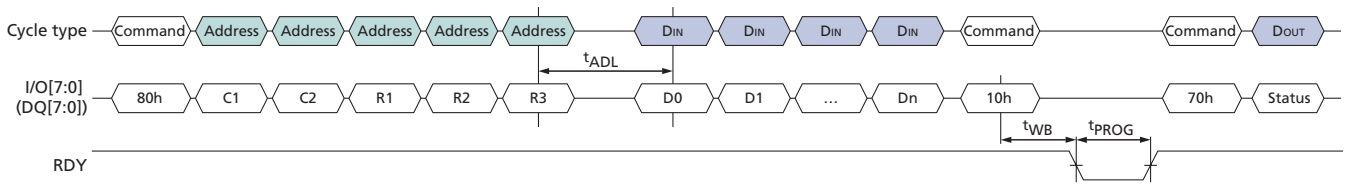
2. A page is input to the cache register and moved to the NAND Flash array at the block and page address specified.
3. Five address cycles containing the column address and row address are written to the address register.
4. The data input cycle begins. Serial data is input, beginning at the specified column address. At any time during the data input cycle, the CHANGE READ COLUMN (05h) and CHANGE ROW ADDRESS (85h) commands can be issued.
5. When the data input cycle has completed, 10h is written to the command register.
6. The selected LUN goes busy (RDY = 0, ARDY = 0) for ^{t}PROG as data is transferred.

To determine the progress of the data transfer, the host can monitor the target's R/B# signal or, alternatively, the status operations (70h, 78h) may be used. When the LUN is ready (RDY = 1, ARDY = 1), the host should check the status of the FAIL bit.

In devices that have more than one LUN per target, during and following multi-LUN operations, the SELECT LUN WITH STATUS (78h) command must be used to select only one LUN for status output. Use of the READ STATUS (70h) command could cause more than one LUN to respond, resulting in bus contention.

7. If a multi-plane program operation is being performed, the PROGRAM PAGE (80h-10h) command is written to the command register as the final command. It is preceded by one or more PROGRAM PAGE MULTI-PLANE (80h-11h) commands. Data is transferred from the cache registers for all of the addressed planes to the NAND Flash array. The host should check the status of the operation by using the status operations (70h, 78h). See"Multi-Plane Addressing" on page 86 for multi-plane addressing requirements.

Figure 46: PROGRAM PAGE (80h–10h) Operation



PROGRAM PAGE CACHE (80h–15h)

The PROGRAM PAGE CACHE (80h-15h) command enables the host to input data to a cache register; copies the data from the cache register to the data register; then moves the data register contents to the specified block and page address in the array of the selected LUN. After the data is copied to the data register, the cache register is available for additional PROGRAM PAGE CACHE (80h-15h) or PROGRAM PAGE (80h-10h) commands. The PROGRAM PAGE CACHE (80h-15h) command is accepted by the LUN when it is ready (RDY = 1, ARDY = 1). It is also accepted by the LUN when busy with a PROGRAM PAGE CACHE (80h-15h) operation (RDY = 1, ARDY = 0).

This command is issued in the following sequence to input a page to the cache register and move it to the NAND array at the block and page address specified:

1. 80h is written to the command register.

Note: Unless this command has been preceded by a PROGRAM PAGE MULTI-PLANE (80h-11h) command, issuing 80h to the command register clears all of the cache register's contents on the selected target.

2. Five address cycles containing the column address and row address are written [to the address register.
3. The data input cycles follow. Serial data is input, beginning at the specified column address. At any time during the data input cycle, the CHANGE READ COLUMN (85h) and CHANGE ROW ADDRESS (85h) commands can be issued.
4. When the data input cycle has completed, 15h is written to the command register.
5. The selected LUN goes busy (RDY = 0, ARDY = 0) for ^{t}CBSY to give the data register time to become available from a previous program cache operation; to copy data from the cache register to the data register; then begin moving the data register contents to the specified page and block address.

   To determine the progress of ^{t}CBSY, the host can monitor the target's R/B# signal or, alternatively, the status operations (70h, 78h) can be used. When the LUN's status shows that it is busy with a program cache operation (RDY = 1, ARDY = 0), the host should check the status of the FAILC bit to see if a previous cache operation was successful.
6. If, after ^{t}CBSY, the host wants to wait for the program cache operation to complete, without issuing the PROGRAM PAGE (80h-10h) command, the host should monitor ARDY until it is "1." The host should then check the status of the FAIL and FAILC bits.

   In devices with more than one LUN per target, during and following multi-LUN operations, the SELECT LUN WITH STATUS (78h) command must be used to select only one LUN for status output. Use of the READ STATUS (70h) command could cause more than one LUN to respond, resulting in bus contention.

7. The PROGRAM PAGE CACHE (80h-15h) command is used as the final command of a multi-plane program cache operation. It is preceded by one or more PROGRAM PAGE MULTI-PLANE (80h-11h) commands. Data for all of the addressed planes is transferred from the cache registers to the corresponding data registers, then moved to the NAND Flash array. The host should check the status of the operation by using the status operations (70h, 78h). See"Multi-Plane Addressing" on page 86 for multi-plane addressing requirements.

Figure 47: PROGRAM PAGE CACHE (80h–15h) Operation (Start)

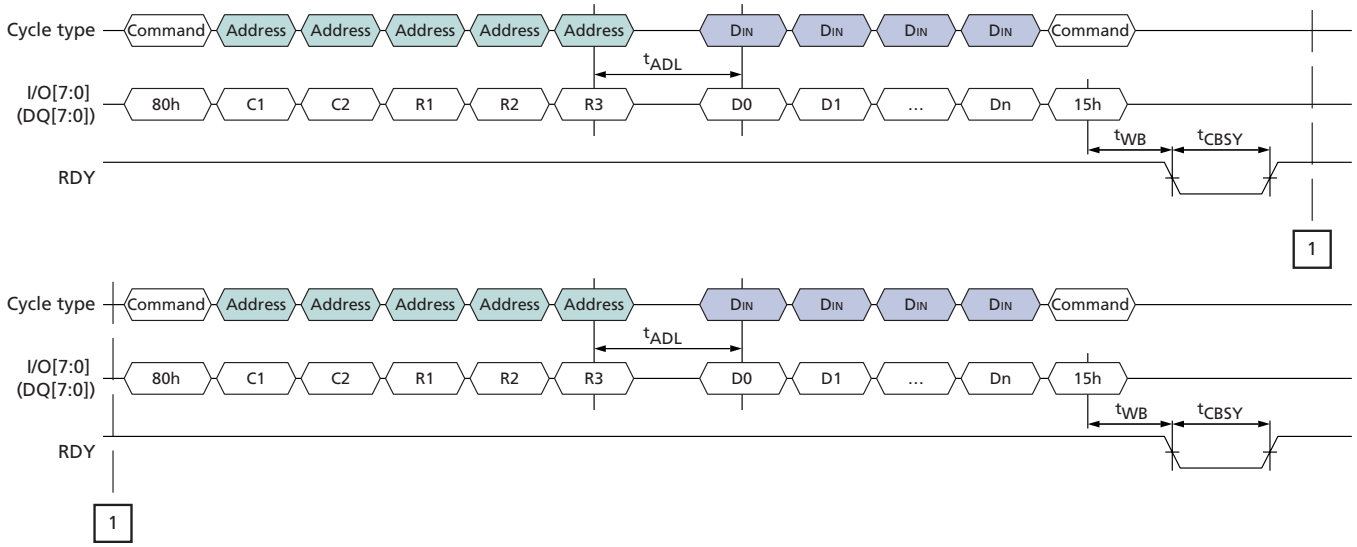
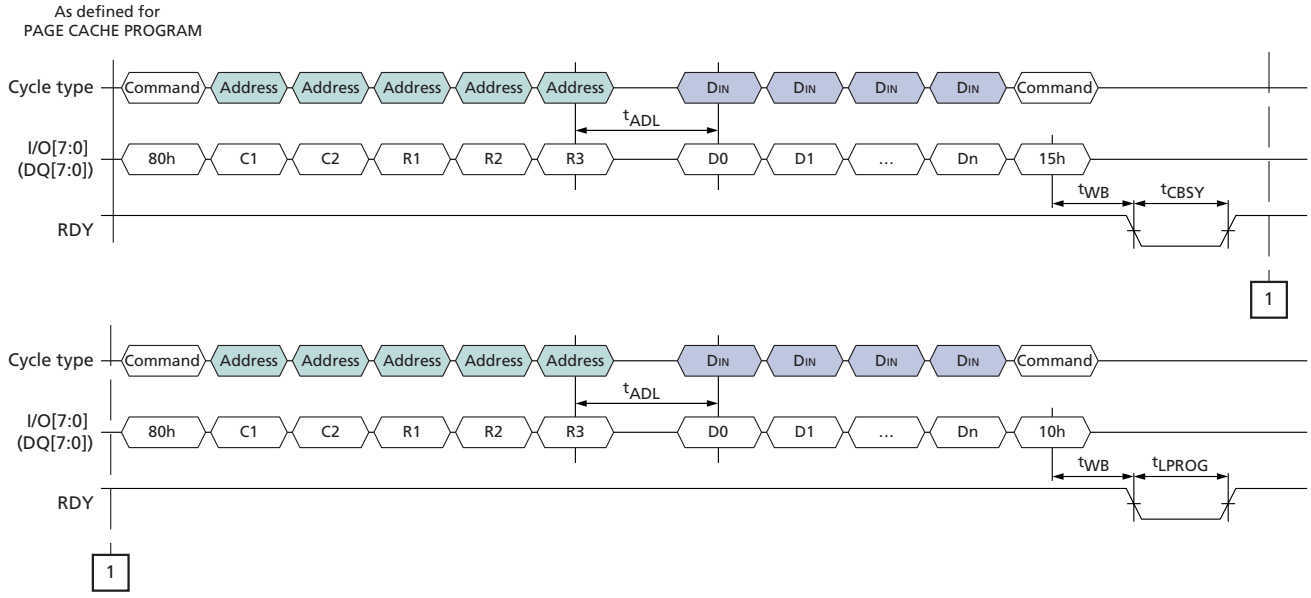


Figure 48: PROGRAM PAGE CACHE (80h–15h) Operation (End)



PROGRAM PAGE MULTI-PLANE 80h-11h

The PROGRAM PAGE MULTI-PLANE (80h-11h) command enables the host to input data to the addressed plane's cache register and queue the cache register to ultimately be moved to the NAND Flash array. This command can be issued one or more times. Each time a new plane address is specified that plane is also queued for data transfer. To input data for the final plane and to begin the program operation for all previously queued

planes, issue either the PROGRAM PAGE (80h-10h) command or the PROGRAM PAGE CACHE (80h-15h) command. All of the queued planes will move the data to the NAND Flash array. This command is accepted by the LUN when it is ready (RDY = 1).

To input a page to the cache register and queue it to be moved to the NAND Flash array at the block and page address specified, write 80h to the command register. Unless this command has been preceded by a PROGRAM PAGE MULTI-PLANE (80h-11h) command, issuing the 80h to the command register clears all of the cache registers' contents on the selected target. Write five address cycles containing the column address and row address; data input cycles follow. Serial data is input beginning at the column address specified. At any time during the data input cycle, the CHANGE READ COLUMN (85h) and CHANGE ROW ADDRESS (85h) commands can be issued. When data input is complete, write 11h to the command register. The selected LUN will go busy (RDY = 0 , ARDY = 0) for ^{t}DBSY.

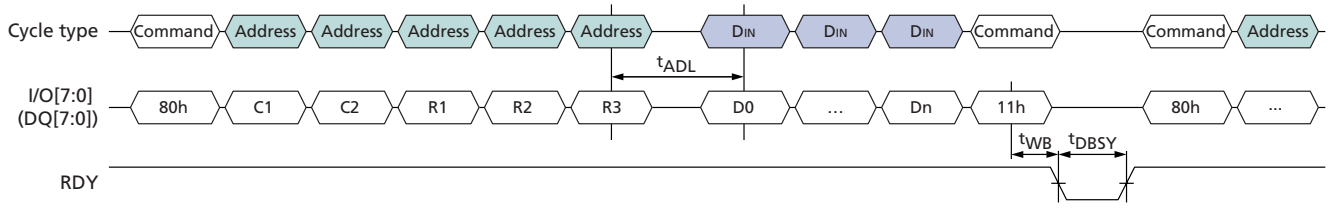
To determine the progress of ^{t}DBSY, the host can monitor the target's R/B# signal, or alternatively, the status operations (70h, 78h) can be used. When the LUN's status shows that it is ready (RDY = 1), additional PROGRAM PAGE MULTI-PLANE (80h-11h) commands can be issued to queue additional planes for data transfer. Alternatively, the PROGRAM PAGE (80h-10h) or PROGRAM PAGE CACHE (80h-15h) commands can be issued.

When the PROGRAM PAGE (80h-10h) command is used as the final command of a multi-plane program operation, data is transferred from the cache registers to the NAND Flash array for all of the addressed planes during ^{t}PROG. When the LUN is ready (RDY = 1, ARDY = 1), the host should check the status of the FAIL bit for each of the planes to verify that programming completed successfully.

When the PROGRAM PAGE CACHE (80h-15h) command is used as the final command of a MULTI-PLANE PROGRAM CACHE operation, data is transferred from the cache registers to the data registers after the previous array operations finish. The data is then moved from the data registers to the NAND Flash array for all of the addressed planes. This occurs during ^{t}CBSY. After ^{t}CBSY, the host should check the status of the FAILC bit for each of the planes from the previous program cache operation, if any, to verify that programming completed successfully.

For the PROGRAM PAGE MULTI-PLANE (80h-11h), PROGRAM PAGE (80h-10h), and PROGRAM PAGE CACHE (80h-15h) commands, See “Multi-Plane Addressing” on page 86 for multi-plane addressing requirements.

Figure 49: PROGRAM PAGE MULTI-PLANE (80h–11h) Operation



ERASE Operations

ERASE operations are used to clear the contents of a block in the NAND Flash array to prepare its pages for program operations.

ERASE Operations

The ERASE BLOCK (60h-D0h) command, when not preceded by the ERASE BLOCK MULTI-PLANE (60h-D1h) command, erases one block in the NAND Flash array. When the LUN is ready (RDY = 1, ARDY = 1), the host should check the FAIL bit to verify that this operation completed successfully.

MULTI-PLANE ERASE Operations

The ERASE BLOCK MULTI-PLANE (60h-D1h) command can be used to improve erase operation system performance by enabling multiple blocks to be erased in the NAND Flash array. This is done by prepending one or more ERASE BLOCK MULTI-PLANE (60h-D1h) commands in front of the ERASE BLOCK (60h-D0h) command. See “Multi-Plane Operations” on page 86 for details.

ERASE BLOCK (60h–D0h)

The ERASE BLOCK (60h-D0h) command erases the specified block in the NAND Flash array. This command is accepted by the LUN when it is ready (RDY = 1, ARDY = 1).

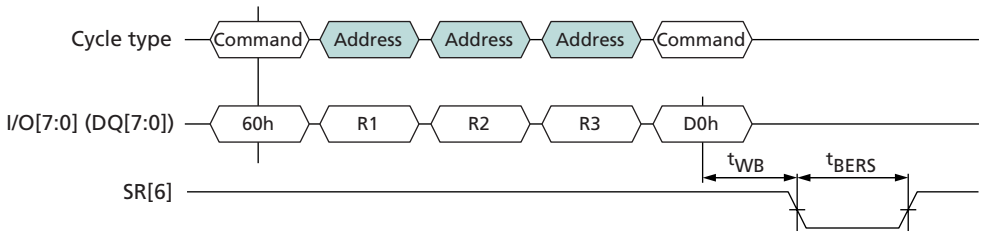
To erase a block, write 60h to the command register. Then write three address cycles containing the row address; the page address is ignored. Conclude by writing D0h to the command register. The selected LUN will go busy (RDY = 0, ARDY = 0) for ^{t}BERS while the block is erased.

To determine the progress of an ERASE operation, the host can monitor the target's R/B# signal, or alternatively, the status operations (70h, 78h) can be used. When the LUN is ready (RDY = 1, ARDY = 1) the host should check the status of the FAIL bit.

In devices that have more than one LUN per target, during and following multi-LUN operations, the SELECT LUN WITH STATUS (78h) command must be used to select only one LUN for status output. Use of the READ STATUS (70h) command could cause more than one LUN to respond, resulting in bus contention.

The ERASE BLOCK (60h-D0h) command is used as the final command of a MULTI-PLANE ERASE operation. It is preceded by one or more ERASE BLOCK MULTI-PLANE (60h-D1h) commands. All of blocks in the addressed planes are erased. The host should check the status of the operation by using the status operations (70h, 78h). See “Multi-Plane Addressing” on page 86 for multi-plane addressing requirements.

Figure 50: ERASE BLOCK (60h–D0h) Operation



ERASE BLOCK MULTI-PLANE (60h–D1h)

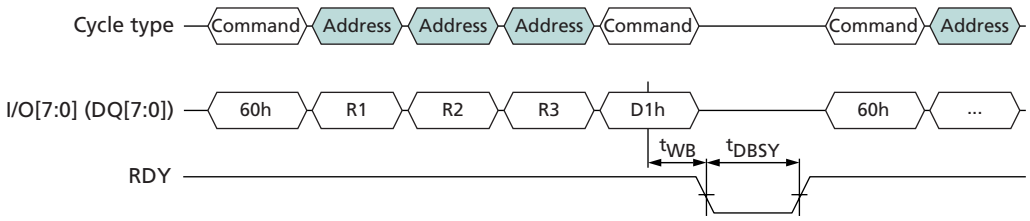
The ERASE BLOCK MULTI-PLANE (60h-D1h) command queues a block in the specified plane to be erased in the NAND Flash array. This command can be issued one or more times. Each time a new plane address is specified, that plane is also queued for a block to be erased. To specify the final block to be erased and to begin the erase operation for all previously queued planes, issue the ERASE BLOCK (60h-D0h) command. This command is accepted by the LUN when it is ready (RDY = 1, ARDY = 1).

To queue a block to be erased, write 60h to the command register, then write three address cycles containing the row address; the page address is ignored. Conclude by writing D1h to the command register. The selected LUN will go busy (RDY = 0, ARDY = 0) for ^{t}DBSY.

To determine the progress of ^{t}DBSY, the host can monitor the target's R/B# signal, or alternatively, the status operations (70h, 78h) can be used. When the LUN's status shows that it is ready (RDY = 1, ARDY = 1), additional ERASE BLOCK MULTI-PLANE (60h-D1h) commands can be issued to queue additional planes for erase. Alternatively, the ERASE BLOCK (60h-D0h) command can be issued to erase all of the queued blocks.

For the ERASE BLOCK MULTI-PLANE (60h-D1h) and ERASE BLOCK (60h-D0h) commands, see “Multi-Plane Addressing” on page 86 for multi-plane addressing requirements.

Figure 51: ERASE BLOCK MULTI-PLANE (60h–D1h) Operation



COPYBACK Operations

COPYBACK operations make it possible to transfer data within a plane from one page to another using the cache register. This is particularly useful for block management and wear-leveling.

The COPYBACK operation is a two-step process consisting of a COPYBACK READ (00h-35h) and a COPYBACK PROGRAM (85h-10h) command. To move data from one page to another on the same plane, first issue the COPYBACK READ (00h-35h) command. When the LUN is ready (RDY = 1, ARDY = 1), the host can transfer the data to a new page by issuing the COPYBACK PROGRAM (85h-10h) command. When the LUN is again ready (RDY = 1, ARDY = 1), the host should check the FAIL bit to verify that this operation completed successfully.

To prevent bit errors from accumulating over multiple COPYBACK operations, it is recommended that the host read the data out of the cache register after the COPYBACK READ (00h-35h) completes, prior to issuing the COPYBACK PROGRAM (85h-10h) command. The CHANGE READ COLUMN (05h-E0h) command can be used to change the column address. The host should check the data for ECC errors and correct them. When the COPYBACK PROGRAM (85h-10h) command is issued, any corrected data can be input. The CHANGE WRITE COLUMN (85h) command can be used to change the column address.

It is not possible to use the COPYBACK operation to move data from one plane to another or from one LUN to another. This is accomplished using a READ PAGE (00h-30h) or COPYBACK READ (00h-35h) command, reading the data out of the NAND, and then using a PROGRAM PAGE or COPYBACK PROGRAM (85h-10h) command with data input to program the data to a new plane or LUN.

Between the COPYBACK READ (00h-35h) and COPYBACK PROGRAM (85h-10h) commands, the following commands are supported: status operations (70h, 78h), and column address operations (05h-E0h, 06h-E0h, 85h). RESET operations (FFh, FCh) can be issued after COPYBACK READ (00h-35h), but the contents of the cache registers on the target are not valid.

In devices that have more than one LUN per target, after COPYBACK READ (00h-35h) is issued, multi-LUN operations are prohibited until after the COPYBACK PROGRAM (85h-10h) command is issued.

MULTI-PLANE COPYBACK Operations

MULTI-PLANE COPYBACK READ operations improve read data throughput by copying data simultaneously from more than one plane to the specified cache registers. This is done by prepending one or more READ PAGE MULTI-PLANE (00h-32h) commands in front of the COPYBACK READ (00h-35h) command.

The COPYBACK PROGRAM MULTI-PLANE (85h-11h) command can be used to improve system performance of COPYBACK PROGRAM operations by enabling movement of multiple pages from the cache registers to different planes of the NAND Flash array. This is done by prepending one or more COPYBACK PROGRAM (85h-11h) commands in front of the COPYBACK PROGRAM (85h-10h) command.

See “Multi-Plane Operations” on page 86 for details.

COPYBACK READ (00h–35h)

The COPYBACK READ (00h-35h) command is functionally identical to the READ PAGE (00h-30h) command, except that 35h is written to the command register instead of 30h. See "READ PAGE (00h–30h)" on page 64 for further details.

Though it is not required, it is recommended that the host read the data out of the device to verify the data prior to issuing the COPYBACK PROGRAM (85h-10h) command to prevent the propagation of data errors.

Figure 52: COPYBACK READ (00h–35h) Operation

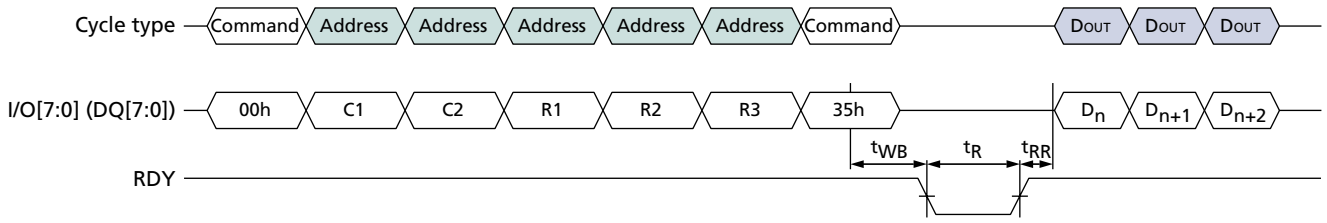
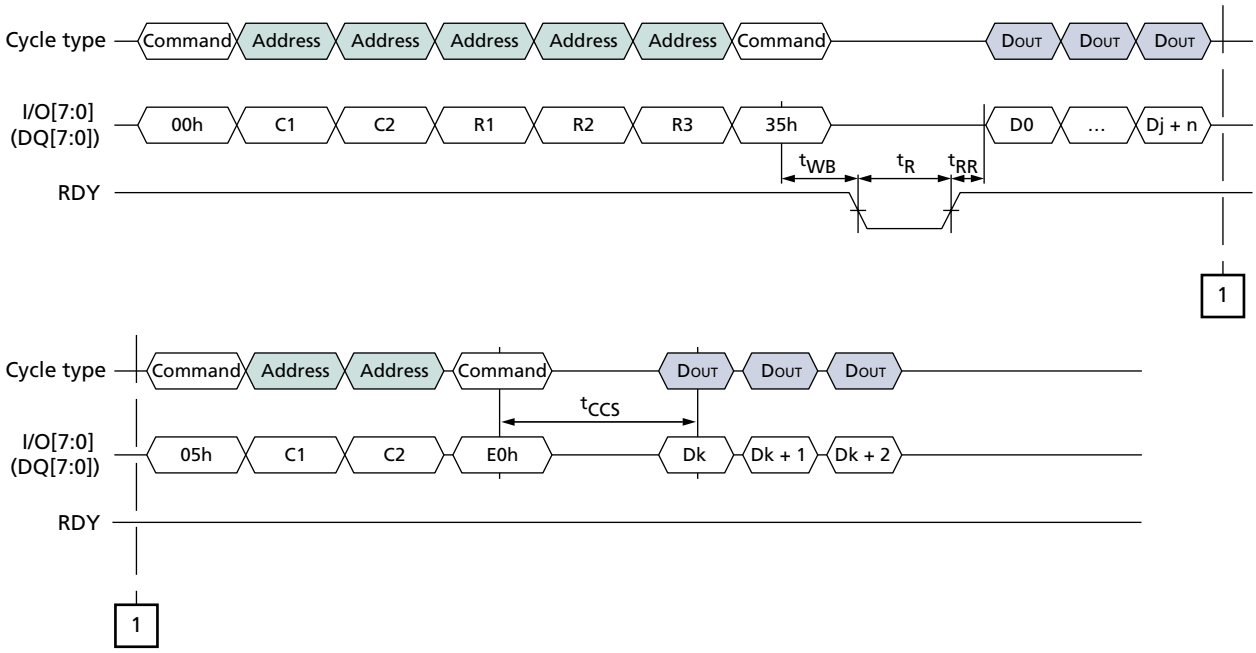


Figure 53: COPYBACK READ (00h–35h) with CHANGE READ COLUMN (05h–E0h) Operation



COPYBACK PROGRAM (85h–10h)

The COPYBACK PROGRAM (85h-10h) command is functionally identical to the PROGRAM PAGE (80h-10h) command, except that when 85h is written to the command register, cache register contents are not cleared. See "PROGRAM PAGE (80h–10h)" on page 72 for further details.

Figure 54: COPYBACK PROGRAM (85h–10h) Operation

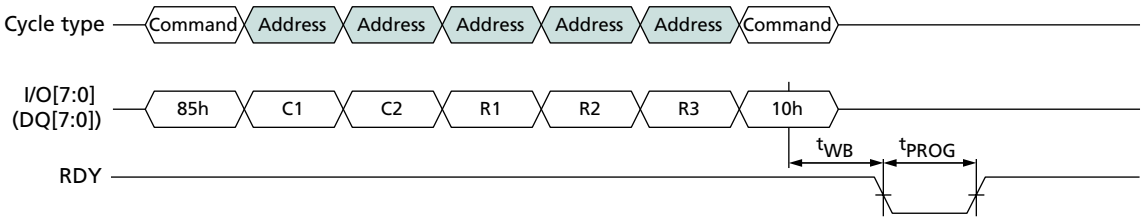
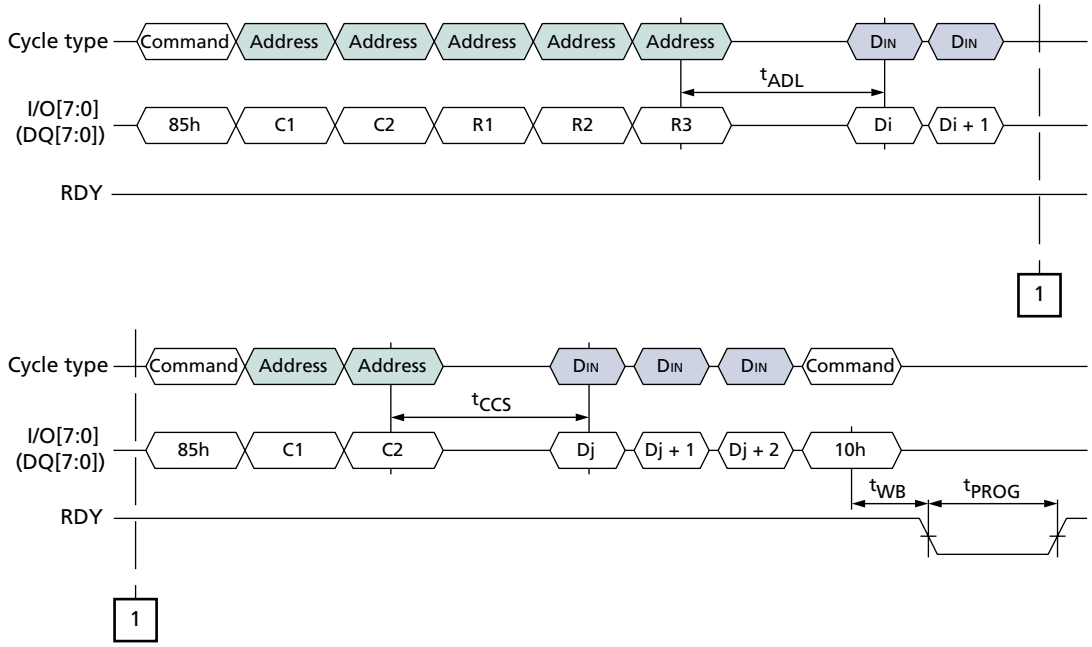


Figure 55: COPYBACK PROGRAM (85h–10h) with CHANGE WRITE COLUMN (85h) Operation



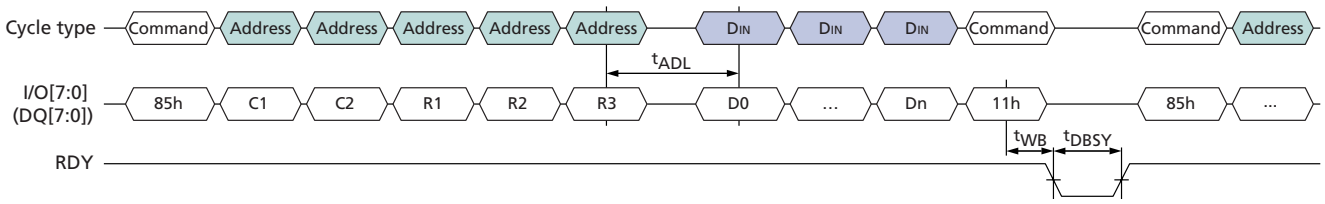
COPYBACK READ MULTI-PLANE (00h-32h)

The COPYBACK READ MULTI-PLANE (00h-32h) command is functionally identical to the READ PAGE MULTI-PLANE (00h-32h) command, except that the 35h command is written as the final command. The complete command sequence for the COPYBACK READ PAGE MUTLI-PLANE is 00h-32h-00h-35h. See "READ PAGE MULTI-PLANE (00h-32h)" on page 66 for further details.

COPYBACK PROGRAM MULTI-PLANE (85h-11h)

The COPYBACK PROGRAM MULTI-PLANE (85h-11h) command is functionally identical to the PROGRAM PAGE MULTI-PLANE (85h-11h) command, except that when 85h is written to the command register, cache register contents are not cleared. See "PROGRAM PAGE MULTI-PLANE 80h-11h" on page 63 for further details.

Figure 56: COPYBACK PROGRAM MULTI-PLANE (85h–11h) Operation



One-Time Programmable (OTP) Operations

This Micron NAND Flash device offers a protected, one-time programmable NAND Flash memory area. Thirty full pages (4,320 bytes per page) of OTP data are available on the target, and the entire range is guaranteed to be good. Customers can use the OTP area in any way they desire; typical uses include programming serial numbers or other data for permanent storage.

In Micron NAND Flash devices, the OTP area leaves the factory in an erased state (all bits are "1"). Programming enables the user to program only "0" bits in the OTP area. The OTP area cannot be erased, even if it is not protected. Protecting the OTP area simply prevents further programming of the OTP area.

While the OTP area is referred to as "one-time programmable," Micron provides a unique way to program and verify data-before permanently protecting it and preventing future changes.

The OTP area is only accessible while in OTP operation mode. To set the device to OTP operation mode, issue the SET FEATURES (EFh) command to feature address 90h and write 01h to P1, followed by 3 cycles of 00h to P2 through P4.

When the device is in OTP operation mode, all subsequent PAGE READ (00h-30h) and PROGRAM PAGE (80h-10h) commands are applied to the OTP area. The OTP area is assigned to page addresses 02h through 1Fh.

OTP programming and protection are achieved in two discrete operations. Each page in the OTP area is programmed using the PROGRAM OTP PAGE (80h-10h) command. The pages in the OTP area (02h-1Fh) must be programmed in ascending order.

To protect the OTP area, issue the 80h command followed by five address cycles (00h-00h-01h-00h-00h), followed by the 10h command. R/B# goes LOW for ^{t}PROG.

To read pages in the OTP area, whether or not the area is protected, issue the PAGE READ (00h-30h) command.

ERASE commands are not valid while the device is in OTP operation mode.

To exit OTP operation mode, issue the SET FEATURES (EFh) command to feature address 90h and write 00h to P1 through P4.

If the host device issues a PAGE PROGRAM (80h-10h) command to an address beyond the maximum page-address range, the device will be busy for ^{t}OBSY and the WP# status register bit will be"0," meaning that the page is write-protected.

If the host device issues the PAGE READ (00h-30h) command to an address beyond the maximum page-address range, the data output will not be valid. To determine whether or not the device is busy during an OTP operation, either monitor R/B# or use the READ STATUS (70h) command. Use of the SELECT LUN WITH STATUS (78h) command is prohibited while the OTP operation is in progress.

If the RESET (FFh) command is issued while in OTP operation mode, the device will exit OTP operation mode and enter normal operating mode. If the device is in the synchronous interface it will exit OTP operation and enter normal operation mode in asynchronous interface.

If the SYNCHRONOUS RESET (FCh) command is issued while in the OTP operation mode, the device will exit OTP operation mode and stay in synchronous interface.

PROGRAM OTP PAGE (80h–10h)

The PROGRAM OTP PAGE (80h-10h) command is used to write data to the pages within the OTP area. An entire page is programmed at one time. To program data in the OTP area, the device must be in OTP operating mode.

To use the PROGRAM PAGE command, issue the 80h command. Issue 5 address cycles: the first 2 address cycles are the column address, and for the remaining 3 cycles, select a page in the range of 02h-00h-00h through 1Fh-00h-00h. Next, write the data to the cache register using data input cycles. After data input is complete, issue the 10h command.

R/B# goes LOW for the duration of the array programming time, ^{t}PROG. The READ STATUS (70h) command is the only valid command for reading status in OTP operation mode. The RDY bit of the status register will reflect the state of R/B#. Use of the SELECT LUN WITH STATUS (78h) command is prohibited.

When the device is ready, read the FAIL bit of the status register to determine if the operation passed or failed (see Table 14 on page 56).

The PROGRAM OTP PAGE (80h-10h) command also accepts the CHANGE WRITE COLUMN (85h) command during data input.

If a PROGRAM PAGE command is issued to the OTP area after the area has been protected, R/B# goes LOW for ^{t}OBSY. After ^{t}OBSY, the status register is set to 60h.

It is possible to program each OTP page a maximum of 8 times.

Figure 57: PROGRAM OTP PAGE (80h–10h) Operation

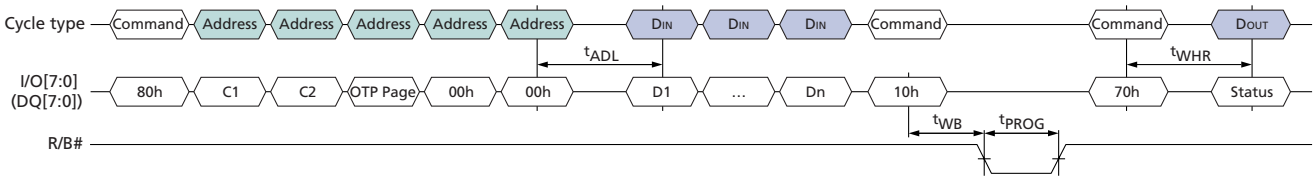
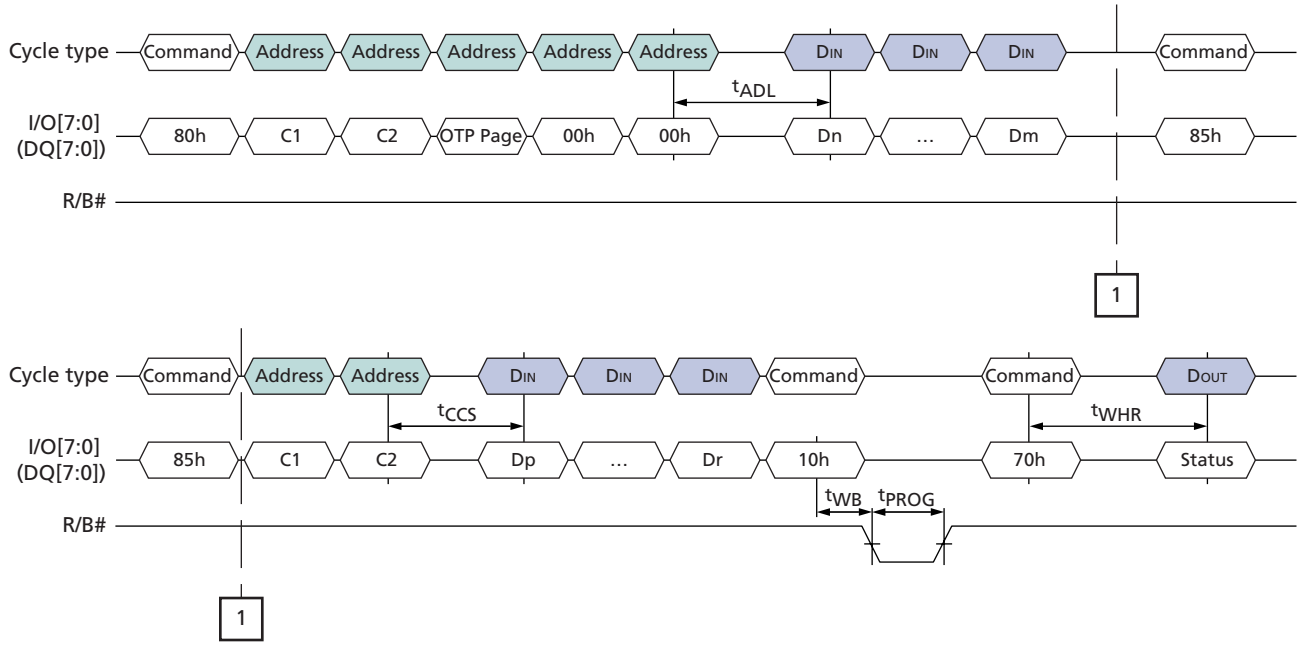


Figure 58: PROGRAM OTP PAGE (80h–10h) with CHANGE WRITE COLUMN (85h) Operation



PROTECT OTP AREA (80h–10h)

To protect all data in the OTP area, set the device to OTP operating mode, then issue the PROTECT OTP AREA (80h-10h) command to page 1 in block 0 and write “00h” for the first byte location.

After the OTP AREA is protected it cannot be programmed further. When the OTP area is protected, the pages within the area are no longer programmable and cannot be unprotected.

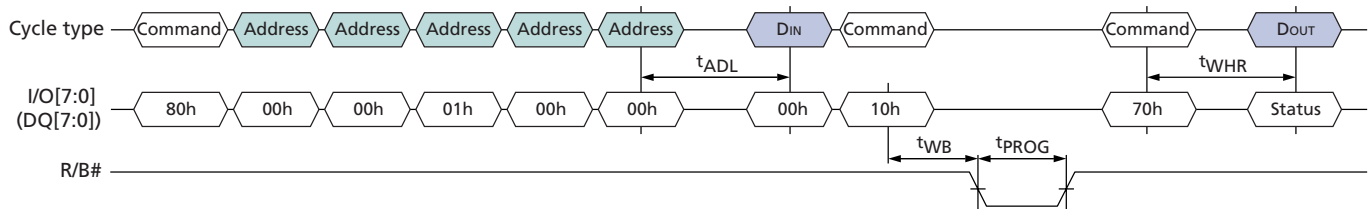
To use the PROTECT OTP AREA (80h-10h) command to protect the OTP area, issue the 80h command. Next, issue the following 5 address cycles: 00h-00h-01h-00h-00h. Finally, issue the 10h command.

R/B# goes LOW for the duration of the array programming time, ^{t}PROG. The READ STATUS (70h) command is the only valid command for reading status in OTP operating mode. The RDY bit of the status register will reflect the state of R/B#. Use of the SELECT LUN WITH STATUS (78h) command is prohibited.

If the PROTECT OTP AREA (80h-10h) command is issued after the OTP area has already been protected, R/B# goes LOW for ^{t}OBSY. After ^{t}OBSY, the status register is set to 60h.

When the device is ready, read the FAIL bit of the status register to determine if the operation passed or failed (see Table 14 on page 56).

Figure 59: PROTECT OTP AREA (80h–10h) Operation



Notes: 1. OTP data is protected following a "pass" status confirmation.

READ OTP PAGE (00h–30h)

To read data from the OTP area, set the device to OTP operation mode, then issue the READ OTP PAGE (00h-30h) command. Data can be read from OTP pages within the OTP area whether or not the area is protected.

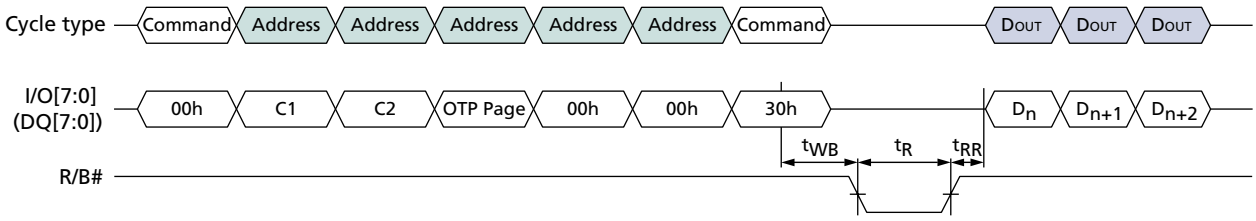
To use the READ OTP PAGE (00h-30h) command for reading data from the OTP area, issue the 00h command. Next, issue five address cycles: the first 2 address cycles are the column address, and for the remaining three cycles select a page in the range of 02h-00h-00h through 1Fh-00h-00h. Finally, issue the 30h command. The selected LUN will go busy (RDY = 0, ARDY = 0) for ^{t}R as data is transferred.

To determine the progress of the data transfer, the host can monitor the target's R/B# signal, or alternatively the READ STATUS (70h) command can be used. If the status operations are used to monitor the LUN's status, when the LUN is ready (RDY = 1, ARDY = 1) the host disables status output and enables data output by issuing the READ MODE (00h) command. When the host requests data output, it begins at the column address specified.

Additional pages within the OTP area can be selected by repeating the READ OTP PAGE (00h-30h) command.

The READ OTP PAGE (00h-30h) command is compatible with the CHANGE READ COLUMN (05h-E0h) command. Use of the SELECT LUN WITH STATUS (78h) and SELECT CACHR REGISTER (06h-E0h) commands are prohibited.

Figure 60: READ OTP PAGE (00h–30h) Operation



Multi-Plane Operations

Each NAND Flash logical unit (LUN) is divided into multiple physical planes. Each plane contains a cache register and a data register independent of the other planes. The planes are addressed via the low-order block address bits. Specific details are provided in Figure 8 and Table 2 on page 13.

Multi-plane operations make better use of the NAND Flash arrays on these physical planes by performing concurrent READ, PROGRAM, or ERASE operations on multiple planes, significantly improving system performance. Multi-plane operations must be of the same type across the planes; for example, it is not possible to perform a PROGRAM operation on one plane with an ERASE operation on another.

When issuing MULTI-PLANE PROGRAM or ERASE operations, use the READ STATUS (70h) command and check whether the previous operation(s) failed. If the READ STATUS (70h) command indicates that an error occurred (FAIL = 1 and/or FAILC = 1), use the SELECT LUN WITH STATUS (78h) command—time for each plane—to determine which plane operation failed.

Multi-Plane Addressing

Multi-plane commands require multiple 5-cycle addresses, one address per operational plane. For a given multi-plane operation, these addresses are subject to the following requirements:

- The LUN address bit(s) must be identical for all of the issued addresses.
- The plane select bit, BA[7], must be different for each issued address.
- The page address bits, PA[6:0], must be identical for each issued address.

The READ STATUS (70h) command should be used following MULTI-PLANE PROGRAM PAGE and ERASE BLOCK operations on a single LUN.

Multi-LUN Operations

In devices that have more than one LUN per target, it is possible to improve performance by interleaving operations between the LUNs. A multi-LUN operation is one that is issued to an idle LUN (RDY = 1) while another LUN is busy (RDY = 0).

Multi-LUN operations are prohibited following RESET (FFh, FCh), identification (90h, ECh, EDh), and configuration (EEh, EFh) operations until ARDY =1 for all of the LUNs on the target.

During a multi-LUN operation, there are two methods to determine operation completion. The R/B# signal indicates when all of the LUNs have finished their operations. R/B# remains LOW while any LUN is busy. When R/B# goes HIGH, all of the LUNs are idle and the operations are complete. Alternatively, the SELECT LUN WITH STATUS (78h) command can report the status of each LUN individually.

If a LUN is performing a cache operation, like PROGRAM PAGE CACHE (80h-15h), then the LUN is able to accept the data for another cache operation when status register bit 6 is "1." All operations, including cache operations, are complete on a die when status register bit 5 is "1."

During and following multi-LUN operations, the READ STATUS (70h) command is prohibited. Instead, use the SELECT LUN WITH STATUS (78h) command to monitor status. This command selects which LUN will report status. When multi-plane commands are used with multi-LUN operations, the multi-plane commands must also meet the requirements in "Multi-Plane Operations" on page 86.

See Table 5 on page 39 for the list of commands that can be issued while other LUNs are busy.

During a multi-LUN operation that involves a PROGRAM-series (80h-10h, 80h-15h, 80h-11h) operation and a READ operation, the PROGRAM-series operation must be issued before the READ-series operation. The data from the READ-series operation must be output to the host before the next PROGRAM-series operation is issued. This is because the 80h command clears the cache register contents of all cache registers on all planes.

Error Management

Each NAND Flash LUN is specified to have a minimum number of valid blocks (NVB) of the total available blocks. This means the LUNs could have blocks that are invalid when shipped from the factory. An invalid block is one that contains at least one page that has more bad bits than can be corrected by the minimum required ECC. Additional blocks can develop with use. However, the total number of available blocks per LUN will not fall below NVB during the endurance life of the product.

Although NAND Flash memory devices could contain bad blocks, they can be used quite reliably in systems that provide bad-block management and error-correction algorithms. This type of software environment ensures data integrity.

Internal circuitry isolates each block from other blocks, so the presence of a bad block does not affect the operation of the rest of the NAND Flash array.

NAND Flash devices are shipped from the factory erased. The factory identifies invalid blocks before shipping by attempting to program the bad-block mark into every location in the first page of each invalid block. It may not be possible to program every location with the bad-block mark. However, the first spare area location in each bad block is guaranteed to contain the bad-block mark. This method is compliant with ONFI Factory Defect Mapping requirements. See Table 15 for the first spare area location and the bad-block mark.

System software should check the first spare area location on the first page of each block prior to performing any PROGRAM or ERASE operations on the NAND Flash device. A bad block table can then be created, enabling system software to map around these areas. Factory testing is performed under worst-case conditions. Because invalid blocks could be marginal, it may not be possible to recover this information if the block is erased.

Over time, some memory locations may fail to program or erase properly. In order to ensure that data is stored properly over the life of the NAND Flash device, the following precautions are required:

- Always check status after a PROGRAM or ERASE operation.
- Under typical conditions, use the minimum required ECC shown in Table 15.
- Use bad-block management and wear-leveling algorithms.

Table 15: Error Management Details

Description	Requirement
Minimum number of valid blocks (NVB) per LUN	2,008
Total available blocks per LUN	2,048
First spare area location	Byte 4,096
Bad-block mark	00h
Minimum required ECC	4-bit ECC per 540 bytes of data

Output Drive Strength

Because High Speed NAND Flash is designed for use in systems that are typically point-to-point connections, an option to control the drive strength of the output buffers is provided. Drive strength should be selected based on the expected loading of the memory bus. There are four supported settings for the output drivers - overdrive 2, overdrive 1, nominal, and underdrive.

The Nominal output drive strength setting is the power-on default value. The host can select a different drive strength setting using the SET FEATURES (EFh) command.

The output impedance range from minimum to maximum covers process, voltage, and temperature variations. Devices are not guaranteed to be at the nominal line.

Table 16: Output Drive Strength Test Conditions (VccQ = 1.7–1.95V)

Range	Process	Voltage	Temperature
Minimum	Fast-Fast	1.95V	–40°C
Nominal	Typical-Typical	1.8V	+25°C
Maximum	Slow-Slow	1.7V	+85°C

Table 17: Output Drive Strength Impedance Values (VccQ = 1.7–1.95V)

Output Strength	Rpd/Rpu	VOUT to VssQ	Maximum	Nominal	Minimum	Unit
Overdrive 2	Rpd	VccQ × 0.2	7.5	13.5	34	Ohms
		VccQ × 0.5	9	18	31	Ohms
		VccQ × 0.8	11	23.5	44	Ohms
	Rpu	VccQ × 0.2	11	23.5	44	Ohms
		VccQ × 0.5	9	18	31	Ohms
		VccQ × 0.8	7.5	13.5	34	Ohms
Overdrive 1	Rpd	VccQ × 0.2	10.5	19	47	Ohms
		VccQ × 0.5	13	25	44	Ohms
		VccQ × 0.8	16	32.5	61.5	Ohms
	Rpu	VccQ × 0.2	16	32.5	61.5	Ohms
		VccQ × 0.5	13	25	44	Ohms
		VccQ × 0.8	10.5	19	47	Ohms
Nominal	Rpd	VccQ × 0.2	15	27	66.5	Ohms
		VccQ × 0.5	18	35	62.5	Ohms
		VccQ × 0.8	22	52	88	Ohms
	Rpu	VccQ × 0.2	22	52	88	Ohms
		VccQ × 0.5	18	35	62.5	Ohms
		VccQ × 0.8	15	27	66.5	Ohms
Underdrive	Rpd	VccQ × 0.2	21.5	39	95	Ohms
		VccQ × 0.5	26	50	90	Ohms
		VccQ × 0.8	31.5	66.5	126.5	Ohms
	Rpu	VccQ × 0.2	31.5	66.5	126.5	Ohms
		VccQ × 0.5	26	50	90	Ohms
		VccQ × 0.8	21.5	39	95	Ohms

Table 18: Output Drive Strength Conditions (VccQ = 2.7-3.6V)

Range	Process	Voltage	Temperature
Minimum	Fast-Fast	3.6V	–40°C
Nominal	Typical-Typical	3.3V	+25°C
Maximum	Slow-Slow	2.7V	+85°C

Table 19: Output Drive Strength Impedance Values (VccQ = 2.7-3.6V)

Output strength	Rpd/Rpu	VOUT to VssQ	Maximum	Nominal	Minimum	Unit
Overdrive 2	Rpd	VccQ x 0.2	6.0	10.0	18.0	Ohms
		VccQ x 0.5	10.0	18.0	35.0	Ohms
		VccQ x 0.8	15.0	25.0	49.0	Ohms
	Rpu	VccQ × 0.2	15.0	25.0	49.0	Ohms
		VccQ × 0.5	10.0	18.0	35.0	Ohms
		VccQ × 0.8	6.0	10.0	18.0	Ohms
Overdrive 1	Rpd	VccQ x 0.2	8.0	15.0	30.0	Ohms
		VccQ x 0.5	15.0	25.0	45.0	Ohms
		VccQ x 0.8	20.0	35.0	65.0	Ohms
	Rpu	VccQ × 0.2	20.0	35.0	65.0	Ohms
		VccQ × 0.5	15.0	25.0	45.0	Ohms
		VccQ × 0.8	8.0	15.0	30.0	Ohms
Nominal	Rpd	VccQ x 0.2	12.0	22.0	40.0	Ohms
		VccQ x 0.5	20.0	35.0	65.0	Ohms
		VccQ x 0.8	25.0	50.0	100.0	Ohms
	Rpu	VccQ × 0.2	25.0	50.0	100.0	Ohms
		VccQ × 0.5	20.0	35.0	65.0	Ohms
		VccQ × 0.8	12.0	22.0	40.0	Ohms
Underdrive	Rpd	VccQ x 0.2	18.0	32.0	55.0	Ohms
		VccQ x 0.5	29.0	50.0	100.0	Ohms
		VccQ x 0.8	40.0	75.0	150.0	Ohms
	Rpu	VccQ × 0.2	40.0	75.0	150.0	Ohms
		VccQ × 0.5	29.0	50.0	100.0	Ohms
		VccQ × 0.8	18.0	32.0	100.0	Ohms

Table 20: Pull-Up and Pull-Down Output Impedance Mismatch

Drive Strength	Minimum	Maximum	Notes
Overdrive 2	0Ω	6.3Ω	1, 2
Overdrive 1	0Ω	8.8Ω	1, 2
Nominal	0Ω	12.3Ω	1, 2
Underdrive	0Ω	17.5Ω	1, 2

Notes:
1. Mismatch is the absolute value between pull-up and pull-down impedances. Both are measured at the same temperature and voltage.
2. Test conditions: VccQ = VccQ(min), Vout = VccQ × 0.5.

Synchronous AC Overshoot/Undershoot Specifications

The supported AC overshoot and undershoot area depends on the timing mode selected by the host.

Table 21: Overshoot / Undershoot Parameters

Parameter	Timing Mode					Unit
	0 (50ns)	1 (30ns)	2 (20ns)	3 (15ns)	4 (12ns)	
Maximum peak amplitude provided for overshoot area	1	1	1	1	1	V
Maximum peak amplitude provided for undershoot area	1	1	1	1	1	V
Maximum overshoot are above VCCQ	3	3	3	2.25	1.8	V-ns
Maximum undershoot area below VSSQ	3	3	3	2.25	1.8	V-ns

Figure 61: Overshoot

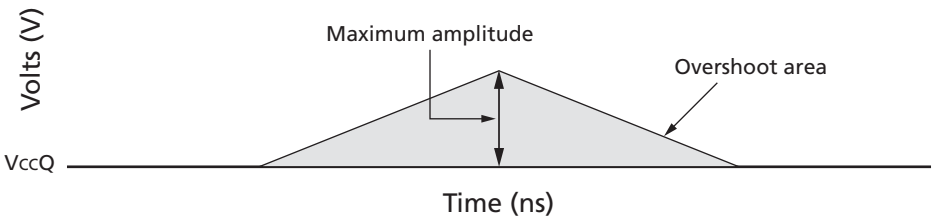
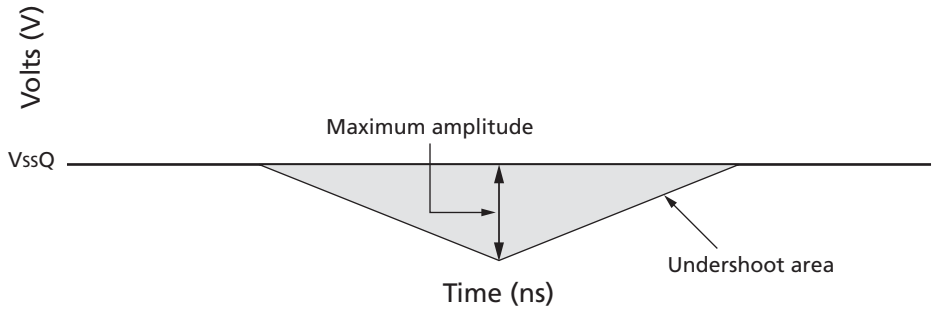


Figure 62: Undershoot



Synchronous Input Slew Rate

Though all AC timing parameters are tested with a nominal input slew rate of 1V/ns, it is possible to run the device at a slower slew rate. The input slew rates shown below are sampled, and not 100 percent tested. If using slew rates slower than the minimum values, timing must be derated by the host.

Table 22: Test Conditions for Input Slew Rate

Parameter	Value
Rising Edge	V_{IL} (DC) to V_{IH} (AC)
Falling Edge	V_{IH} (DC) to V_{IL} (AC)
Temperature Range	T_A

Table 23: Input Slew Rate (VccQ = 1.7–1.95V)

Description	Timing Mode					Unit
	0	1	2	3	4	
Input slew rate (Min)	0.5	0.5	0.5	0.5	0.5	V/ns
Derating factor for setup times	TBD	TBD	TBD	TBD	TBD	ps per 100mV
Derating factor for hold times	TBD	TBD	TBD	TBD	TBD	ps per 100mV

Synchronous Output Slew Rate

The output slew rate is tested using the following setup with only one die per I/O channel.

Table 24: Test Conditions for Output Slew Rate

Parameter	Value
Rising Edge	V_{IL} (DC) to V_{IH} (AC)
Falling Edge	V_{IH} (DC) to V_{IL} (AC)
Output Capacitive Load (C_{LOAD})	5pF
Temperature Range	T_A

Table 25: Output Slew Rate (VccQ = 1.7–1.95V)

Output Drive Strength	Min	Max	Unit
Overdrive 2	1	5.5	V/ns
Overdrive 1	0.85	5	V/ns
Nominal	0.75	4	V/ns
Underdrive	0.6	4	V/ns

Electrical Characteristics

Stresses greater than those listed under "Absolute Maximum Ratings" can cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not guaranteed. Exposure to absolute maximum rating conditions for extended periods can affect reliability.

Table 26: Absolute Maximum Ratings by Device

Parameter	Symbol	Min[1]	Max[1]	Unit
Voltage input	V_{IN}	-0.6	4.6	V
V_{CC} supply voltage	V_{CC}	-0.6	4.6	V
V_{CCQ} supply voltage	V_{CCQ}	-0.6	4.6	V
Storage temperature	T_{STG}	-65	150	°C

Notes: 1. Voltage on any pin relative to V_{SS}.

Table 27: Recommended Operating Conditions

Parameter		Symbol	Min	Typ	Max	Unit
Operating temperature	Commercial	T_A	0	–	70	°C
	Industrial		–40	–	+85	
V_{CC} supply voltage		V_{CC}	2.7	3.3	3.6	V
V_{CCQ} supply voltage (1.8V)		V_{CCQ}	1.7	1.8	1.95	V
V_{CCQ} supply voltage (3.3V)			2.7	3.3	3.6	V
V_{SS} ground voltage		V_{SS}	0	0	0	V

Table 28: Asynchronous Device DC and Operating Characteristics

Parameter	Conditions	Symbol	Min[1]	Typ[1]	Max[1]	Unit
Array read current	–	I_{CC1_a}	–	20	50	mA
Array program current	–	I_{CC2_a}	–	20	50	mA
Array erase current	–	I_{CC3_a}	–	20	50	mA
I/O burst read current	$^{t}RC = {}^{t}RC$ (MIN); Iout = 0mA	Icc4r_a	–	TBD	TBD	mA
I/O burst write current	$^{t}WC = {}^{t}WC$ (MIN)	Icc4w_a	–	TBD	TBD	mA
Bus idle current	–	Icc5_a	–	TBD	TBD	mA
Standby current (CMOS)	CE# = V_{CCQ} - 0.2V; WP# = 0V/V_{CC}	I_{SB_a}	–	10	50	µA

Notes: 1. All values are per LUN unless otherwise specified.

Table 29: Synchronous Device DC and Operating Characteristics

Parameter	Conditions	Symbol	Min[1]	Typ[1]	Max[1]	Unit
Array read current	$^{t}CK = {}^{t}CK$ (MIN)	ICC1_S	–	20	50	mA
Array program current	$^{t}CK = {}^{t}CK$ (MIN)	ICC2_S	–	20	50	mA
Array erase current	$^{t}CK = {}^{t}CK$ (MIN)	ICC3_S	–	20	50	mA
I/O burst read current	$^{t}CK = {}^{t}CK$ (MIN); Iout = 0mA	Icc4r_s	–	TBD	TBD	mA
I/O burst write current	$^{t}CK = {}^{t}CK$ (MIN)	Icc4w_s	–	TBD	TBD	mA
Bus idle current	$^{t}CK = {}^{t}CK$ (MIN)	Icc5_s	–	TBD	TBD	mA
Standby current (CMOS)	CE# = VCCQ - 0.2V; WP# = 0V/VCC	ISB_S	–	10	50	µA

Notes: 1. All values are per LUN unless otherwise specified.

Table 30: Ball Capacitance: BGA-100 Package

Description	Symbol	SDP[4]			Unit	Notes
		Min	Typ	Max		
Input capacitance (CLK)	CCK	3.35	3.6	3.85	pF	1, 2, 3
Input capacitance (ALE, CLE, W/R#)	CIN	3.5	4	4.5	pF	1, 2, 3
Input/output capacitance (DQ[7:0], DQS)	CIO	4	4.5	5	pF	1, 2, 3
Input capacitance (CE#, WP#)	COTHER	–	–	5	pF	1, 2
Delta clock capacitance	DCCK	–	–	0.25	pF	1, 2
Delta input capacitance	DCIN	–	–	0.5	pF	1, 2
Delta input/output capacitance	DCIO	–	–	0.5	pF	1, 2

Notes:
1. Verified in device characterization; not 100 percent tested.
2. Test conditions: TA = 25ºC, f = 100MHz, VIN = 0V.
3. Values for CCK, CIN and CIO (typ) are estimates.
4. SDP = Single die pacakge.

Table 31: Pin Capacitance: TSOP-48 Package

Description	Symbol	Device[2]	Max	Unit	Notes
Input/output capacitance ALE, CE#, CLE, R/B#, RE#, WE#, WP#	Cin/Cout	SDP	10	pF	1
Input/output capacitance (I/O[7:0], DQ[7:0])	Cin/Cout	SDP	5	pF	1

Notes:
1. These parameters are verified in device characterization and are not 100 percent tested.Test conditions: T_c = 25°C; f = 1 MHz; VIN = 0V.
2. SDP = Single die package..

Table 32: Pad Capacitance: LGA-52 Package

Description	Symbol	Device[2]	Max	Unit	Notes
Input/output capacitance ALE, CE#, CLE, R/B#, RE#, WE#, WP#	Cin/Cout	SDP	10	pF	1
Input/output capacitance I/O[7:0]	Cin/Cout	SDP	5	pF	1

Notes:
1. These parameters are verified in device characterization and are not 100 percent tested. Test conditions: T_c = 25°C; f = 1 MHz; V_{IN} = 0V.
2. SDP = Single die package.

Table 33: Test Conditions

Parameter	Value	Notes
Input pulse levels	0V to V_{CCQ}	–
Input rise and fall slew rates	1V/ns	–
Input and output timing levels	V_{CCQ}/2	–
Output load: Synchronous interface, nominal output drive strength	C_L = 5pF	1, 2
Output load: Asynchronous interface, nominal output drive strength (V_{CCQ} = 1.7–1.95V)	C_L = 30pF	2
Output load: Asynchronous interface, nominal output drive strength (V_{CCQ} = 2.7–3.6V)	C_L = 50pF	2

Notes:
1. Transmission line delay is assumed to be very small.
2. This test setup applies to all package configurations.

Table 34: 3.3V VccQ Device Operating Characteristics

Parameter	Condition	Symbol	Min	Typ	Max	Unit	Notes
AC input high voltage	CE#, DQ[7:0], DQS, DQS#, ALE, CLE, CLK (WE#), CLK#, W/R# (RE#), WP#	VIH (AC)	0.8 × VccQ	–	VccQ + 0.3	V	–
AC input low voltage		VIL (AC)	–0.3	–	0.2 × VccQ	V	–
Output high voltage	IOH = –400ìA	VOH	0.67 × VccQ	–	–	V	–
Output low voltage	IOL = 2.1mA	VOL	–	–	0.4	V	–
Input leakage current	Any input VIN = 0V to VCCQ (all other pins under test=0V)	ILI	–	–	±10	µA	1
Output leakage current	I/Os are disabled; VOUT = 0V to VCCQ	ILO	–	–	±10	µA	1
Output low current (R/B#)	VOL = 0.4V	IOL (R/B#)	8	10	–	mA	2

Notes:
1. All leakage currents are per LUN.
2. DC characteristics may need to be relaxed if R/B# pull-down strength is not set to “Full.” See Table 13 on page 14 for additional details.

Table 35: 1.8V VccQ Device Operating Characteristics

Parameter	Condition	Symbol	Min	Typ	Max	Unit	Notes
AC input high voltage	CE#, DQ[7:0], DQS, ALE, CLE, CLK (WE#), W/R# (R/E#), WP#	V_{IH} (AC)	0.8 × V_{CCQ}	–	V_{CCQ} + 0.3	V	–
AC input low voltage		V_{IL} (AC)	-0.3	–	0.2 × V_{CCQ}	V	–
DC input high voltage	DQ[7:0], DQS, ALE, CLE, CLK (WE#), W/R# (R/E#)	V_{IH} (DC)	0.7 × V_{CCQ}	–	V_{CCQ} + 0.3	V	1
DC input low voltage		V_{IL} (DC)	-0.3	–	0.3 × V_{CCQ}	V	1
Output high voltage	I_{OH} = -100µA	V_{OH}	V_{CCQ} - 0.1	–	–	V	2
Output low voltage	I_{OL} = -100µA	V_{OL}	–	–	0.1	V	2
Input leakage current	Any input V_{IN} = 0V to V_{CCQ} (all other pins under test = 0V)	I_{LI}	–	–	±10	µA	3
Output leakage current	I/Os are disabled; V_{OUT} = 0V to V_{CCQ}	I_{LO}	–	–	±10	µA	3
Output low current (R/B#)	V_{OL} = 0.2V	I_{OL} (R/B#)	3	4	–	mA	–

Notes:
1. The DC values only apply to the synchronous interface.
2. V_{OH} and V_{OL} only apply to the asynchronous interface.
3. All leakage currents are per LUN.

Table 36: AC Characteristic: Synchronous Command, Address, and Data

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Clock Period		50		30		20		15		12		ns	–
Frequency		≈20		≈33		≈50		≈67		≈83		MHz	–
Access window of DQ[7:0] from CLK	^{t}AC	–	20	–	20	–	20	–	20	–	20	ns	–
ALE to data loading time	^{t}ADL	100	–	100	–	70	–	70	–	70	–	ns	–
Cmd, Addr, Data delay	^{t}CAD	25	–	25	–	25	–	25	–	25	–	ns	1
ALE, CLE, W/R# hold	^{t}CALH	10	–	5	–	4	–	3	–	2.5	–	ns	–
ALE, CLE, W/R# setup	^{t}CALS	10	–	5	–	4	–	3	–	2.5	–	ns	–
DQ hold - Cmd, Addr	^{t}CAH	10	–	5	–	4	–	3	–	2.5	–	ns	–
DQ setup - Cmd, Addr	^{t}CAS	10	–	5	–	4	–	3	–	2.5	–	ns	–
Change column setup to data in/out or next command	^{t}CCS	200	–	200	–	200	–	200	–	200	–	ns	2
CE# hold	^{t}CH	10	–	5	–	4	–	3	–	2.5	2	ns	–
Average CLK cycle time	^{t}CK (avg)	50	100	30	50	20	30	15	20	12	15	ns	3
Absolute CLK cycle time, from rising edge rising edge	^{t}CK (abs)	^{t}CK (abs) MIN = ^{t}CK (avg) + ^{t}JIT(per) MIN ^{t}CK (abs) MAX = ^{t}CK (avg) + ^{t}JIT(per) MAX										ns	
CLK cycle HIGH	^{t}CKH (abs)	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	^{t}CK	4
CLK cycle LOW	^{t}CKL (abs)	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	^{t}CK	4
Data output end to W/R# HIGH	^{t}CKWR	^{t}CKWR(MIN) = RoundUp[^{t}DQSCK(MAX) + ^{t}CK) / ^{t}CK] ^{t}CKWR(MAX): -										^{t}CK	–
CE# setup	^{t}CS	35	–	25	–	15	–	15	–	15	–	ns	–
Data In hold	^{t}DH	5	–	2.5	–	1.7	–	1.3	–	1.1	–	ns	–
Access window of DQS from CLK	^{t}DQSCK	–	20	–	20	–	20	–	20	–	20	ns	–
DQS, DQ[7:0] Driven by NAND	^{t}DQSD	0	20	0	20	0	20	0	20	0	20	ns	–
DQS, DQ[7:0] to tri-state	^{t}DQSHZ	–	20	–	20	–	20	–	20	–	20	ns	5
DQS input high pulse width	^{t}DQSH	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	^{t}CK	–
DQS input low pulse width	^{t}DQSL	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	^{t}CK	–
DQS-DQ skew	^{t}DQSQ	–	5	–	2.5	–	1.7	–	1.3	–	1.1	ns	–
Data input	^{t}DQSS	0.75	1.25	0.75	1.25	0.75	1.25	0.75	1.25	0.75	1.25	^{t}CK	–
Data In setup	^{t}DS	5	–	3	–	2	–	1.5	–	1.1	–	ns	–

Table 36: AC Characteristic: Synchronous Command, Address, and Data (continued)

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
DQS falling edge from CLK rising - hold	tDSH	0.2	–	0.2	–	0.2	–	0.2	–	0.2	–	tCK	–
DQS falling to CLK rising - setup	tDSS	0.2	–	0.2	–	0.2	–	0.2	–	0.2	–	tCK	–
Data Valid Window	tDVW	tDVW = tOH - tDQSQ										ns	–
Half Clock Period	tHP	tHP = Min(tCKH, tCKL)										ns	–
The deviation of a given tCK(abs) from tCK(avg)	tJIT(per)	-0.7	0.7	-0.7	0.7	-0.7	0.7	-0.6	0.6	-0.6	0.6	ns	
DQ-DQS hold, DQS to first DQ to go non-valid, per access	tQH	tQH = tHP - tQHS										ns	–
Data Hold Skew Factor	tQHS	–	6	–	3	–	2	–	1.5	–	1.2	ns	–
Data output to command, address, or data input	tRHW	100	–	100	–	100	–	100	–	100	–	ns	–
Ready to data output	tRR	20	–	20	–	20	–	20	–	20	–	ns	–
Device reset time (Read/Program/Erase)	tRST	–	5/10/500	–	5/10/500	–	5/10/500	–	5/10/500	–	5/10/500	µs	6
CLK high to R/B# low	tWB	–	100	–	100	–	100	–	100	–	100	ns	–
Command cycle to data output	tWHR	80	–	60	–	60	–	60	–	60	–	ns	–
DQS write preamble	tWPRE	1.5	–	1.5	–	1.5	–	1.5	–	1.5	–	tCK	–
DQS write postamble	tWPST	1.5	–	1.5	–	1.5	–	1.5	–	1.5	–	tCK	–
W/R# LOW to data output cycle	tWRCK	20	–	20	–	20	–	20	–	20	–	ns	–
WP# transition to command cycle	tWW	100	–	100	–	100	–	100	–	100	–	ns	–

Notes:
1. Delay is from start of command to next command, address, or data cycle; start of address to next command, address, or data cycle; and end of data to start of next command, address, or data cycle.
2. This value is specified in the parameter page.
3. tCK(avg) is the average clock period over any consecutive 200-cycle window.
4. tCKH(abs) and tCKL(abs) include static offset and duty cycle jitter.
5. tDQSHZ begins when W/R# is latched HIGH by CLK. This parameter is not referenced to a specific voltage level; it specifies when the device outputs are no longer driving.
6. If RESET (FFh) is issued when the target is idle, the target goes busy for a maximum of 5µs.

Table 37: AC Characteristics: Asynchronous Command, Address, and Data

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Clock Period		100		50		35		30		25		ns	

Table 37: AC Characteristics: Asynchronous Command, Address, and Data (continued)

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Frequency		≈10		≈20		≈28		≈33		≈40		MHz	
ALE to data start	^{t}ADL	200	–	100	–	100	–	100	–	70	–	ns	1
ALE hold time	^{t}ALH	20	–	10	–	10	–	5	–	5	–	ns	
ALE setup time	^{t}ALS	50	–	25	–	15	–	10	–	10	–	ns	
ALE to RE# delay	^{t}AR	25	–	10	–	10	–	10	–	10	–	ns	
CE# access time	^{t}CEA	–	100	–	45	–	30	–	25	–	25	ns	
Change column setup to data in/out or next command	^{t}CCS	200	–	200	–	200	–	200	–	200	–	ns	
CE# hold time	^{t}CH	20	–	10	–	10	–	5	–	5	–	ns	
CE# high to output high-Z	^{t}CHZ	–	100	–	50	–	50	–	50	–	30	ns	2
CLE hold time	^{t}CLH	20	–	10	–	10	–	5	–	5	–	ns	
CLE to RE# delay	^{t}CLR	20	–	10	–	10	–	10	–	10	–	ns	
CLE setup time	^{t}CLS	50	–	25	–	15	–	10	–	10	–	ns	
CE# high to output hold	^{t}COH	0	–	15	–	15	–	15	–	15	–	ns	
CE# setup time	^{t}CS	70	–	35	–	25	–	25	–	20	–	ns	
Data hold time	^{t}DH	20	–	10	–	5	–	5	–	5	–	ns	
Data setup time	^{t}DS	40	–	20	–	15	–	10	–	10	–	ns	
Output high-Z to RE# low	^{t}IR	10	–	0	–	0	–	0	–	0	–	ns	
RE# cycle time	^{t}RC	100	–	50	–	35	–	30	–	25	–	ns	
RE# access time	^{t}REA	–	40	–	30	–	25	–	20	–	20	ns	3
RE# high hold time	^{t}REH	30	–	15	–	15	–	10	–	10	–	ns	3
RE# high to output hold	^{t}RHOH	0	–	15	–	15	–	15	–	15	–	ns	3
RE# high to WE# low	^{t}RHW	200	–	100	–	100	–	100	–	100	–	ns	
RE# high to output high-Z	^{t}RHZ	–	200	–	100	–	100	–	100	–	100	ns	2, 3
RE# low to output hold	^{t}RLOH	0	–	0	–	0	–	0	–	5	–	ns	3
RE# pulse width	^{t}RP	50	–	25	–	17	–	15	–	12	–	ns	
Ready to RE# low	^{t}RR	40	–	20	–	20	–	20	–	20	–	ns	
Device reset time (Read/Program/Erase)	^{t}RST	–	5/10/500	–	5/10/500	–	5/10/500	–	5/10/500	–	5/10/500	µs	4, 5
WE# high to R/B# low	^{t}WB	–	200	–	100	–	100	–	100	–	100	ns	6
WE# cycle time	^{t}WC	100	–	45	–	35	–	30	–	25	–	ns	
WE# high hold time	^{t}WH	30	–	15	–	15	–	10	–	10	–	ns	
WE# high to RE# low	^{t}WHR	120	–	80	–	80	–	60	–	60	–	ns	
WE# pulse width	^{t}WP	50	–	25	–	17	–	15	–	12	–	ns	

Table 37: AC Characteristics: Asynchronous Command, Address, and Data (continued)

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
WP# transition to WE# low	^{t}WW	100	–	100	–	100	–	100	–	100	–	ns	

Notes:
1. Timing for ^{t}ADL begins in the ADDRESS cycle, on the final rising edge of WE# and ends with the first rising edge of WE# for data input.
2. Data transition is measured ±200mV from steady-steady voltage with load. This parameter is sampled and not 100 percent tested.
3. AC characteristics may need to be relaxed if output drive strength is not set to at least nominal.
4. If RESET (FFh) command is issued when the target is READY, the target goes busy for a maximum of 5µs.
5. See Table 39 for details on the power-on reset time, ^{t}POR
6. Do not issue a new command during ^{t}WB, even if R/B# or RDY is ready.

Table 38: Valid Blocks per LUN

Parameter	Symbol	Min	Max	Unit	Notes
Valid block number	NVB	2,008	2,048	Blocks	1

Notes:
1. Invalid blocks are block that contain one or more bad bits beyond ECC. The device may contain bad blocks upon shipment. Additional bad blocks may develop over time; however, the total number of available blocks will not drop below NVB during the endurance life of the device. Do not erase or program blocks marked invalid from the factory.

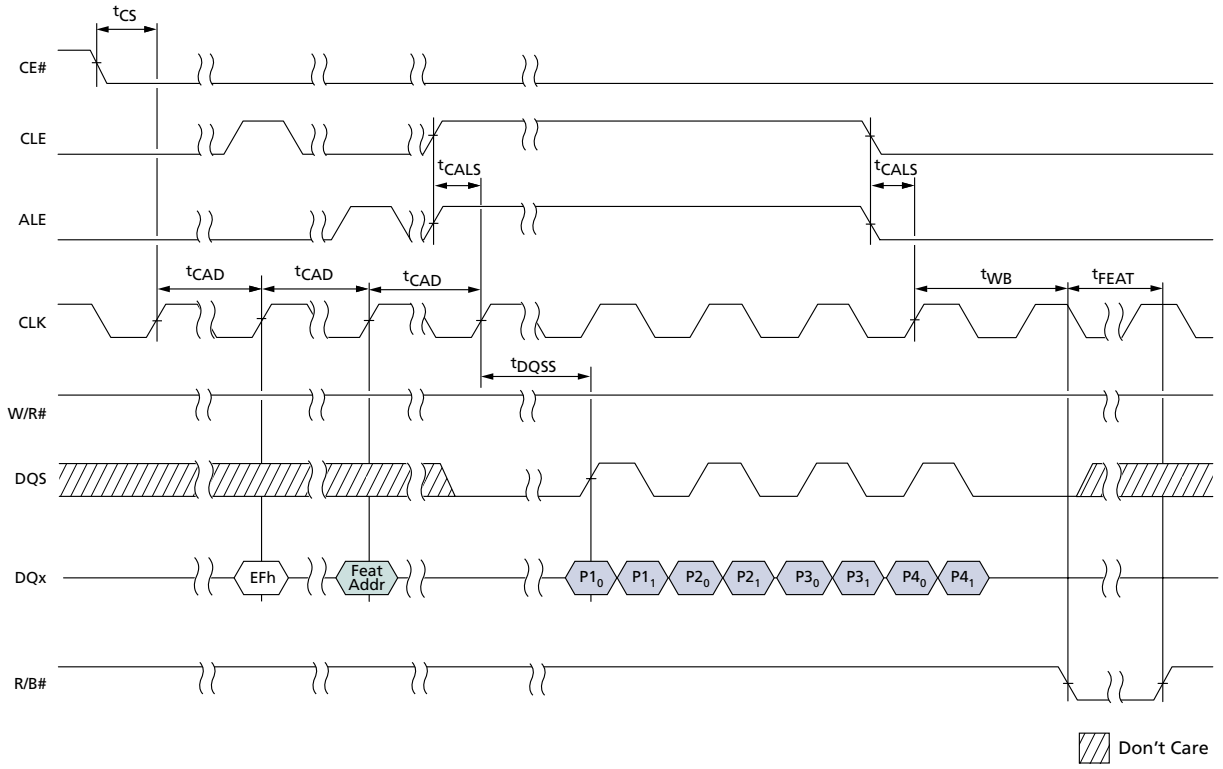
Table 39: Array Characteristics

Parameter	Symbol	Typ	Max	Unit	Notes
Number of partial page programs	NOP	–	4	Cycles	1
ERASE BLOCK operation time	^{t}BERS	0.7	3	ms	
Cache busy	^{t}CBSY	3	500	µs	
Dummy busy time	^{t}DBSY	0.5	1	µs	
Cache read busy time	^{t}RCBSY	3	25	µs	
Busy time for SET FEATURES and GET FEATURES operations	^{t}FEAT	–	1	µs	
Busy time for interface change	^{t}ITC	–	1	µs	2
LAST PAGE PROGRAM operation time	^{t}LPROG	–	–	µs	3
Busy time for OTP DATA PROGRAM operation if OTP is protected	^{t}OBSY	–	30	µs	
Power-on reset time	^{t}POR	–	1	ms	
PROGRAM PAGE operation time	^{t}PROG	200	500	µs	
READ PAGE operation time	^{t}R	–	25	µs	

Notes:
1. The pages in the OTP Block have an NOP of 8.
2. ^{t}ITC (MAX) is the busy time when the interface changes from asynchronous to synchronous using the SET FEATURES (EFh) command or synchronous to asynchronous using the RESET (FFh) command. During the ^{t}ITC time, any command, including READ STATUS (70h) and SELECT LUN WITH STATUS (78h), is prohibited.
3. ^{t}LPROG = ^{t}PROG (last page) + ^{t}PROG (last page - 1) - command load time (last page) - address load time (last page) - data load time (last page).

Timing Diagrams

Synchronous Interface



Notes:
1. When CE# remains LOW, tCAD begins at the rising edge of the clock from which the last data byte is input for the subsequent command or data input cycle(s).
2. tDSH (MIN) generally occurs during tDQSS (MIN).
3. tDSS (MIN) generally occurs during tDQSS (MAX).
4. The cycle that tCAD is measured from may be an idle cycle (as shown), another command cycle, and address cycle, or a data cycle. The idle cycle is shown in this diagram for simplicity.

Figure 63: READ ID Operation

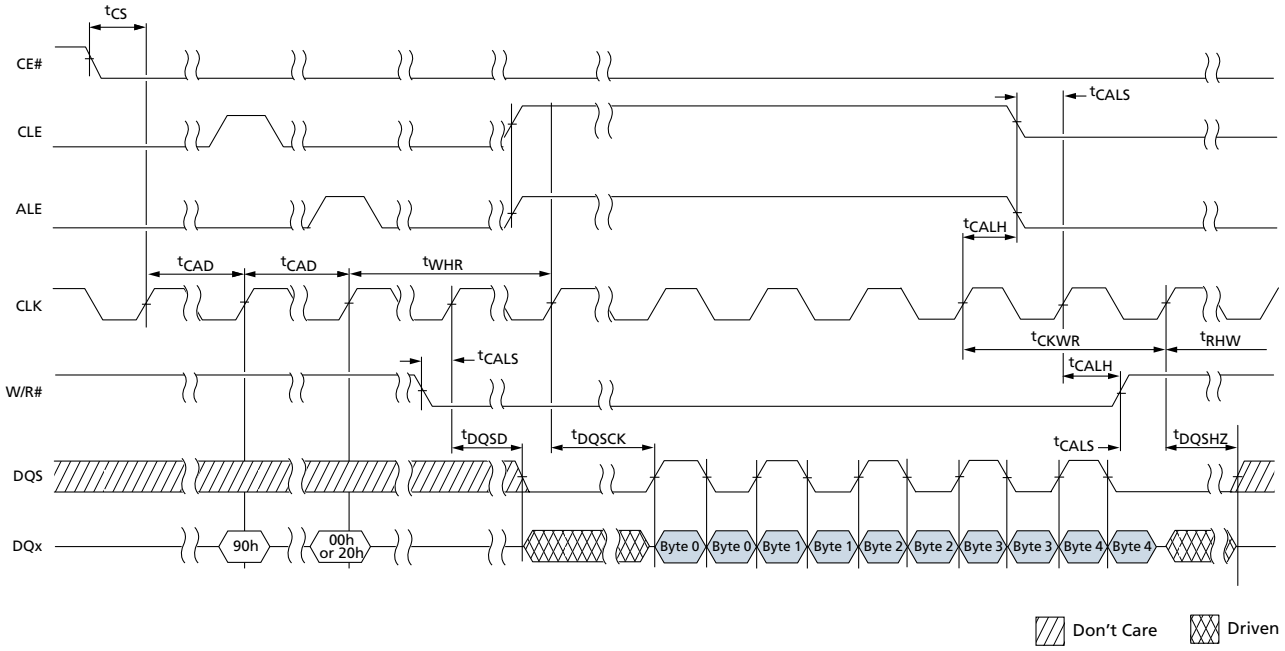


Figure 64: GET FEATURES Operation

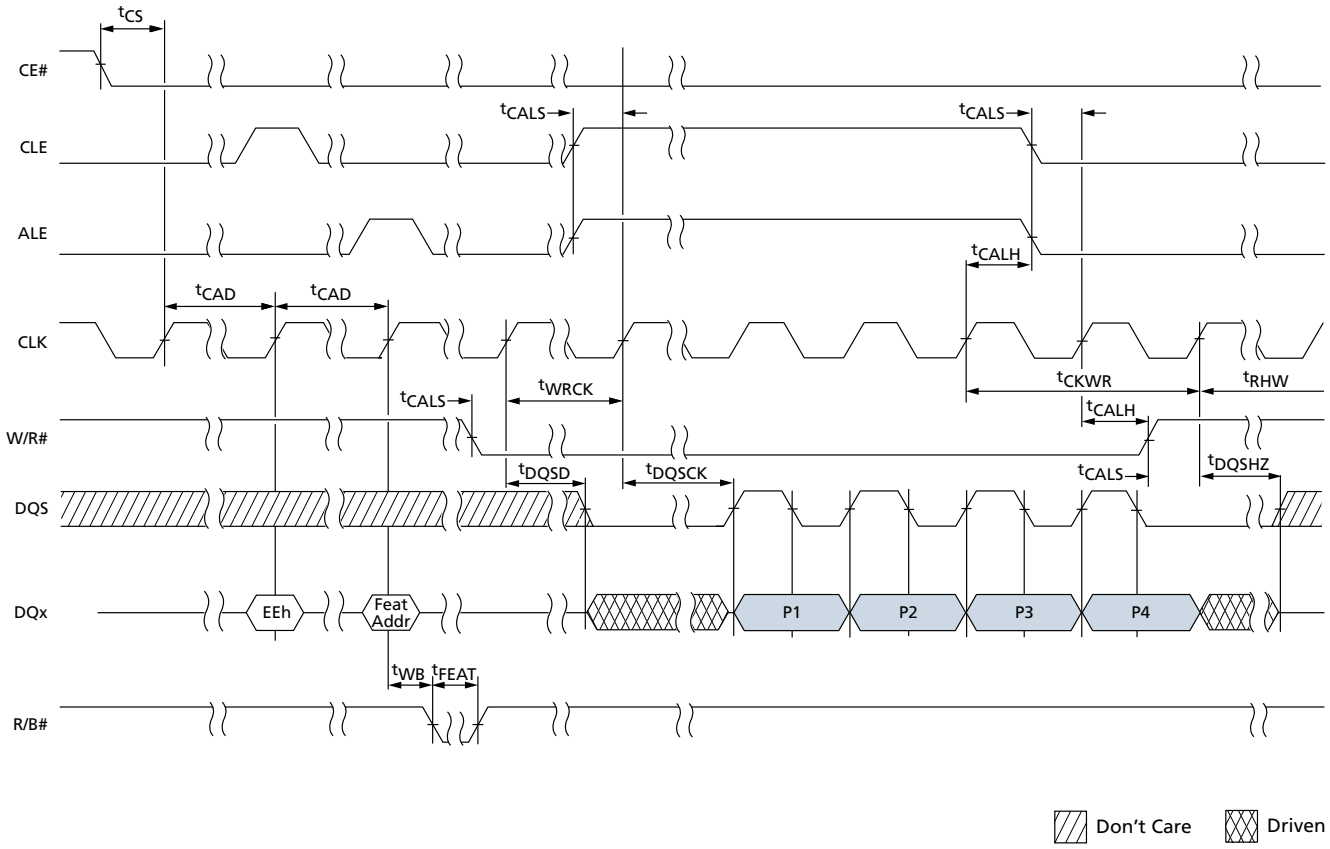


Figure 65: READ STATUS Cycle

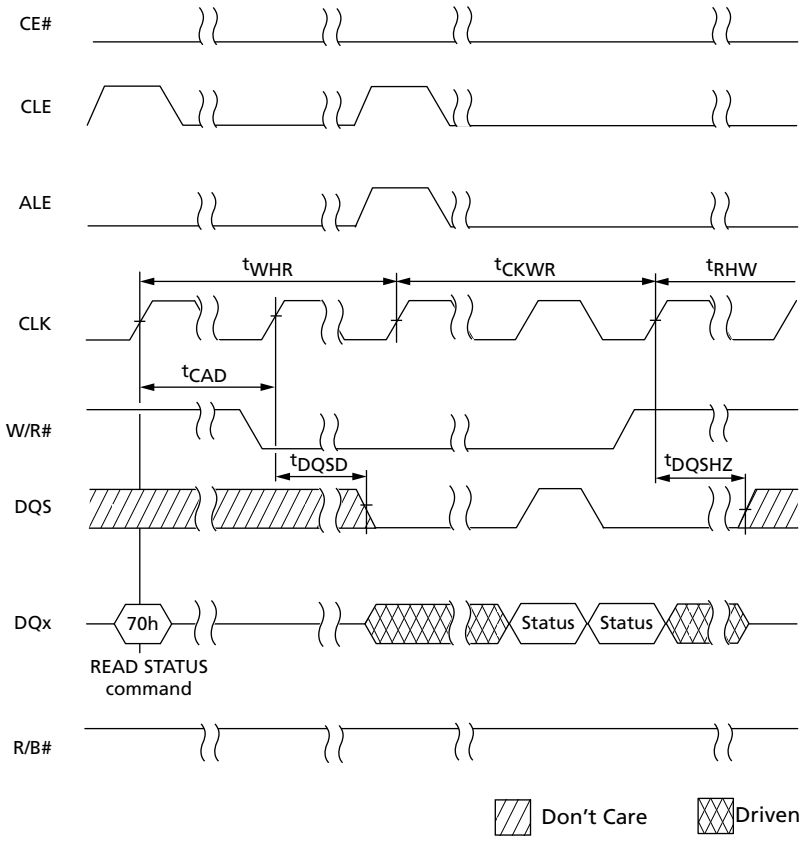


Figure 66: SELECT LUN with STATUS Operation

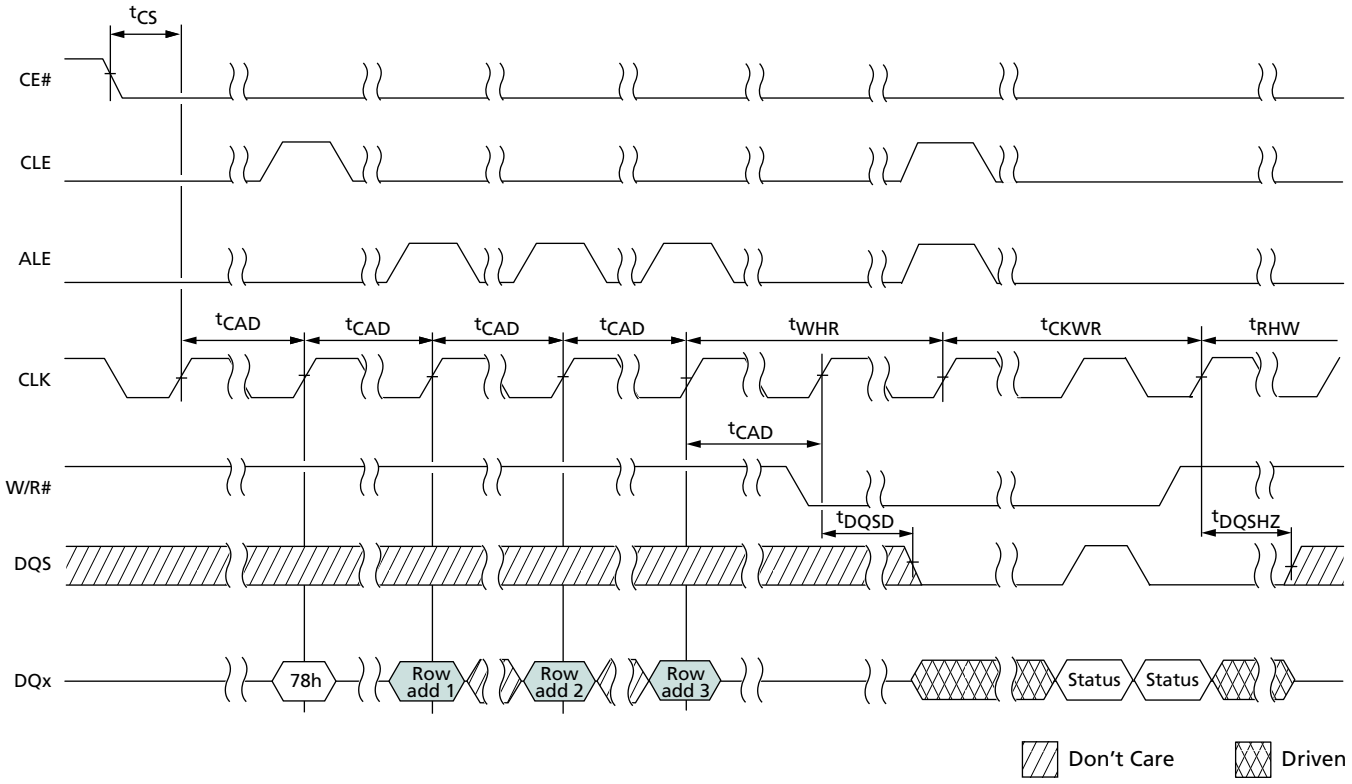


Figure 67: READ PARAMETER PAGE Operation

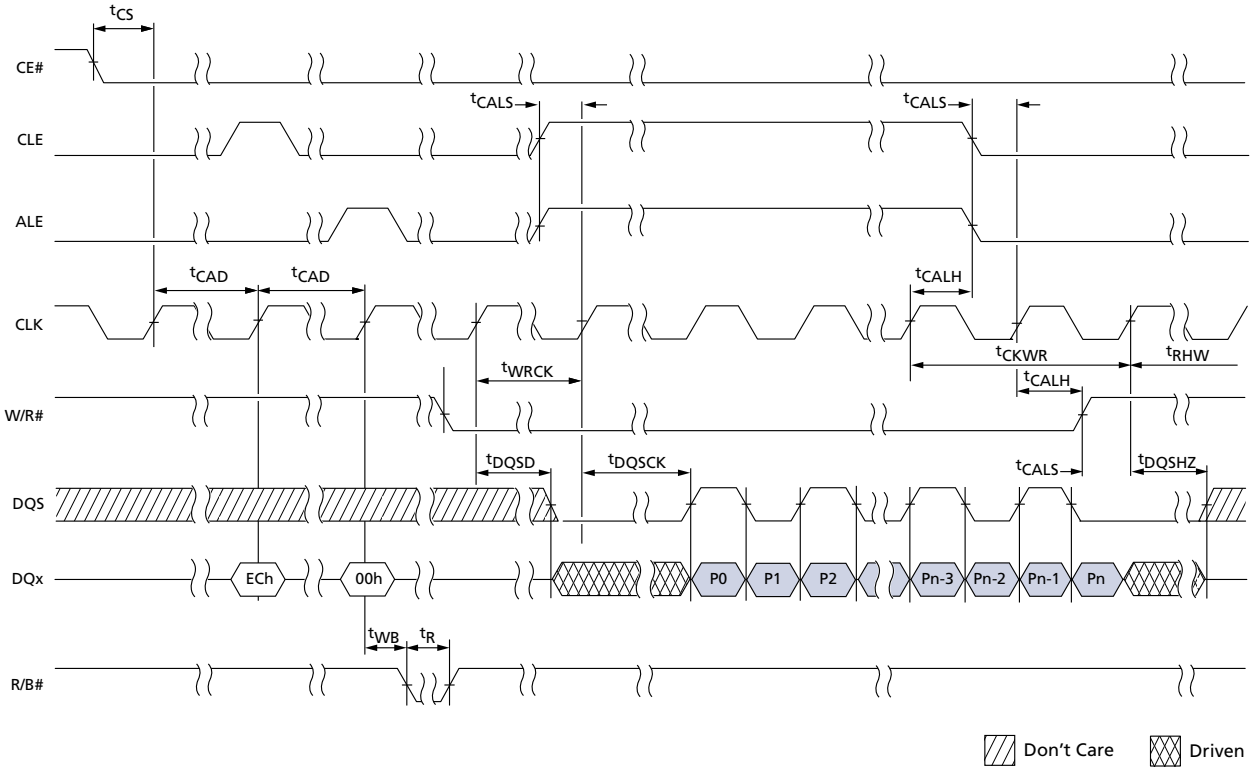


Figure 68: READ PAGE Operation

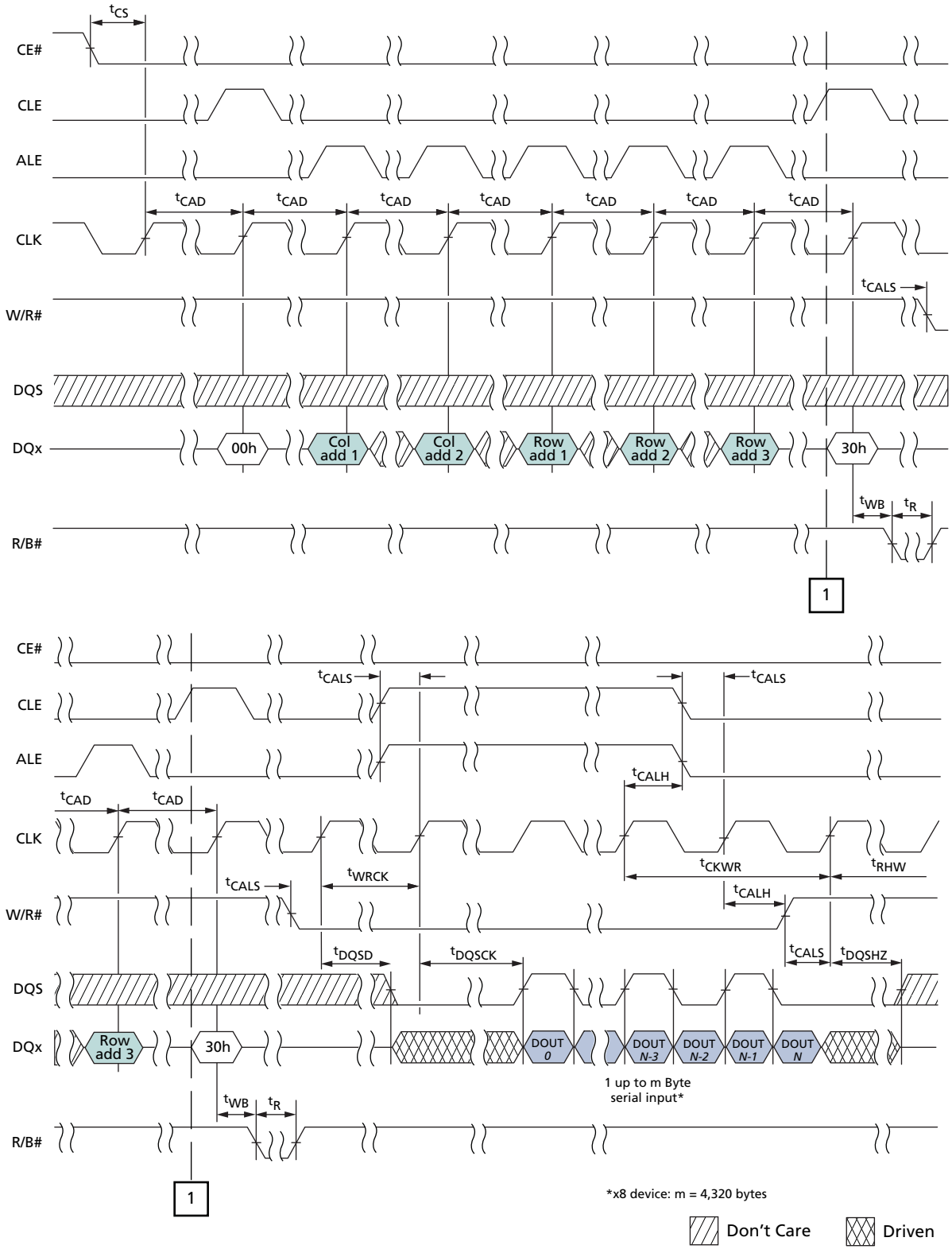


Figure 69: CHANGE READ COLUMN

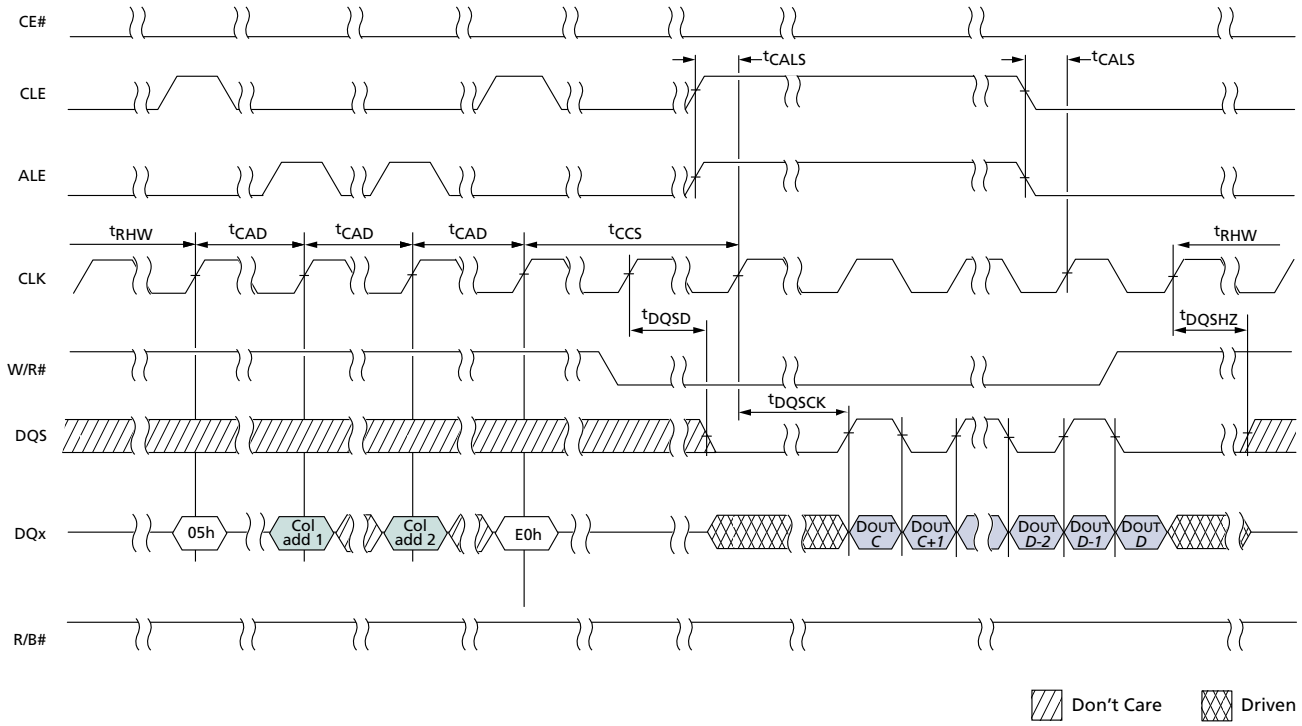


Figure 70: READ PAGE CACHE SEQUENTIAL (1 of 2)

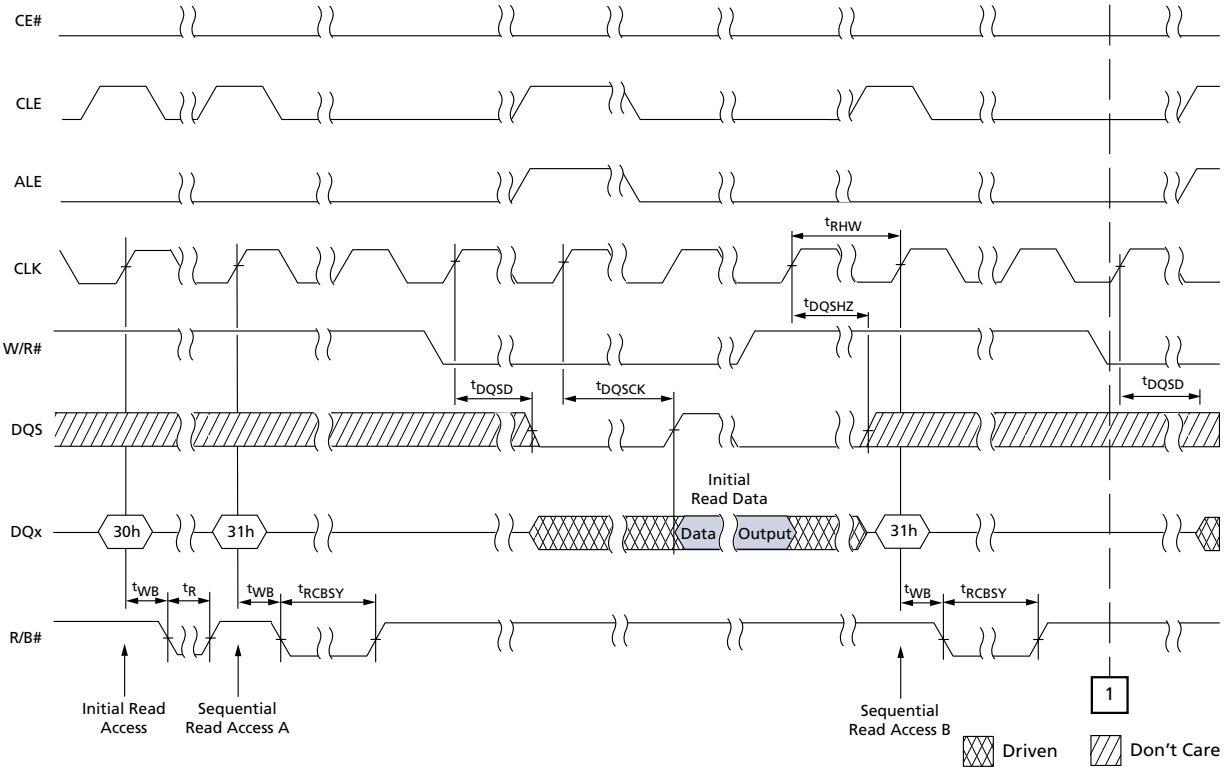


Figure 71: READ PAGE CACHE SEQUENTIAL (2 of 2)

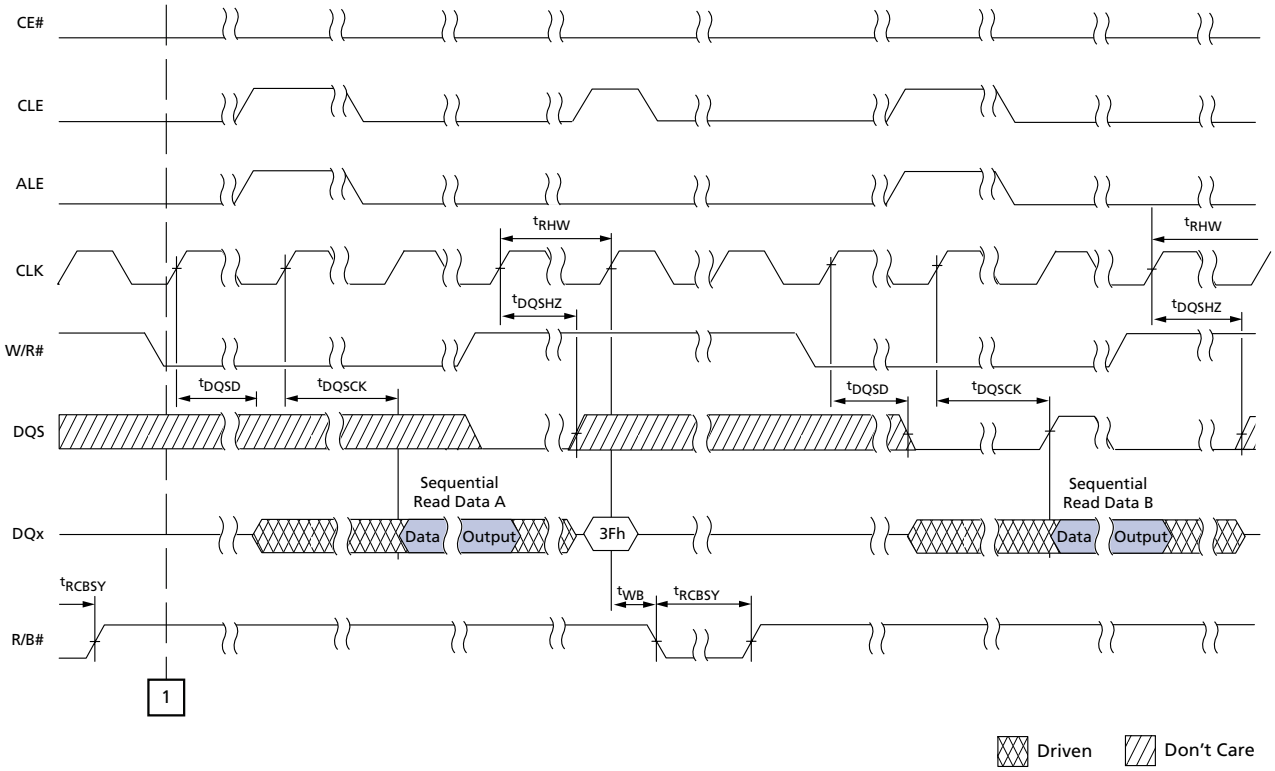


Figure 72: READ PAGE CACHE RANDOM (1 of 2)

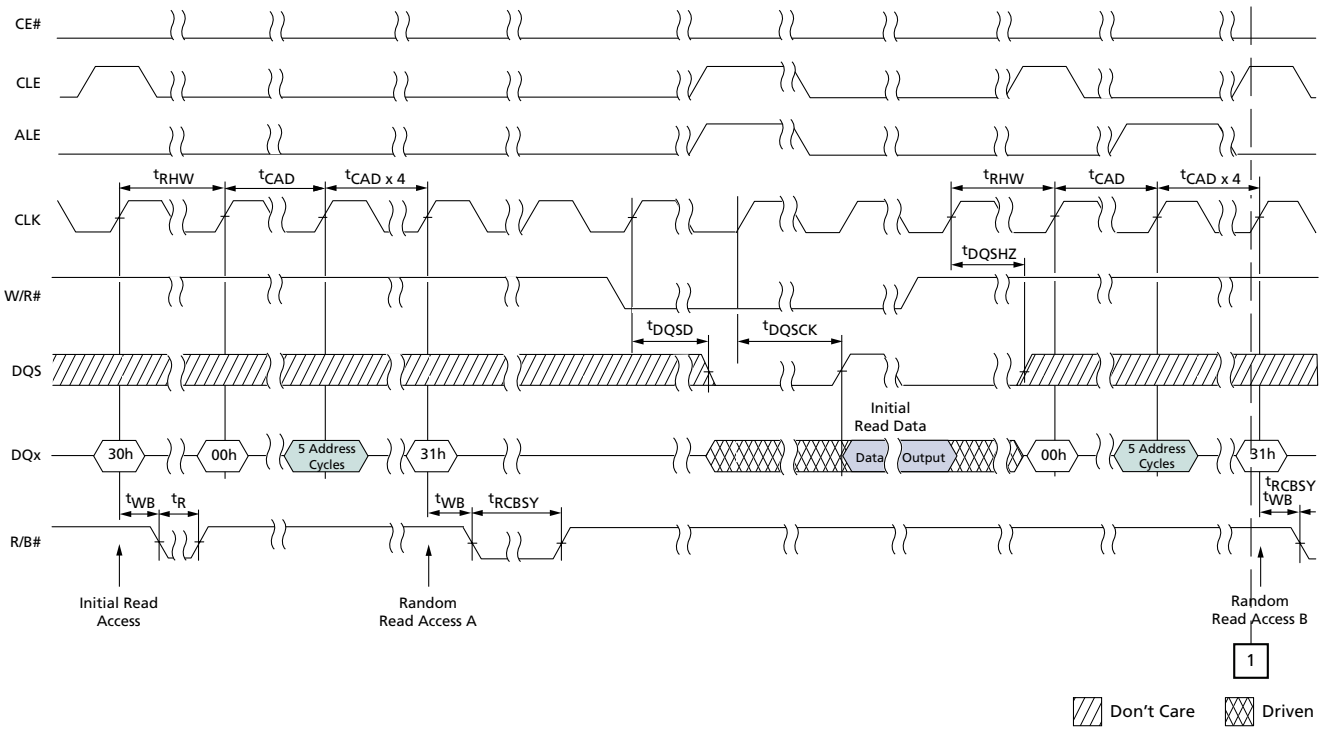


Figure 73: READ PAGE CACHE RANDOM (2 of 2)

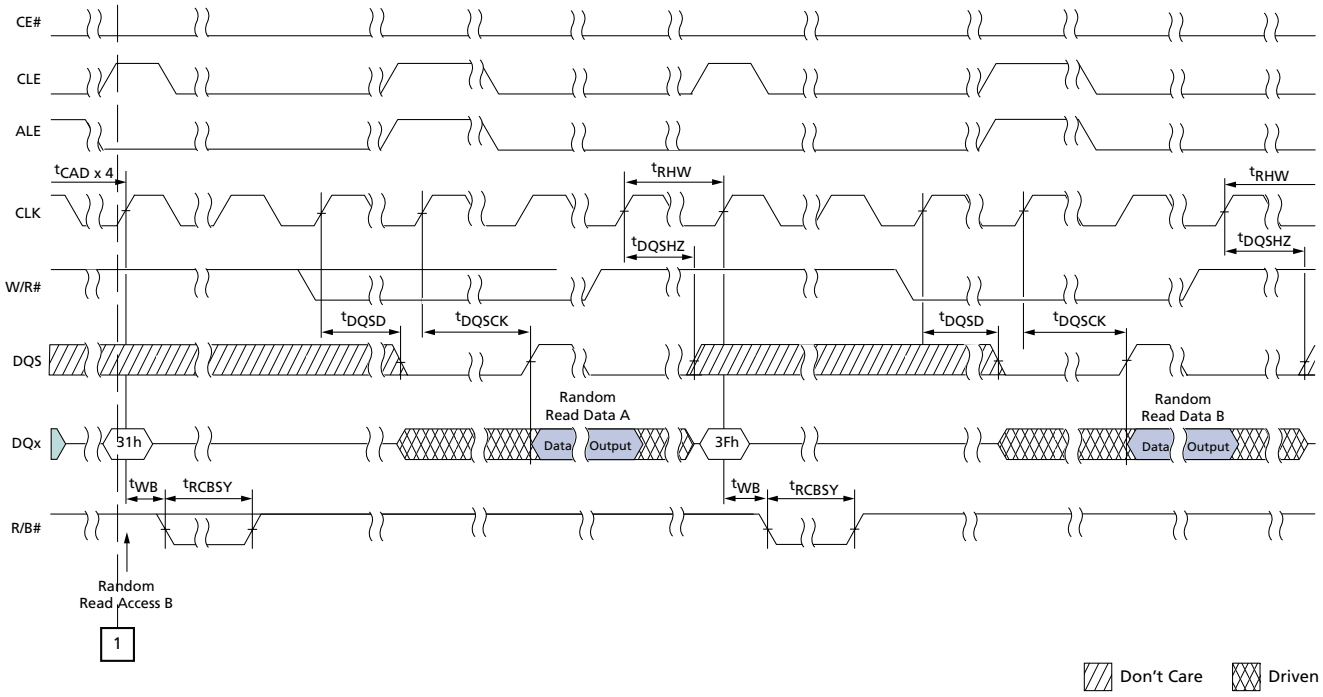


Figure 74: Multi-Plane Read Page (1 of 2)

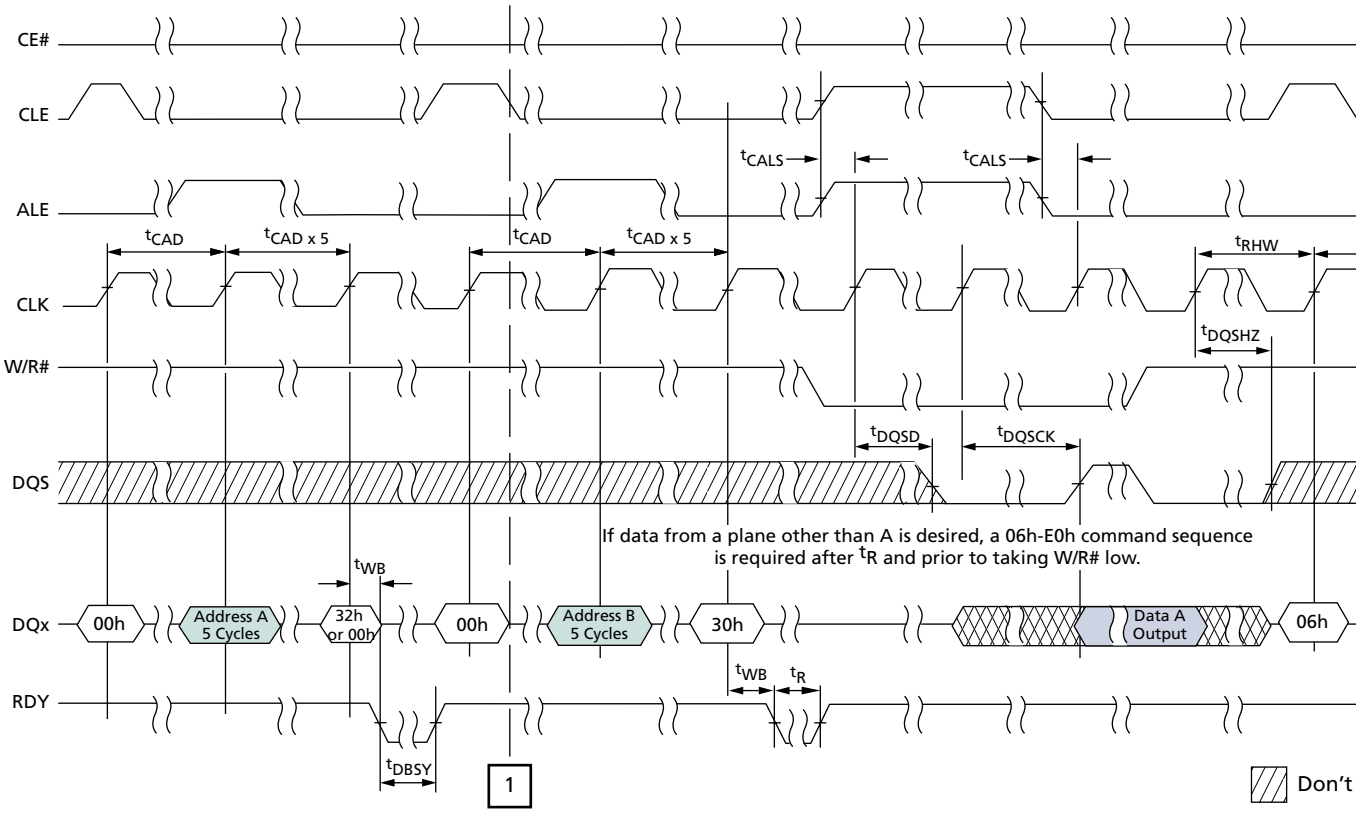


Figure 75: Multi-Plane Read Page (2 of 2)

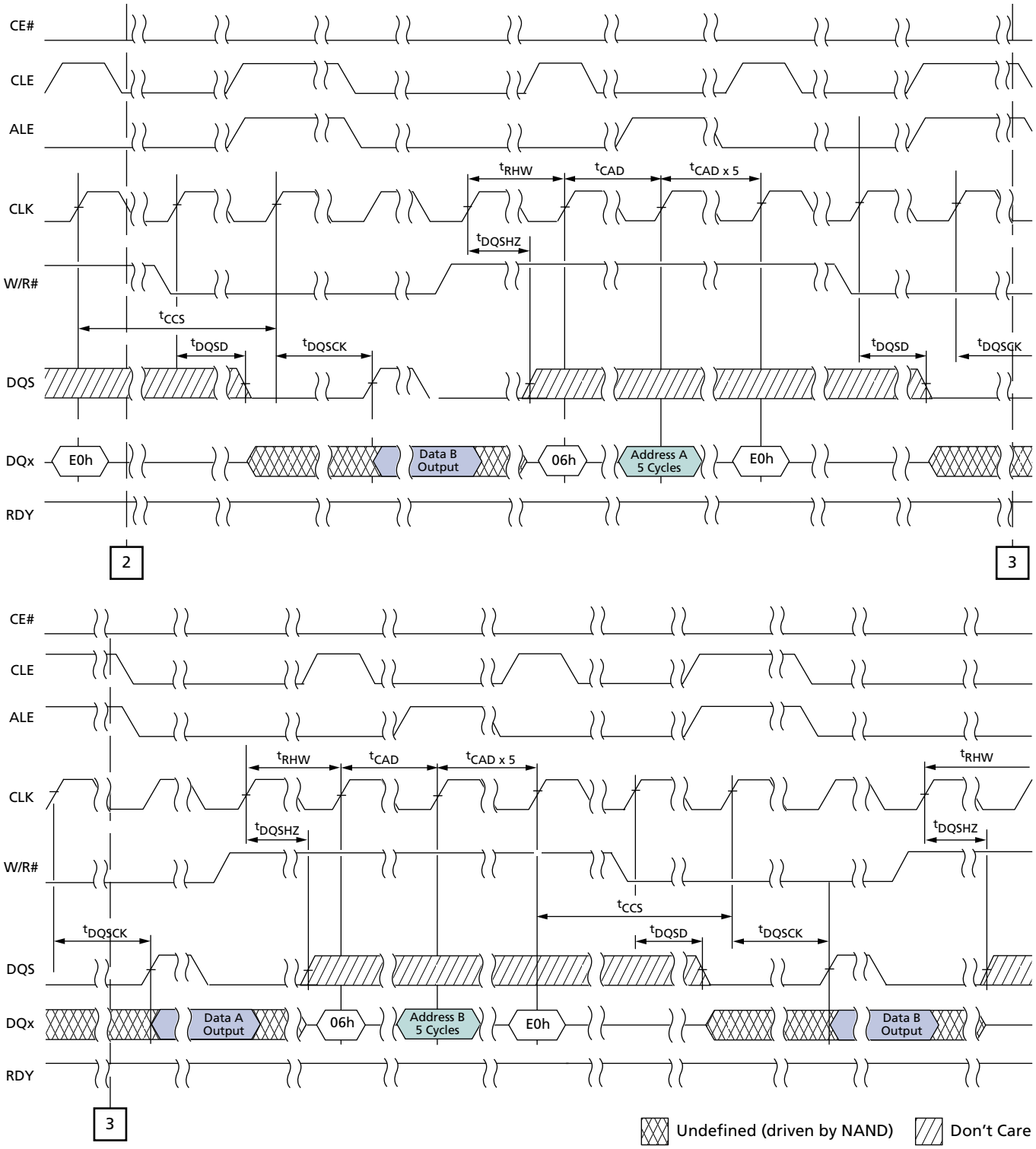


Figure 76: PROGRAM PAGE Operation (1 of 2)

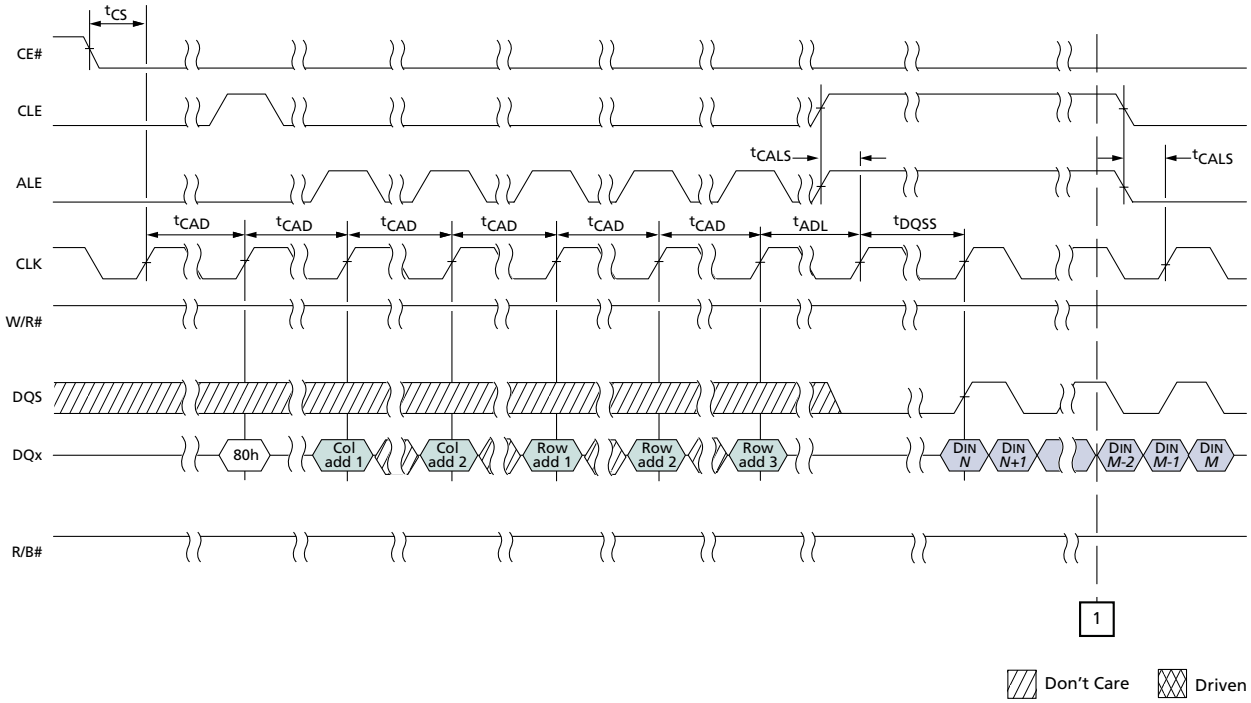


Figure 77: PROGRAM PAGE Operation (2 of 2)

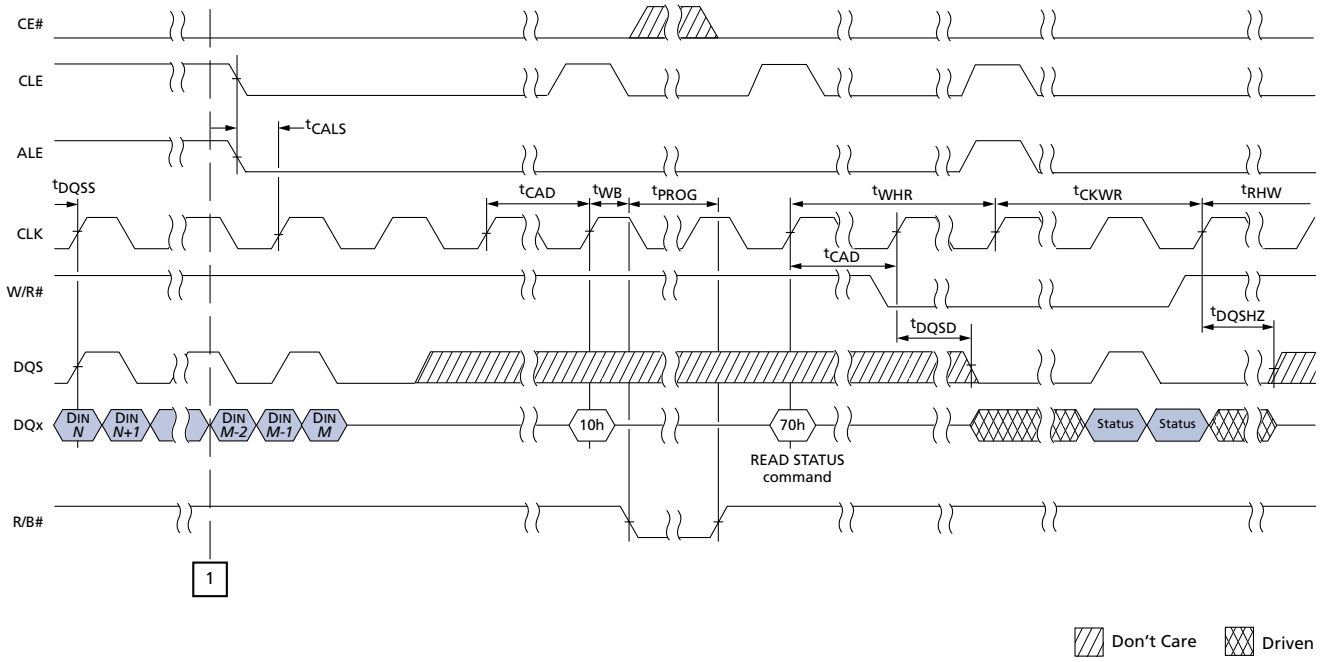


Figure 78: CHANGE WRITE COLUMN

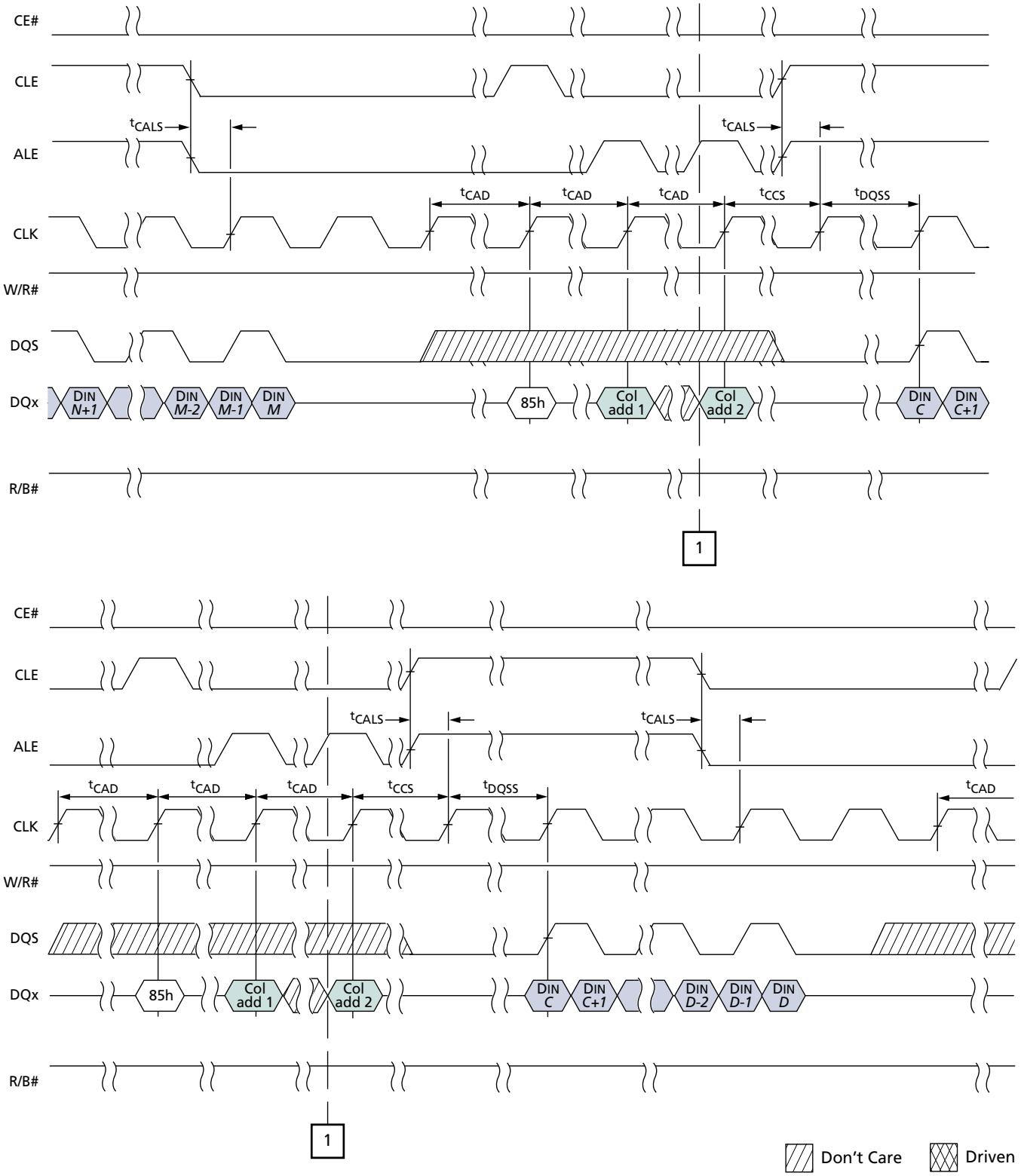


Figure 79: Multi-Plane Program Page

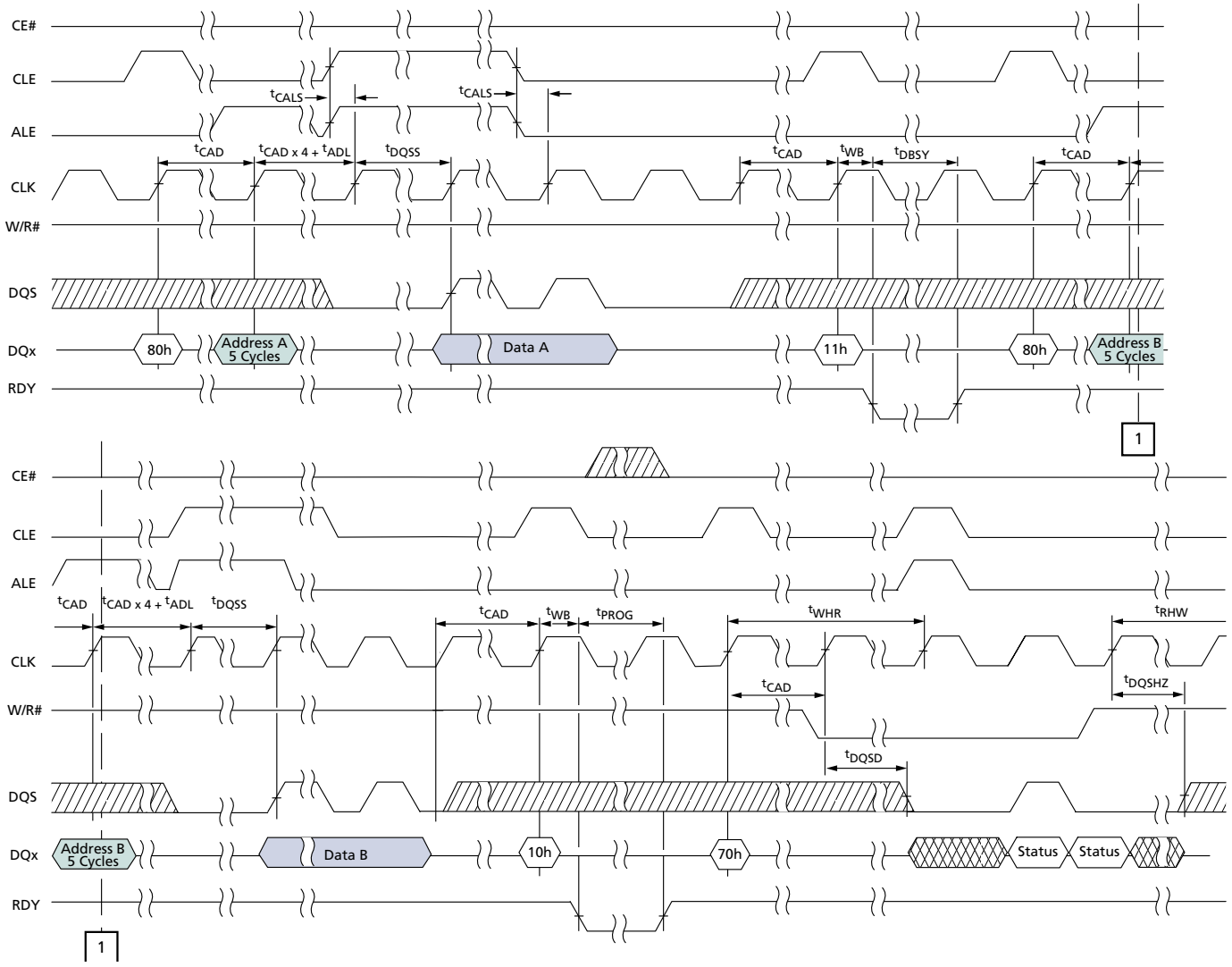


Figure 80: ERASE BLOCK

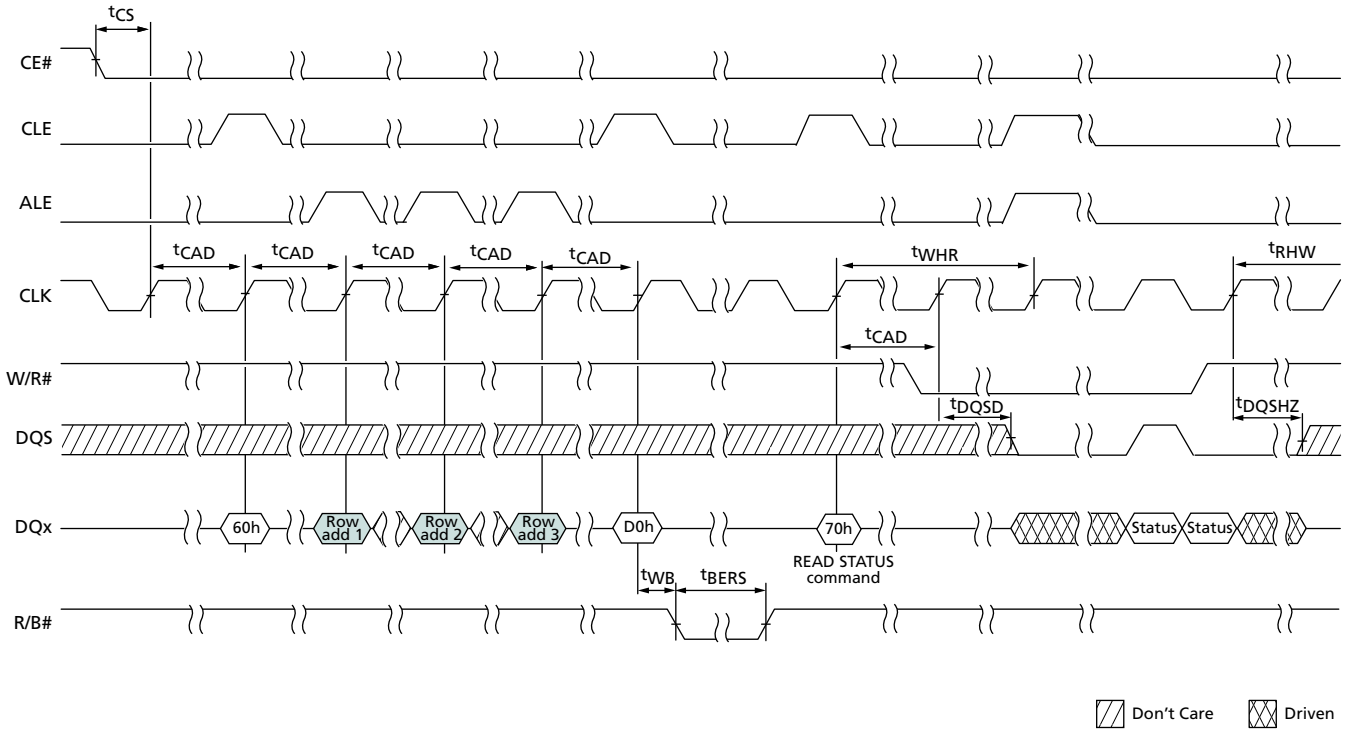


Figure 81: COPYBACK (1 of 3)

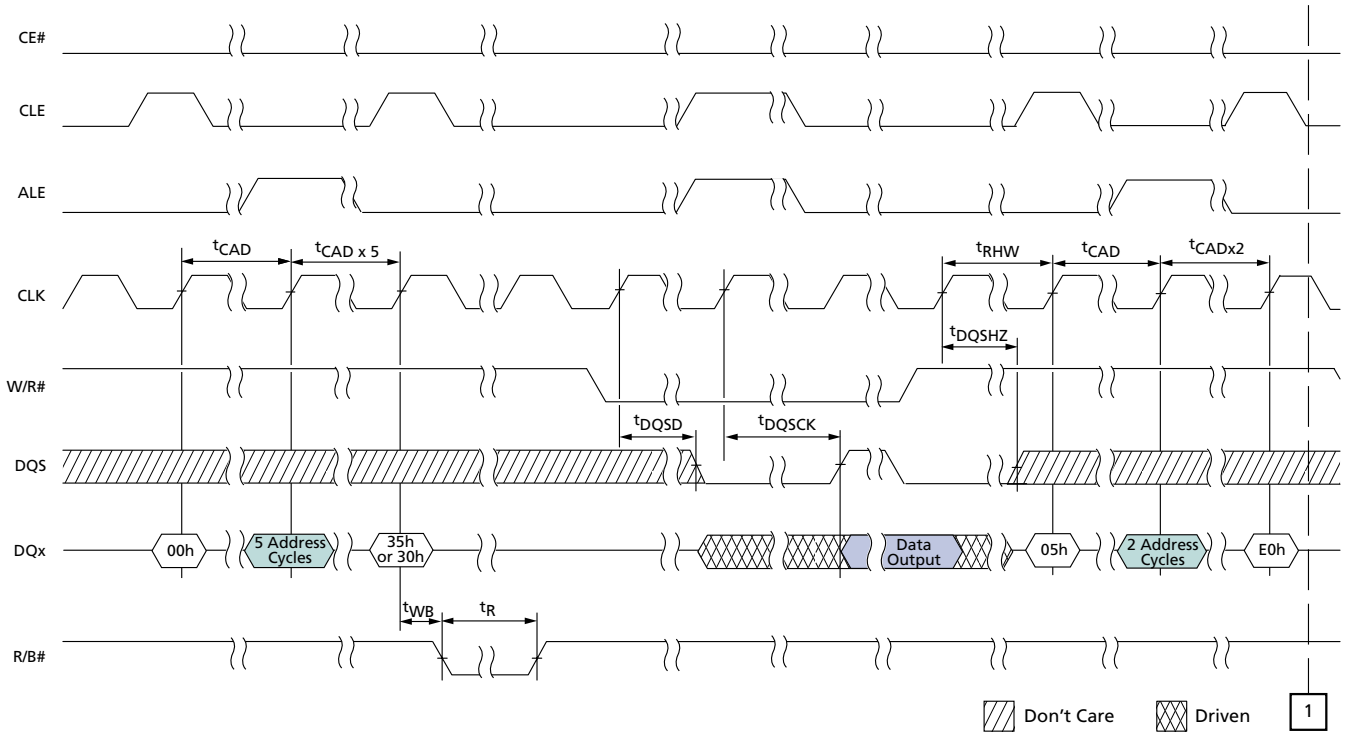


Figure 82: COPYBACK (2 of 3)

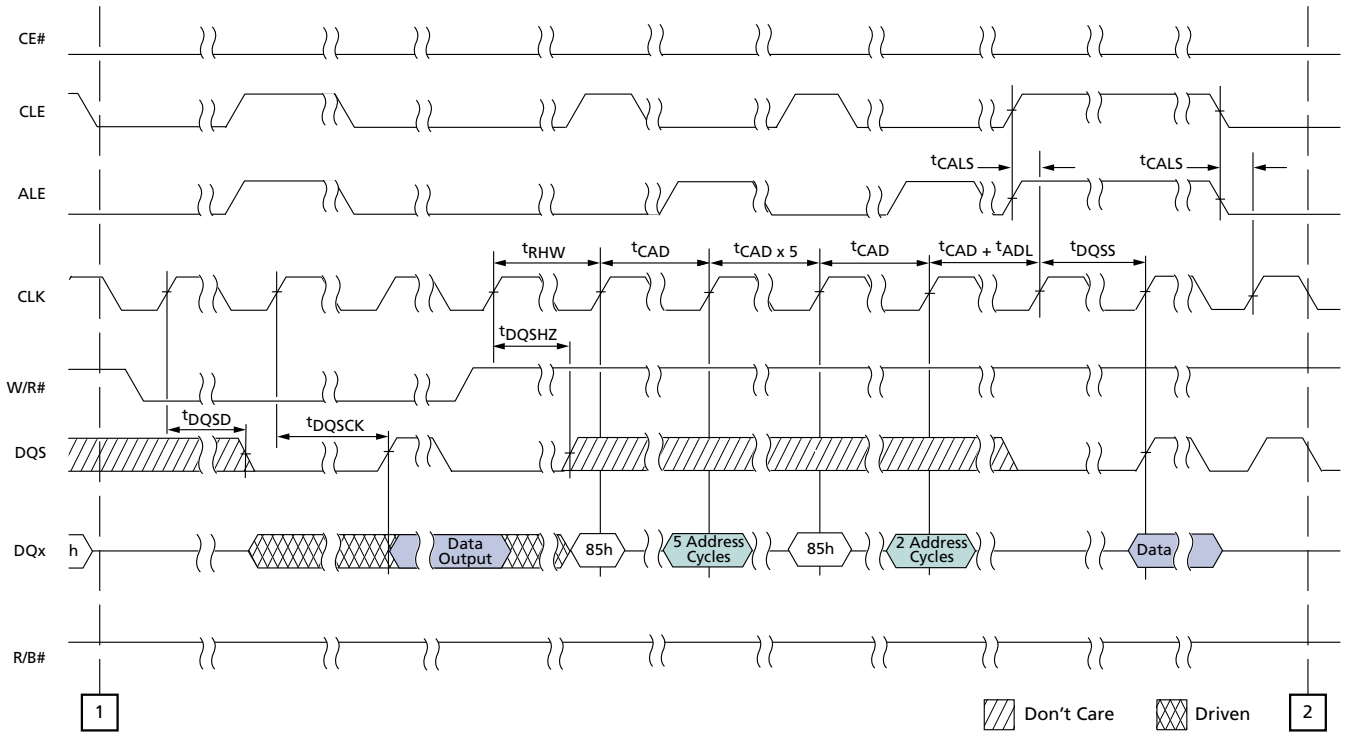


Figure 83: COPYBACK (3 of 3)

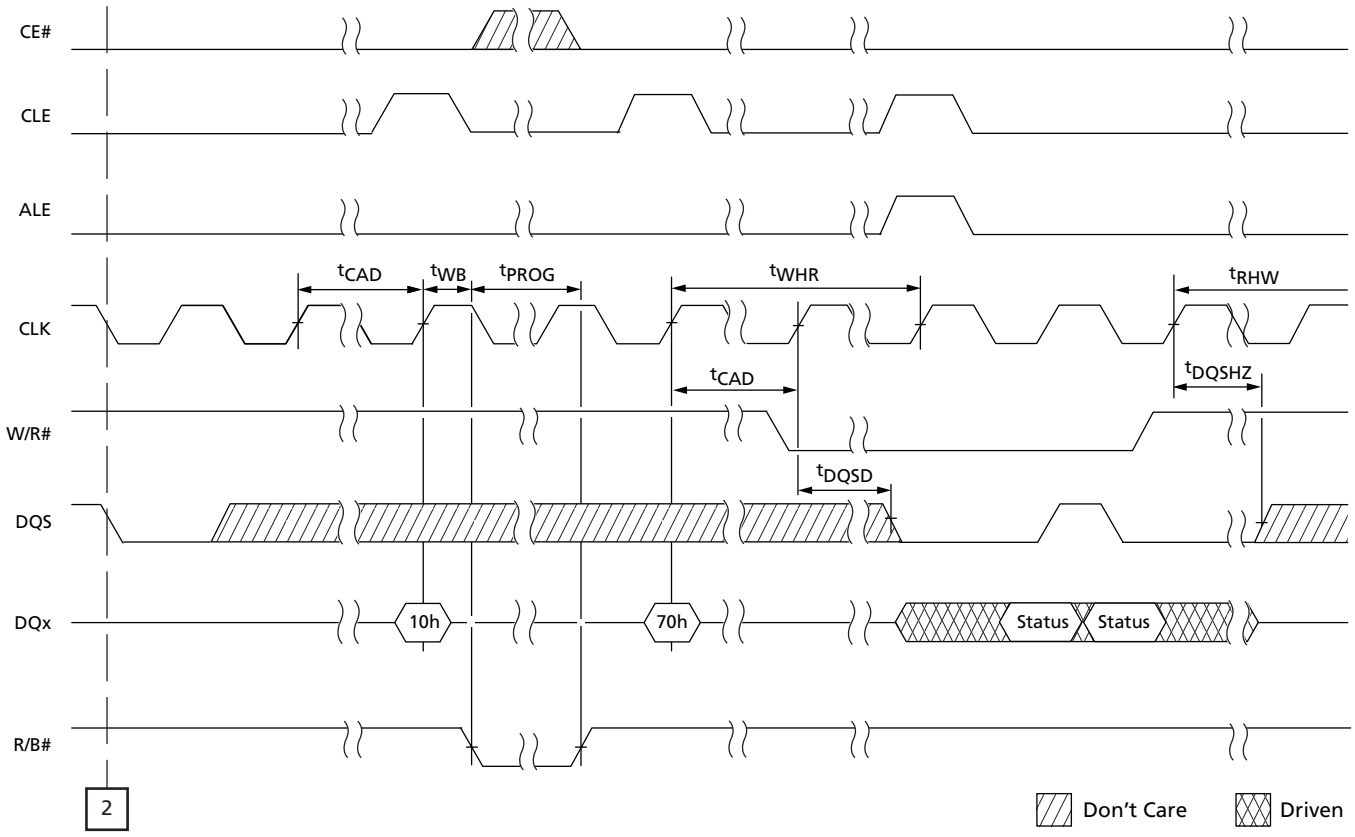


Figure 84: READ OTP PAGE

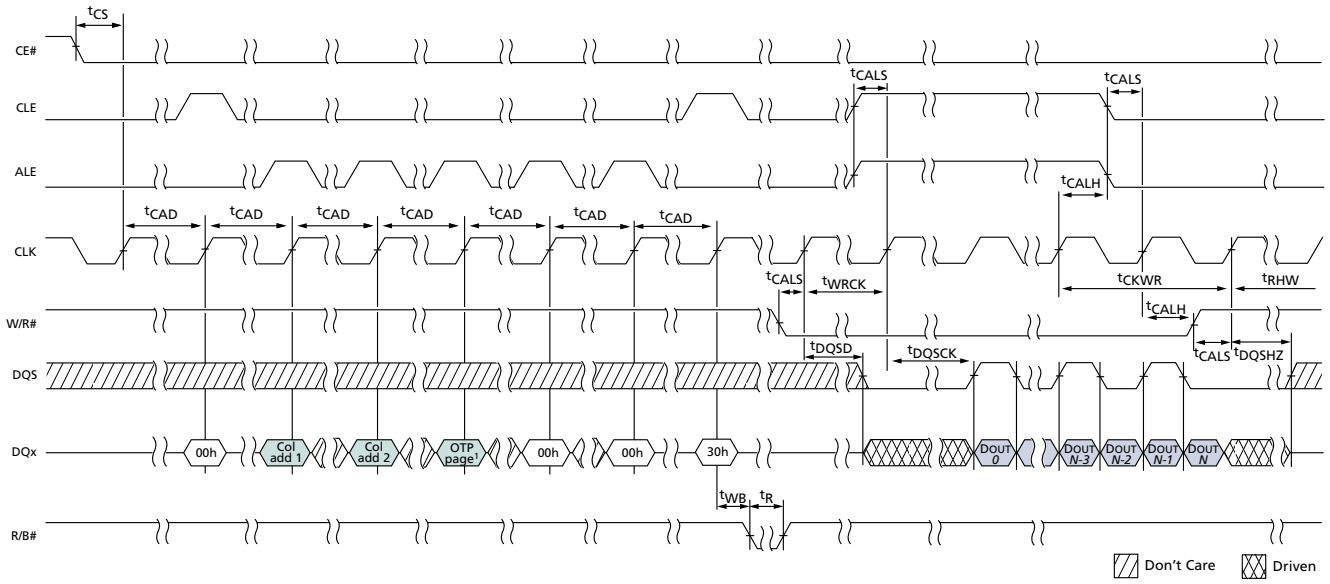


Figure 85: PROGRAM OTP PAGE (1 of 2)

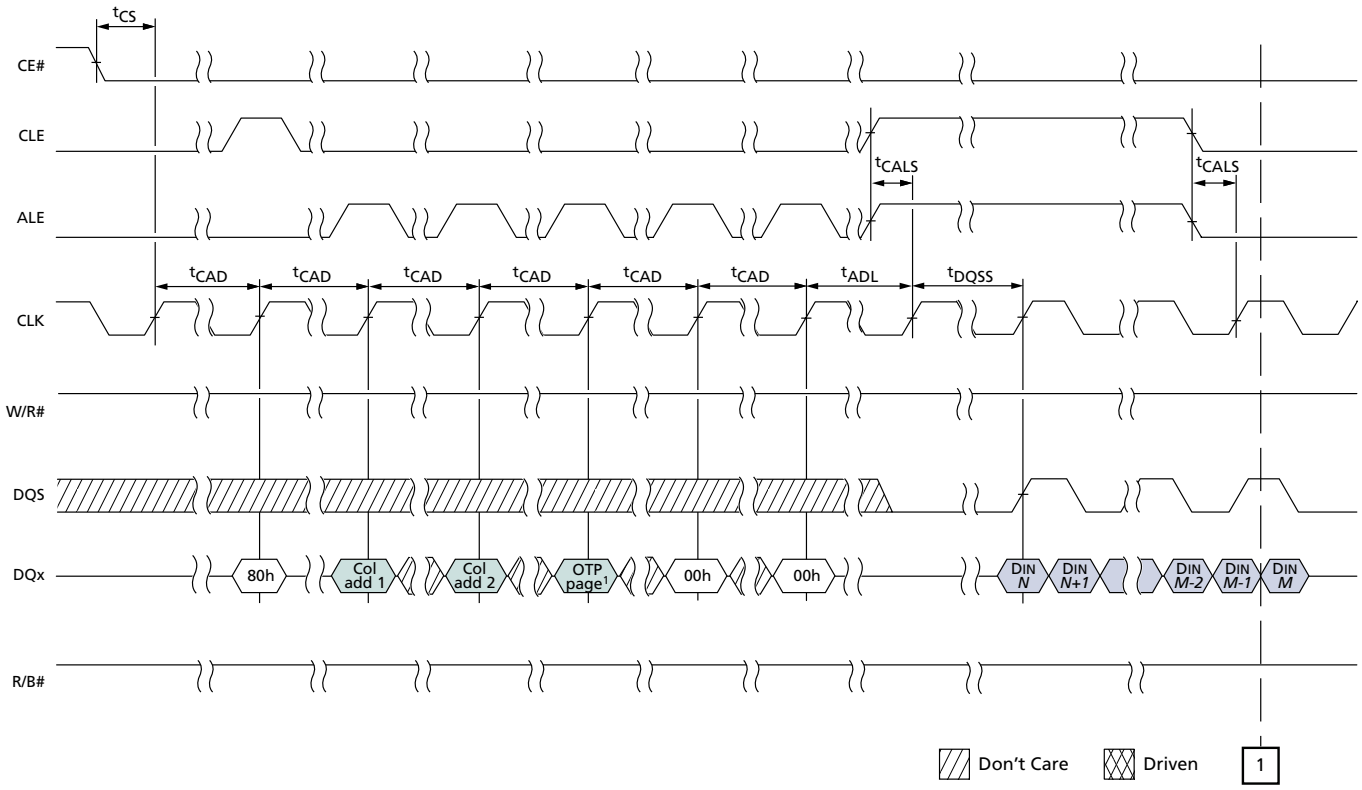


Figure 86: PROGRAM OTP PAGE (2 of 2)

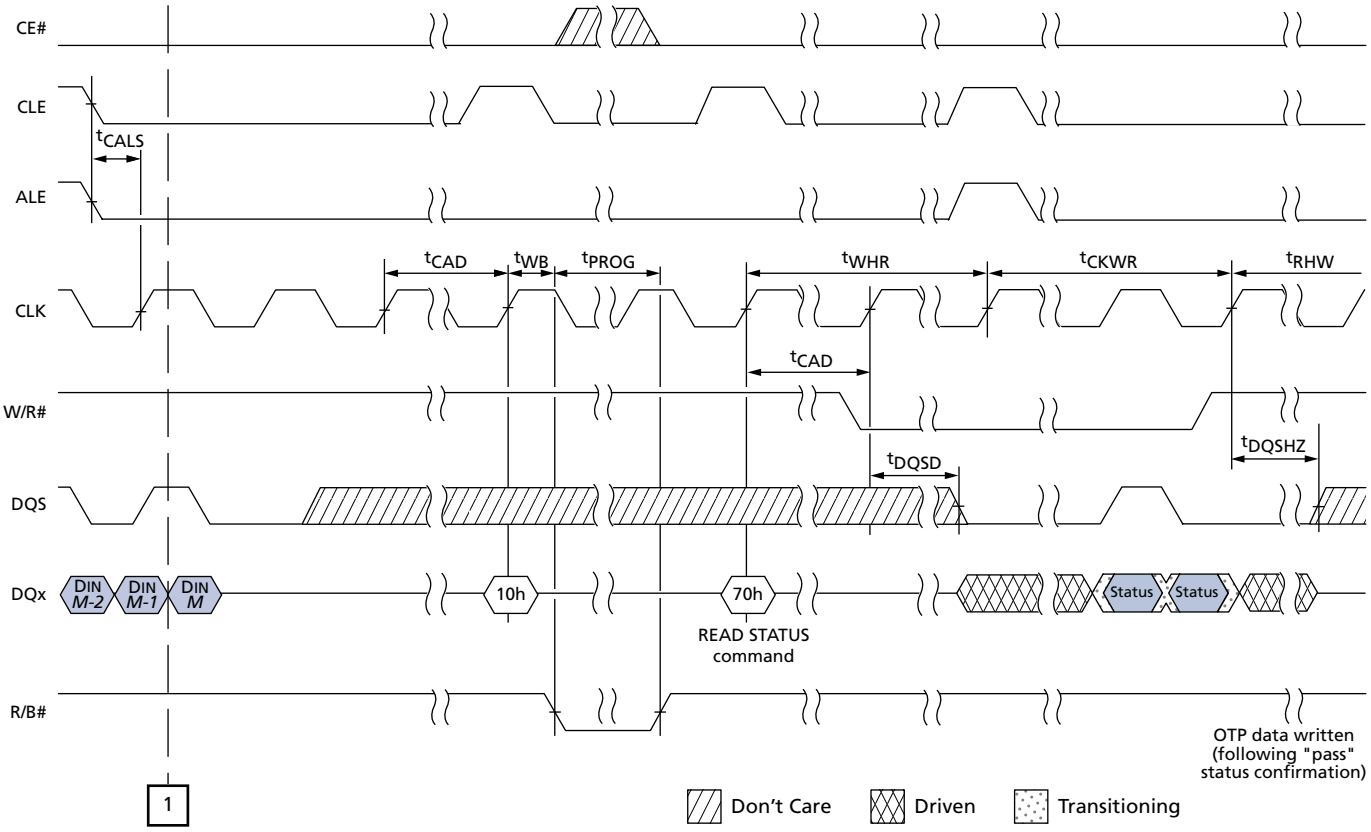
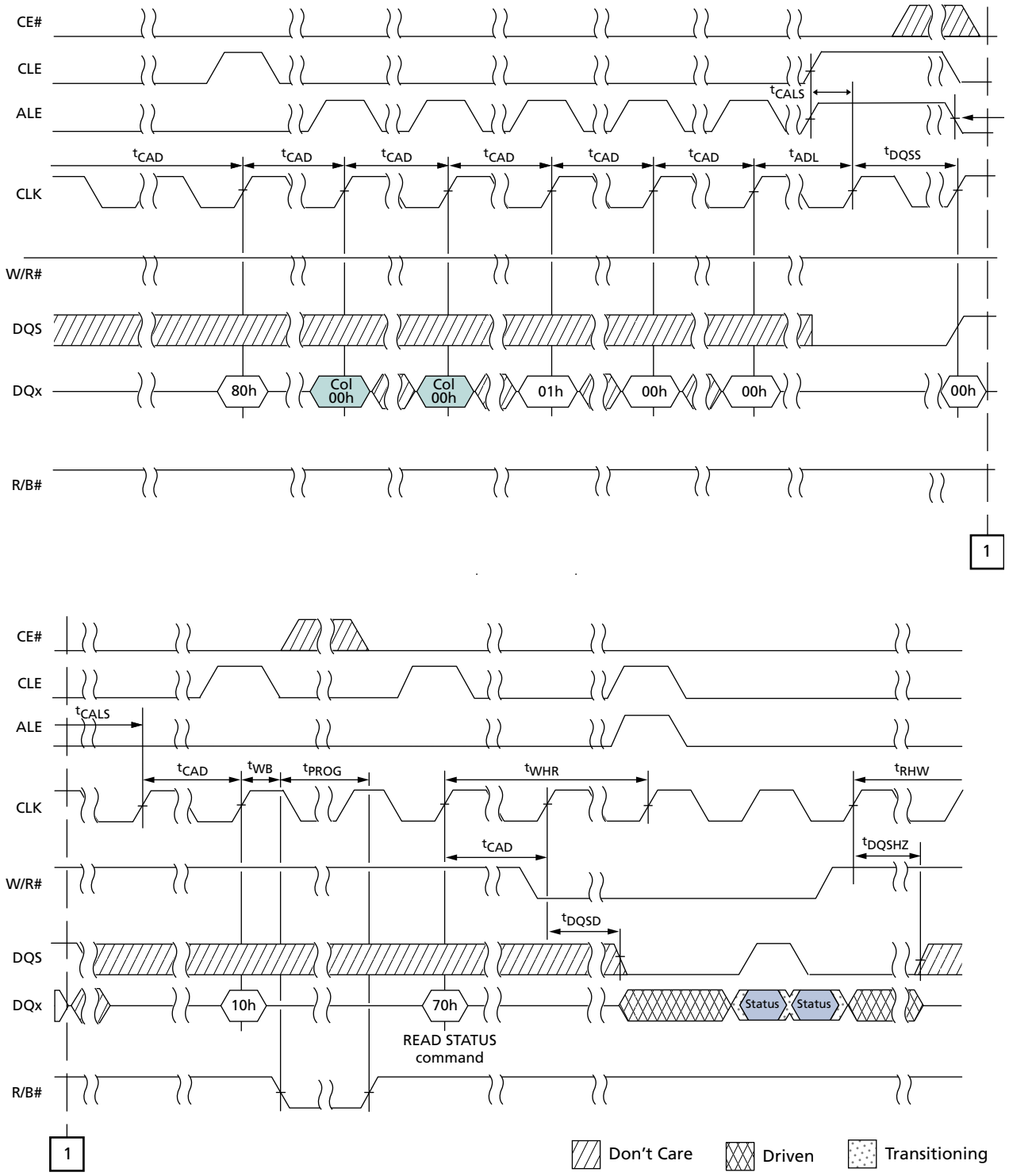


Figure 87: PROTECT OTP AREA



Asynchronous Interface

Figure 88: RESET Operation

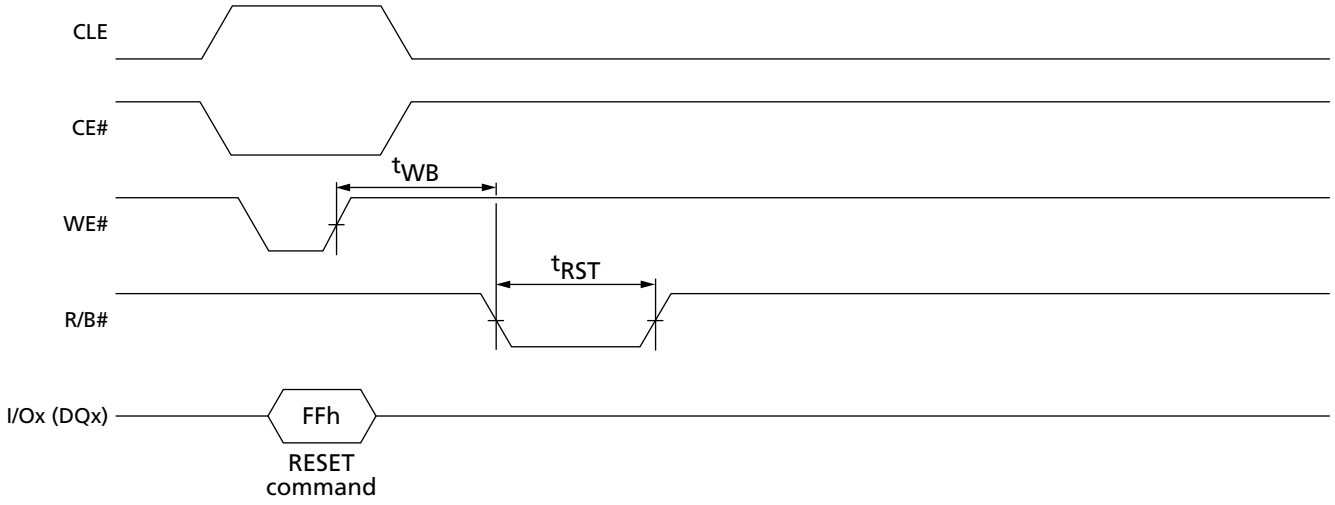


Figure 89: READ STATUS Cycle

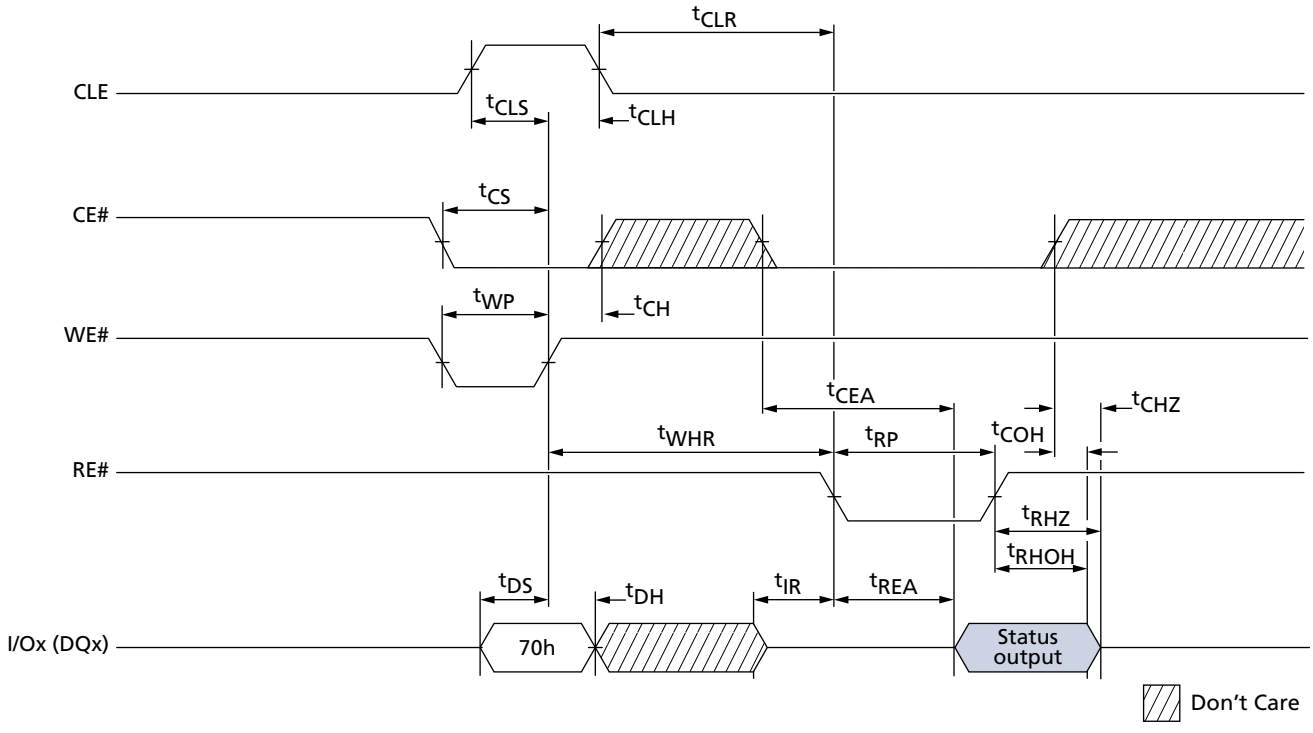


Figure 90: SELECT LUN WITH STATUS Cycle

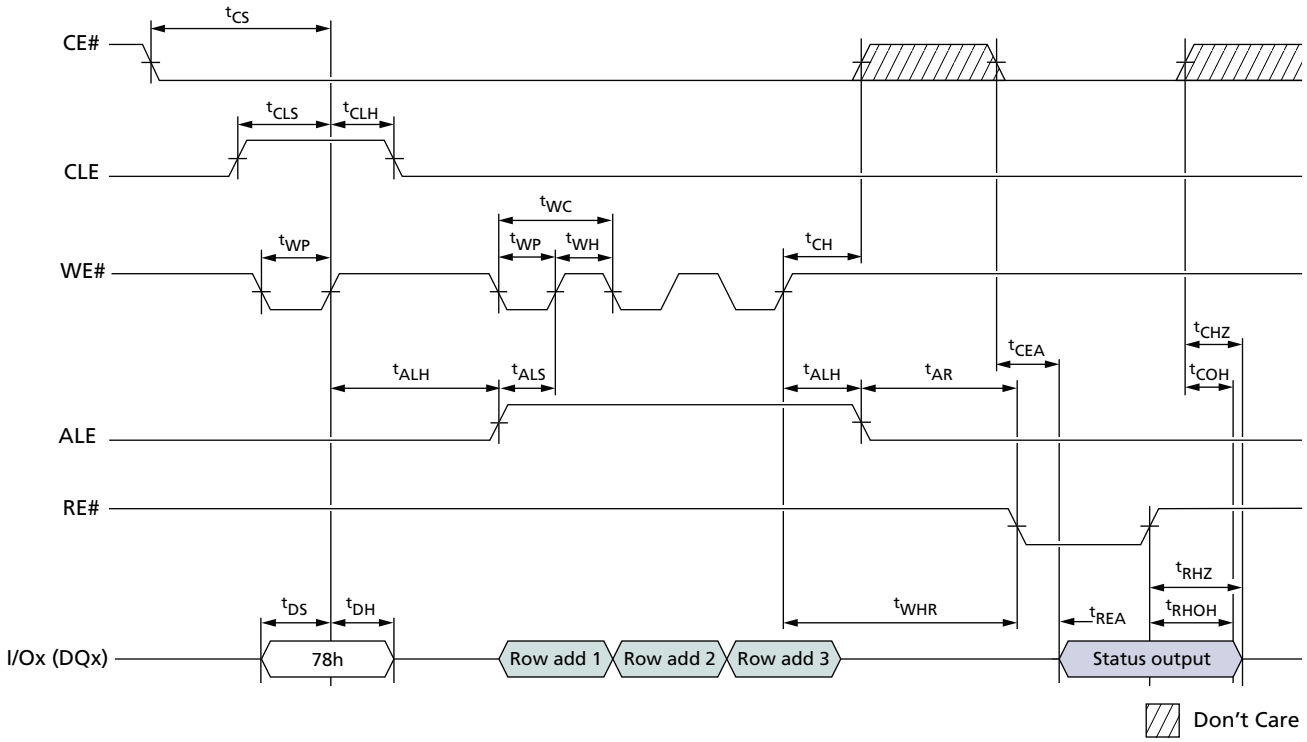


Figure 91: READ PARAMETER PAGE

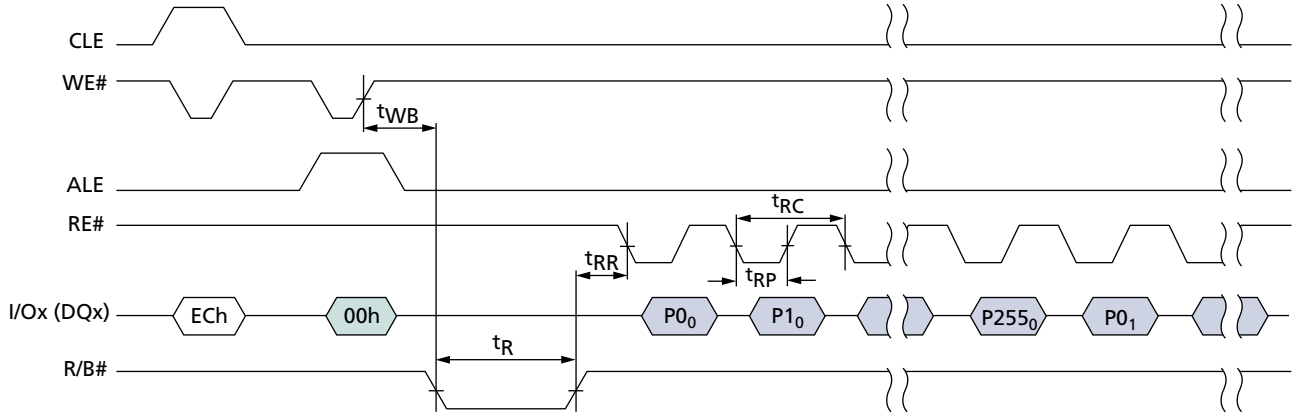


Figure 92: READ PAGE

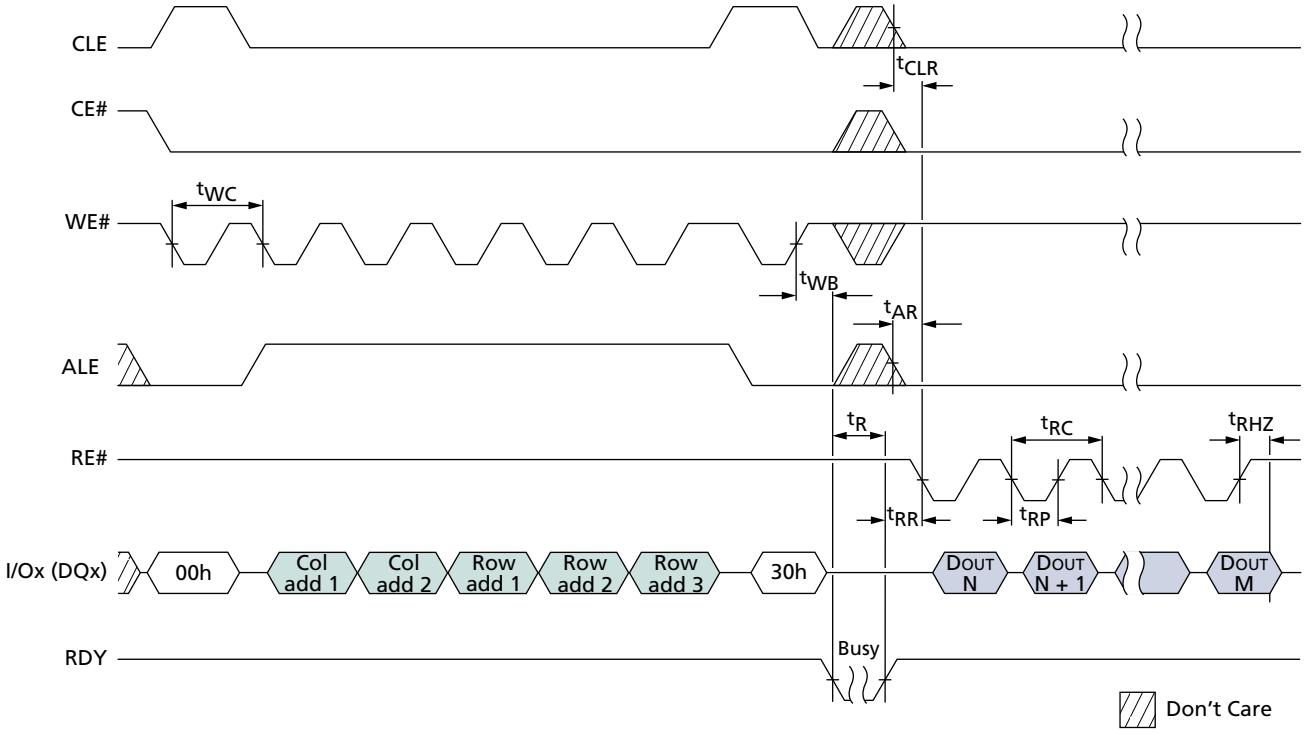


Figure 93: READ PAGE Operation with CE# "Don't Care"

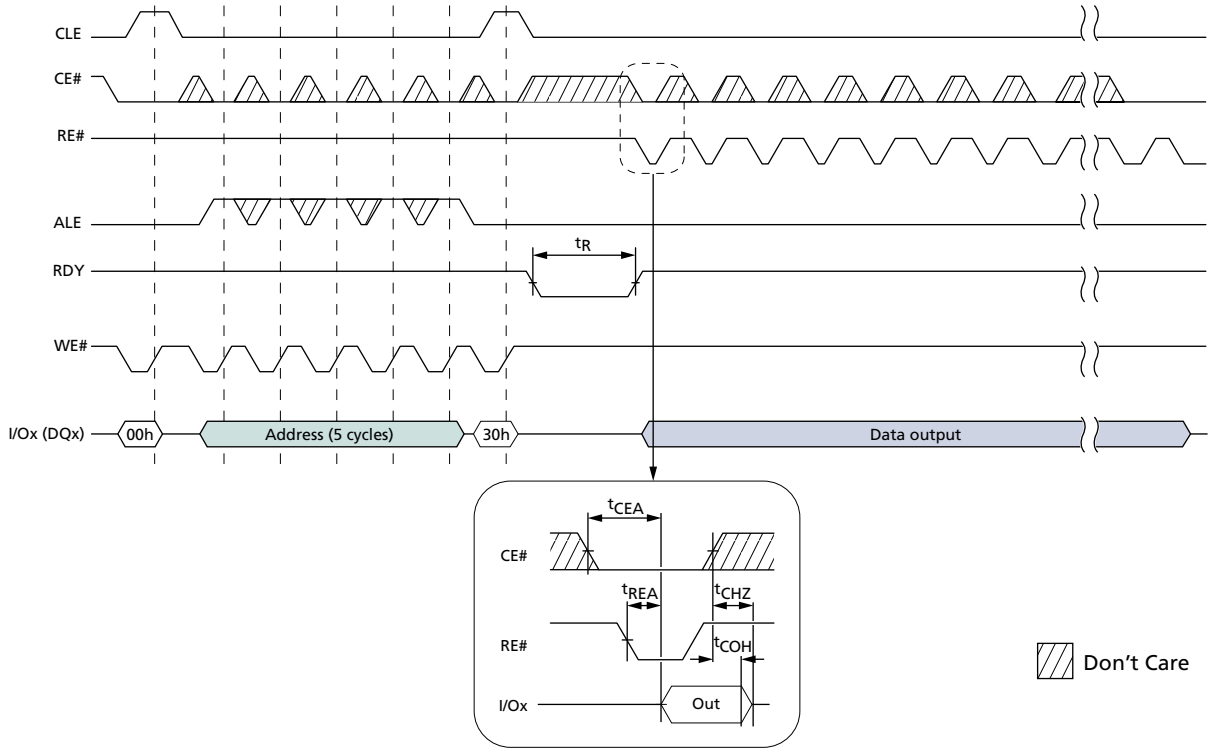


Figure 94: CHANGE READ COLUMN

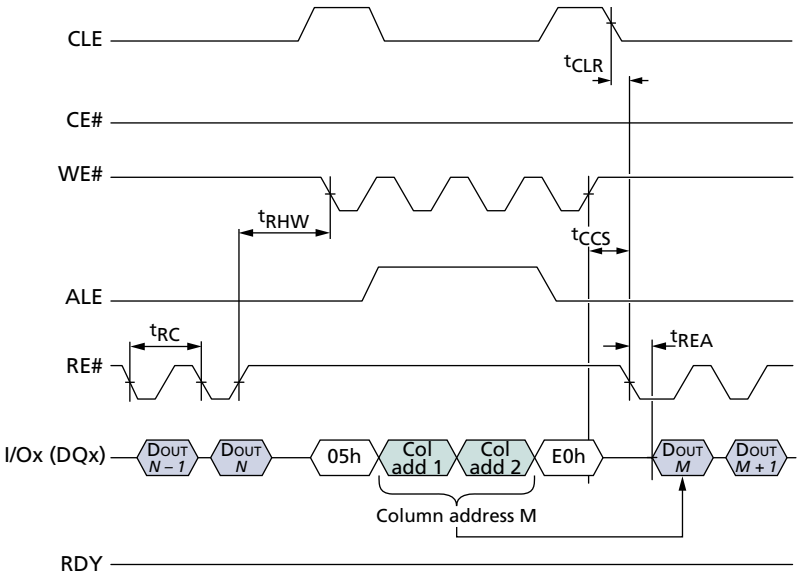


Figure 95: READ PAGE CACHE SEQUENTIAL

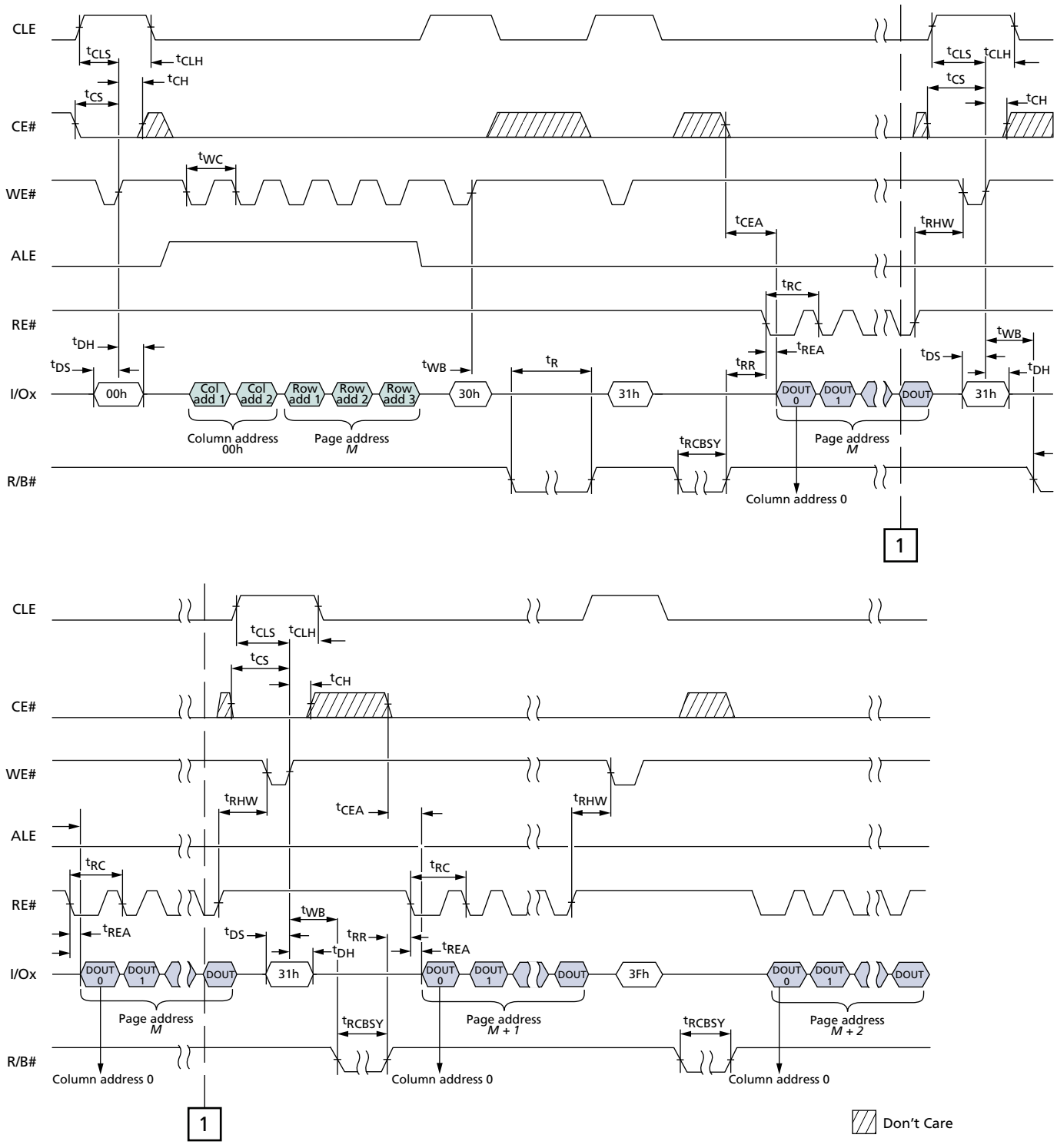


Figure 96: READ PAGE CACHE RANDOM

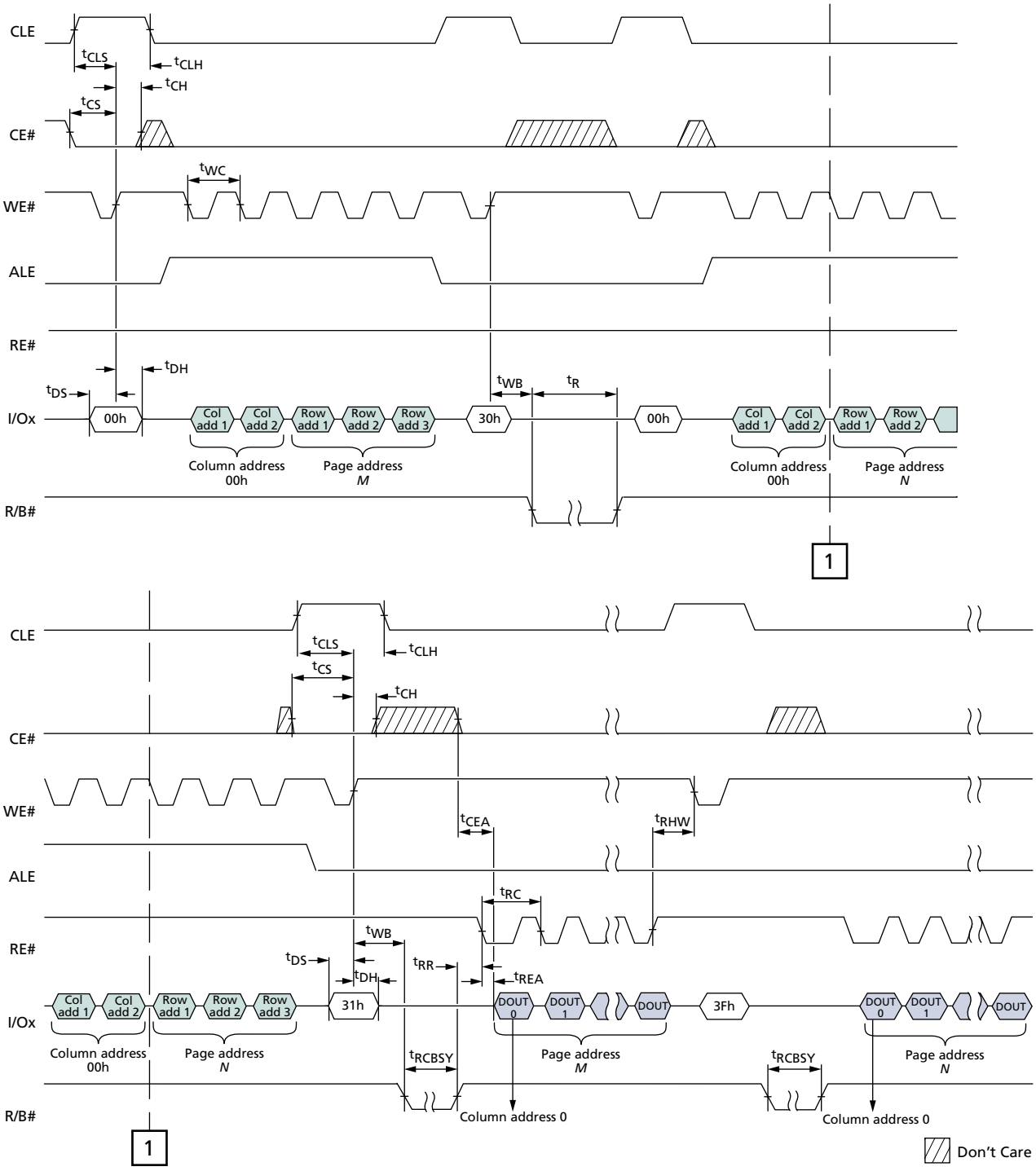


Figure 97: READ ID Operation

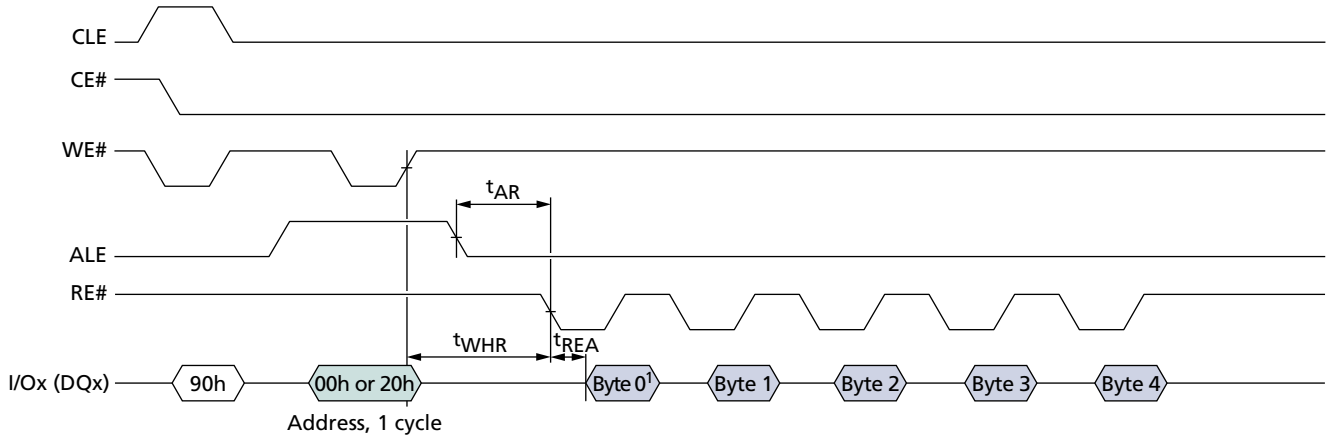


Figure 98: PROGRAM PAGE Operation

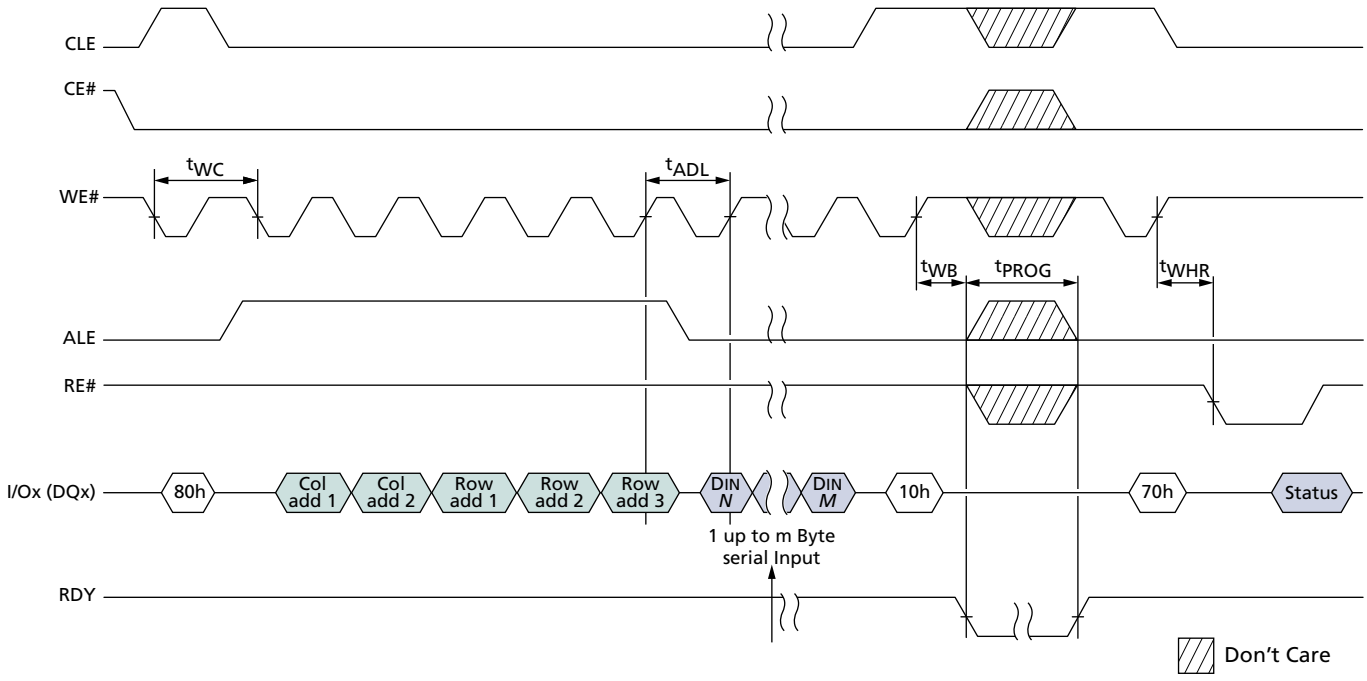


Figure 99: PROGRAM PAGE Operation with CE# "Don't Care"

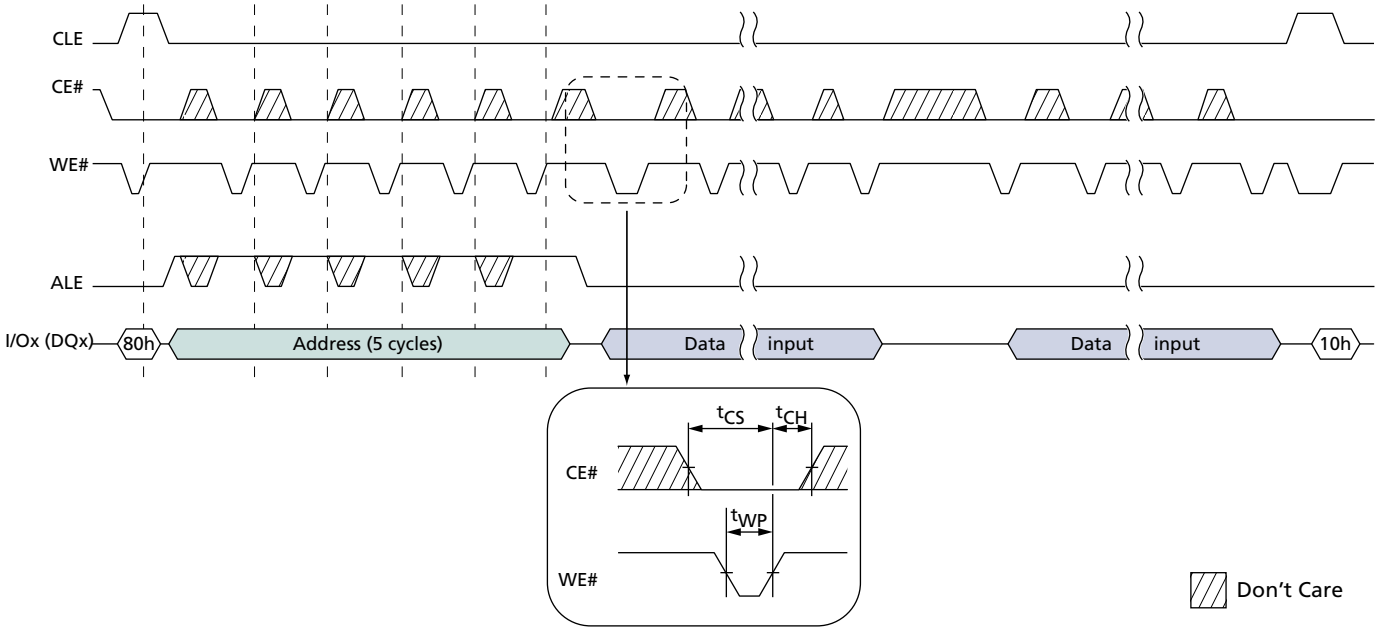


Figure 100: PROGRAM PAGE Operation with CHANGE WRITE COLUMN

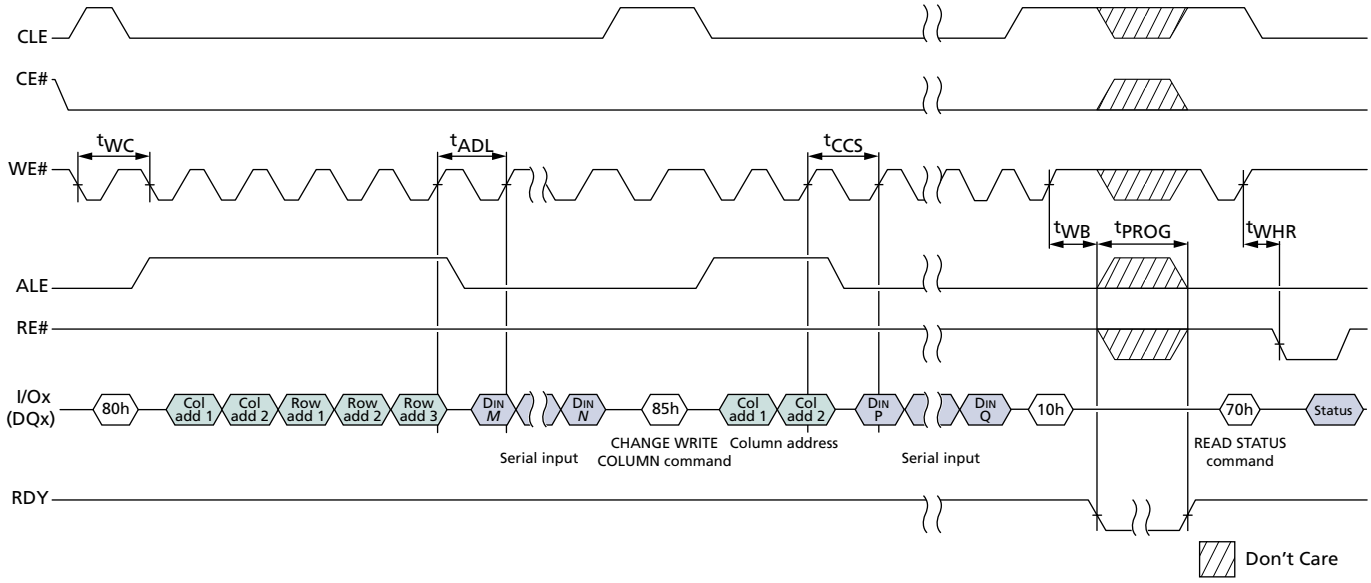


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Figure 101: PROGRAM PAGE CACHE

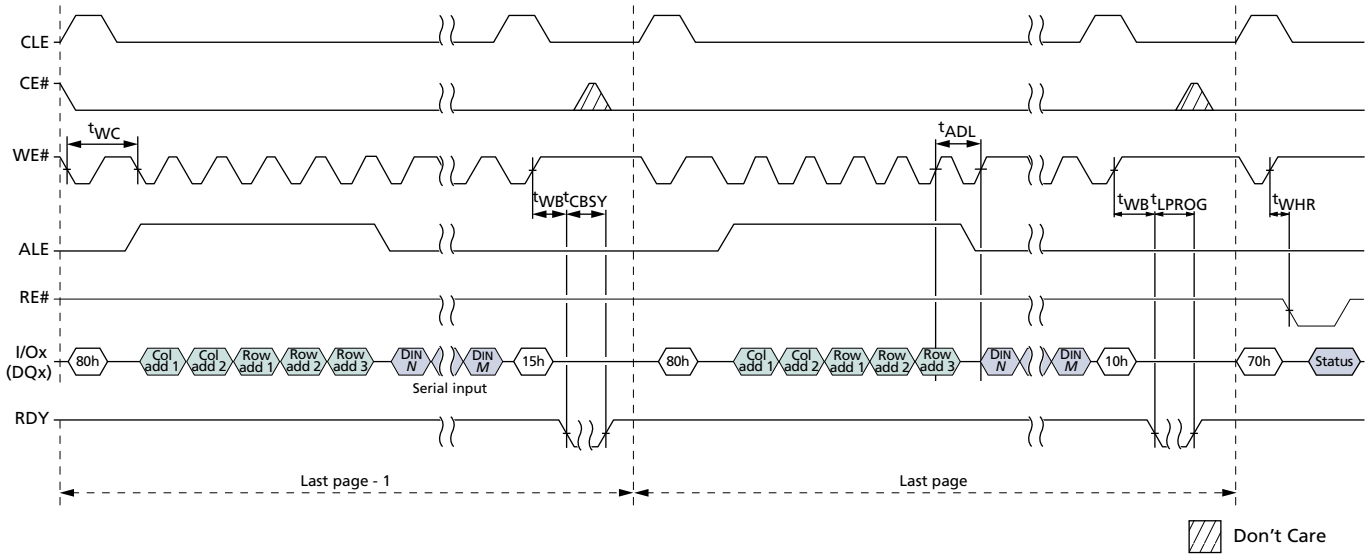


Figure 102: PROGRAM PAGE CACHE Ending on 15h

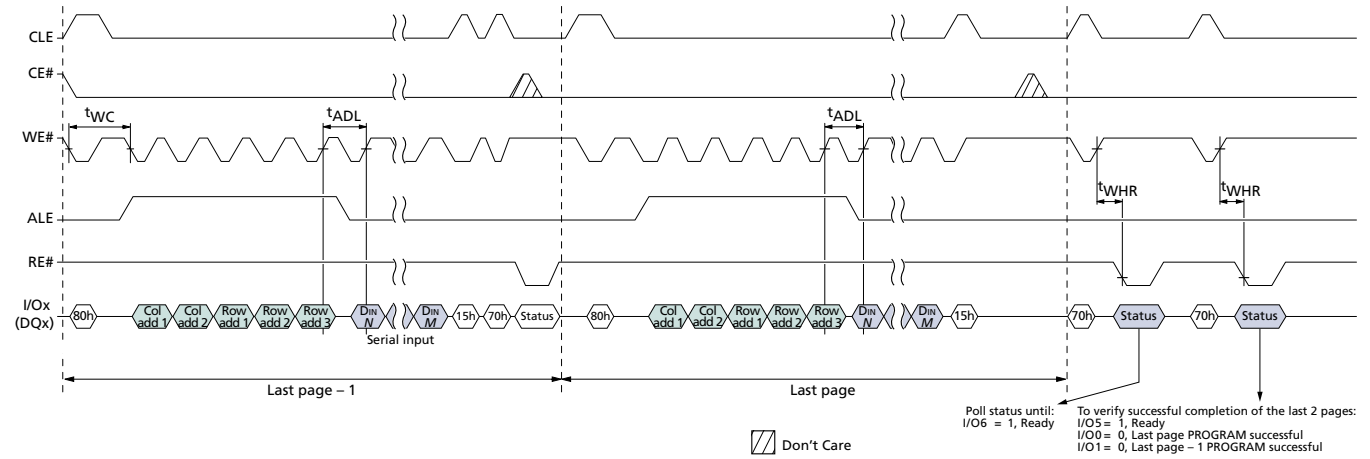


Figure 103: COPYBACK

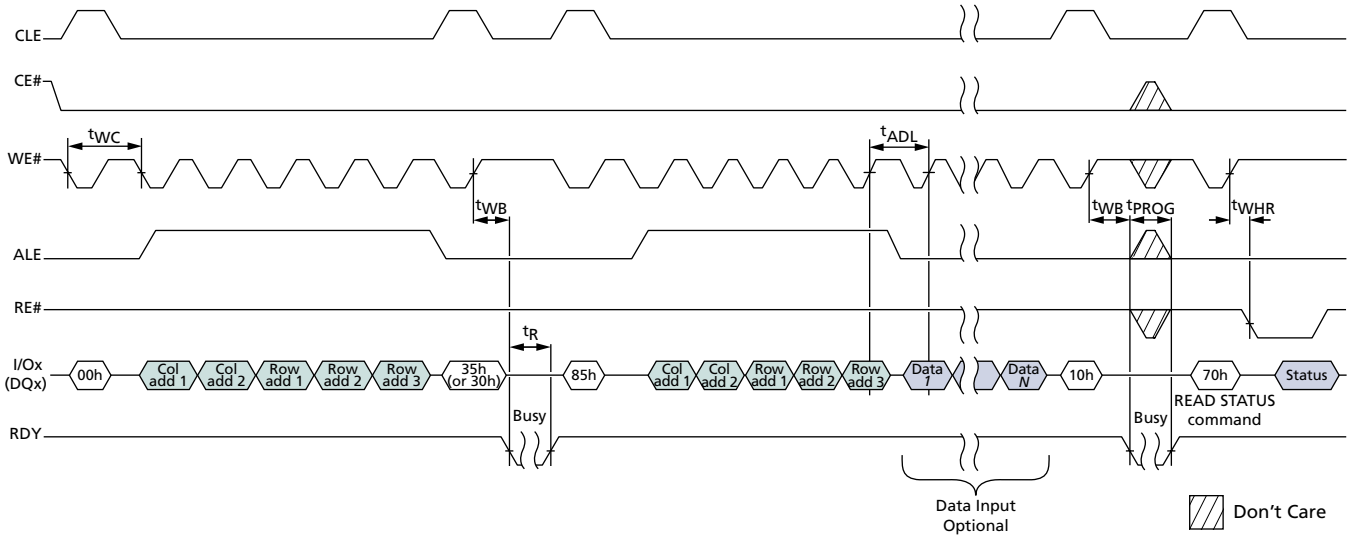
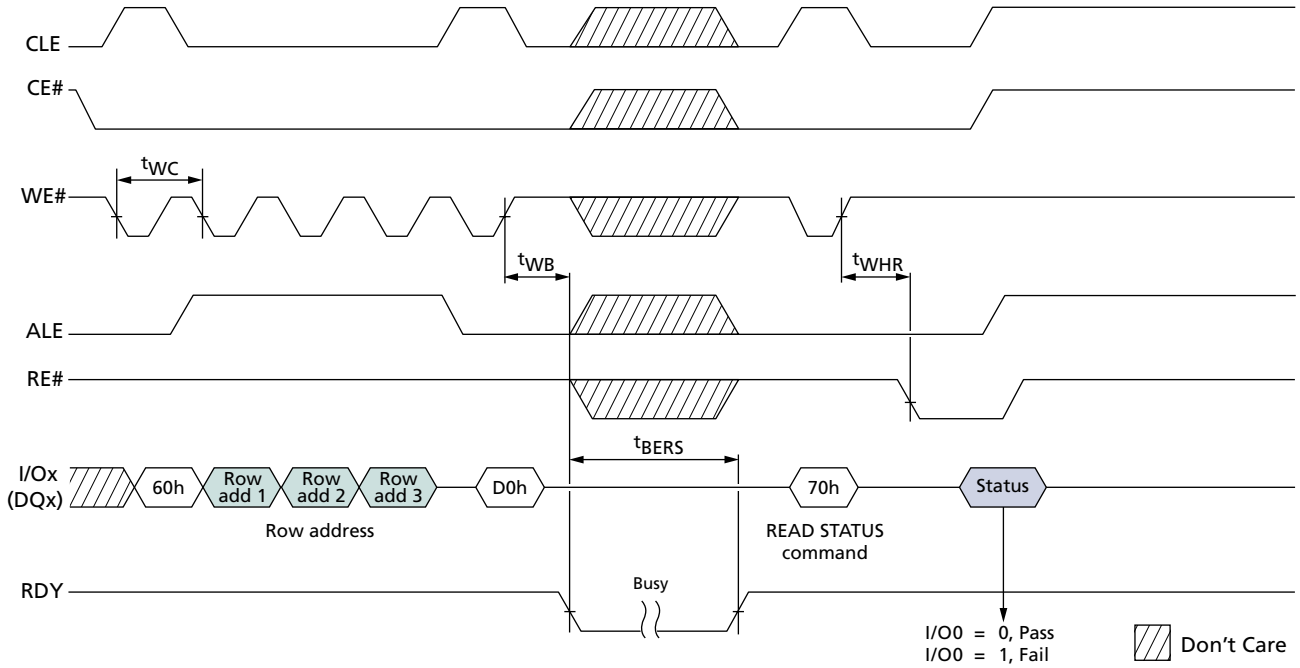
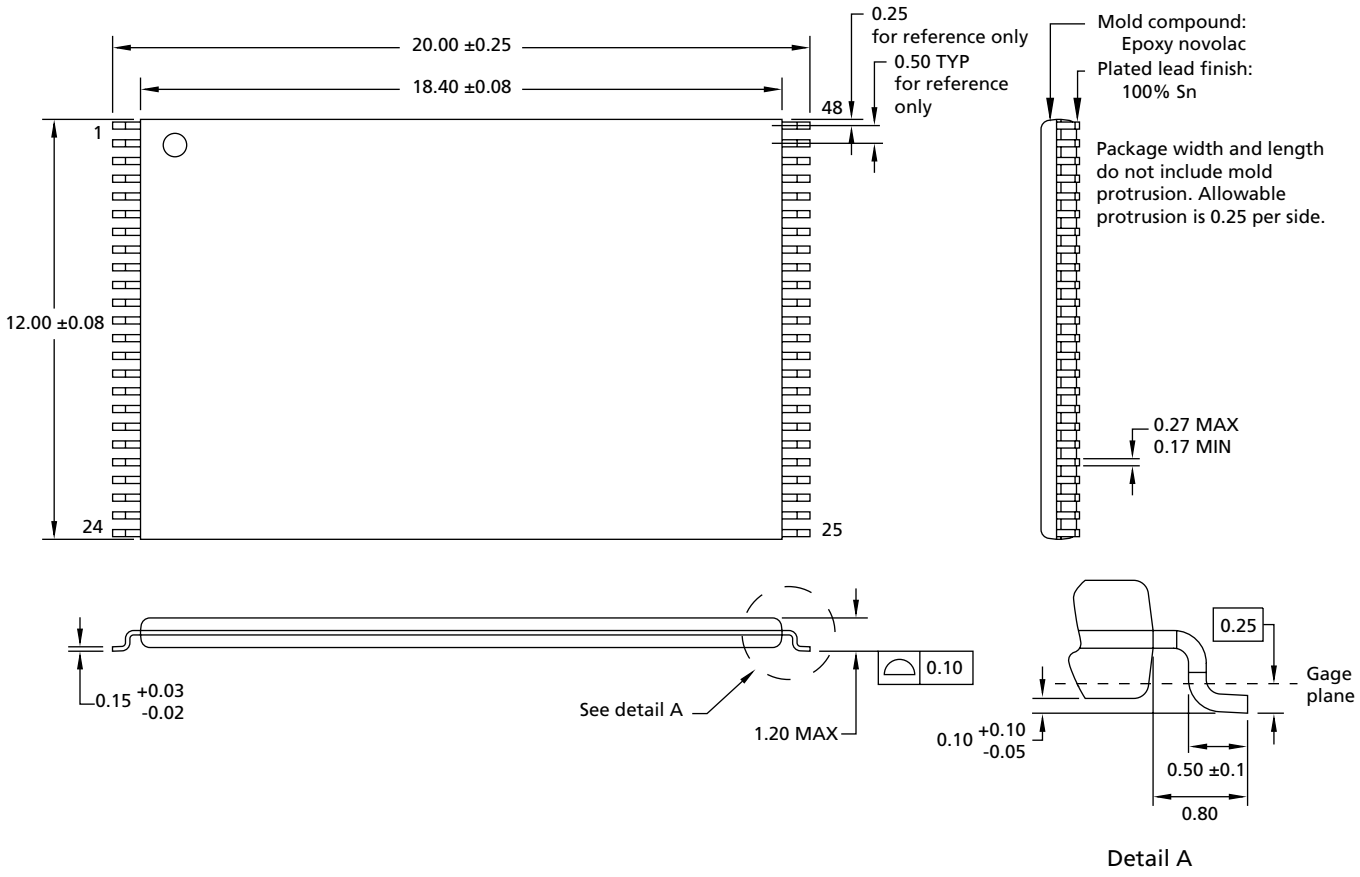


Figure 104: ERASE BLOCK Operation



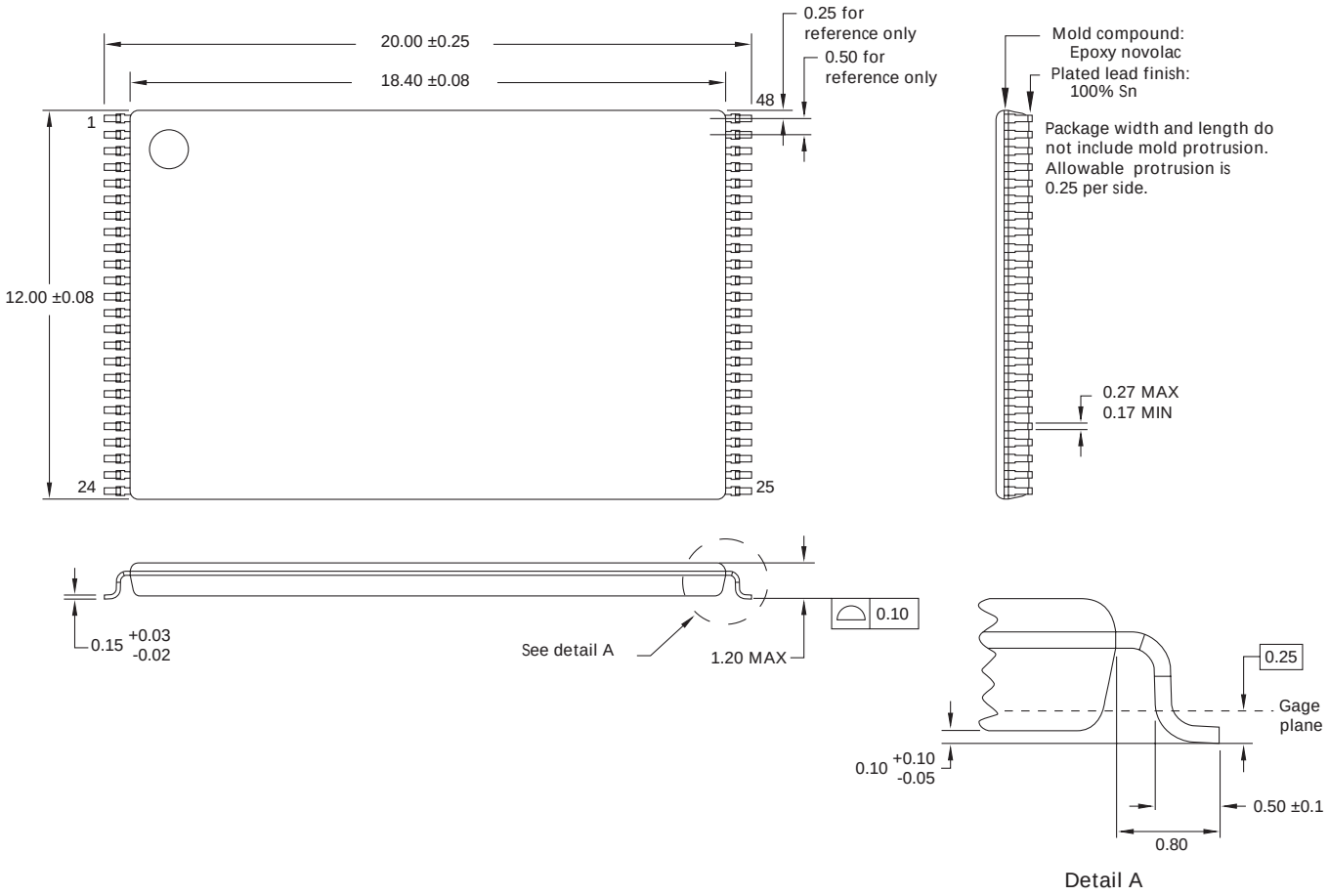
Package Dimensions

Figure 105: 48-Pin TSOP Type 1 CPL (WP Package Code)



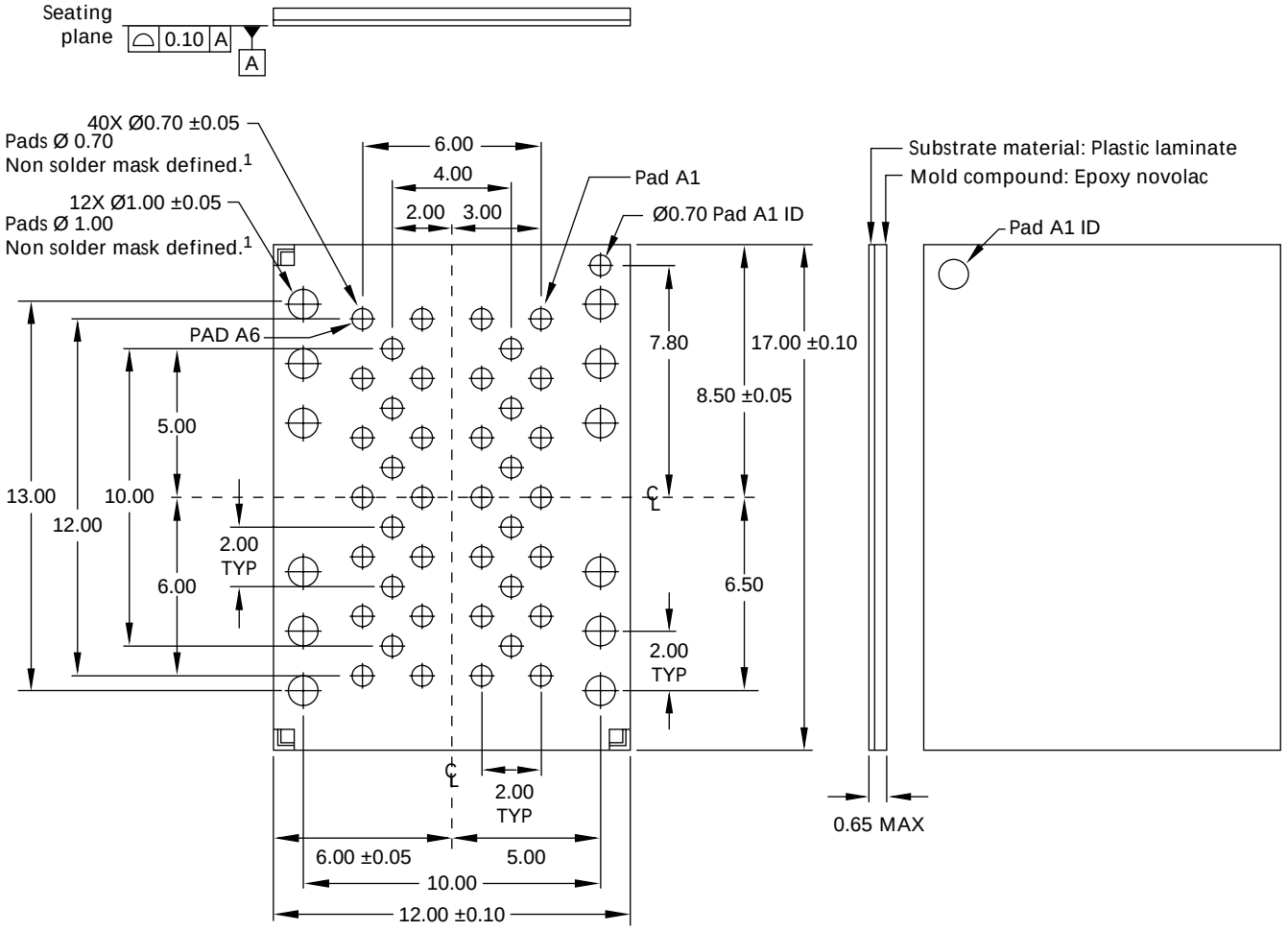
Notes: 1. All dimensions are in millimeters.

Figure 106: 48-Pin TSOP Type 1 OCPL (WC Package Code)



Notes: 1. All dimensions are in millimeters.

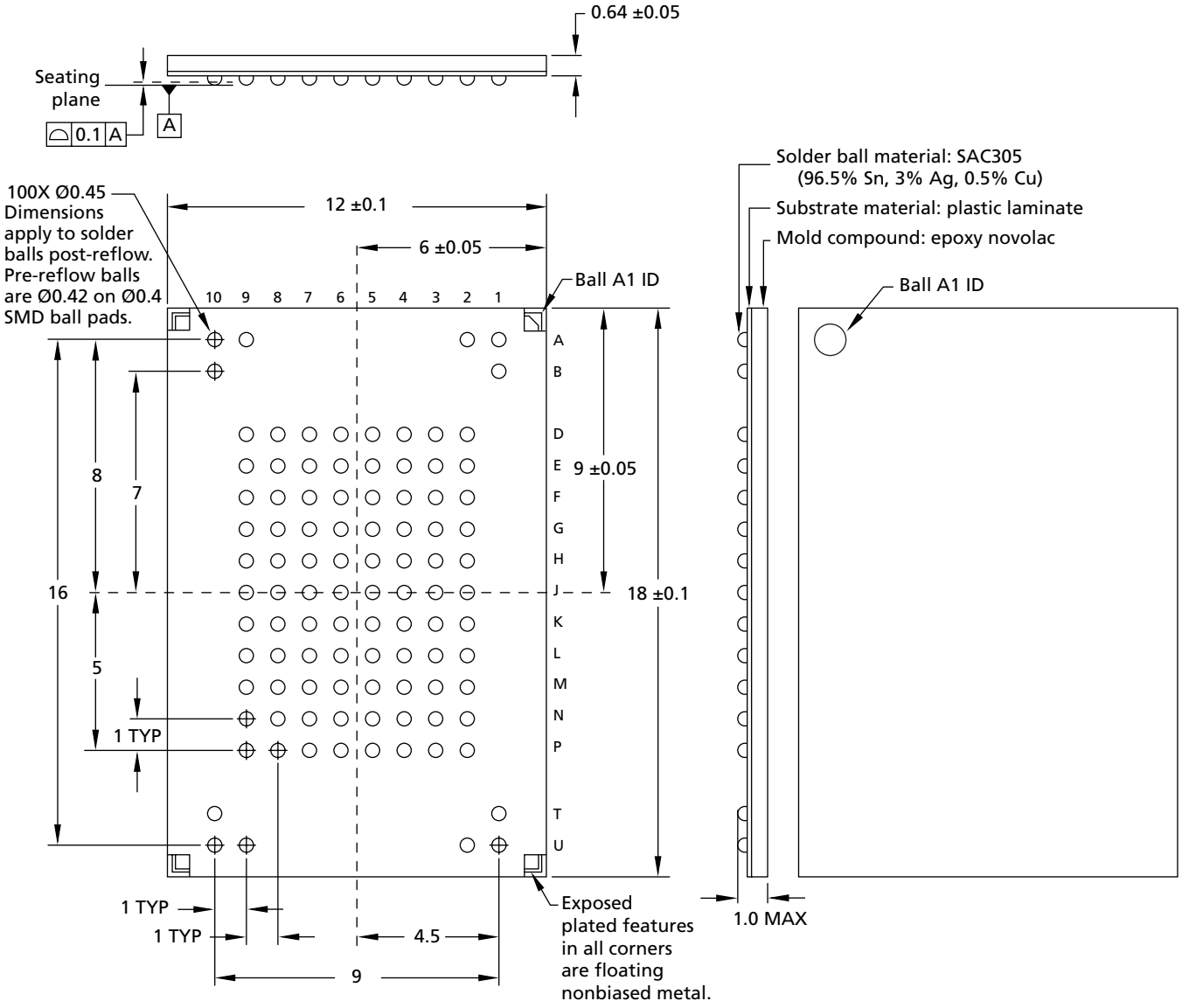
Figure 107: 52-Pad ULGA Package



NOTE 1: Pads are plated with 5-16 microns of nickel followed by a minimum of 0.50 microns of soft wire bondable gold (99.9% pure).

Notes:
1. All dimensions are in millimeters.
2. Solder pads are nonsolder-mask defined (NSMD).
3. Primary datum A (seating plane) is defined by the bottom terminal surface. Metallized test terminal lands or interconnect terminals need not extend below the package bottom surface.

Figure 108: 100-Ball VBGA (Package Code H1), 12×18



Notes: 1. All dimensions in millimeters.

Revision History

Rev A. 2/09

- Initial release
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