Ordering number : EN4357

CMOS LSI

SANYO

No. 4357

# LC7538NM

## Electronic Volume Control System for Car Audio



## Overview

The LC7538NM is a fully equipped electronic volume IC which permits significant reductions in externally connected components while providing ample volume, balance, loudness, fader, bass and treble control functions.

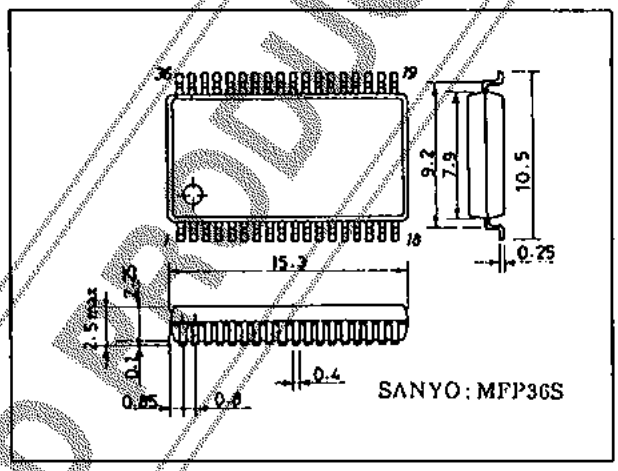
## Features

- Volume : 81 positions ranging from 0 dB to -79 dB (in 1 dB increments) plus -∞. Separate left and right control provides excellent balance function.
- Loudness : Loudness operation provided by externally attached CR to activate tap at the -20 dB position of the volume ladder resistor.
- Fader : Fader function traversing 16 positions with rear or front attenuated output only (these 16 positions consist of 2 dB step intervals ranging from 0 dB to -20 dB, 5 dB step intervals ranging from -20 dB to -45 dB, plus the end settings of -60 dB and -∞).
- Bass and Treble: Using externally attached C (capacitor), the LC7538NM provides bass-treble mutual 15-position control and formats a NF-form tone control circuit (LUX form).
- On-chip OP amplifier for caching applications reduces external components.
- Reduced switching noise with silicon gate CMOS processor.
- All controls performed using serial data input (C²B).

## Package Dimensions

unit : mm

**3129-MFP36S**




## Specifications

### Absolute Maximum Ratings at Ta = 25°C, $V_{SS}$ = 0V

| | | | | unit |
|---|---|---|---|---|
| Maximum supply voltage | $V_{DD}$ max | $V_{DD}$ | 11 | V |
| Input impression voltage | $V_{IN}$ max1 | CL, DI, CE | $V_{SS}$–0.3 to $V_{DD}$+0.3 | V |
| | $V_{IN}$ max2 | LTIN, RTIN, L5dBIN, R5dBIN, L1dBIN, R1dBIN, LFIN, RFIN | $V_{SS}$–0.3 to $V_{DD}$+0.3 | V |
| Allowable power dissipation | Pd max | Ta≤85°C | 280 | mW |
| Operating temperature | Topg | | –40 to +85 | °C |
| Storage temperature | Tstg | *1 | –50 to +125 | °C |

*1 When mounting the QIP package on the board, do not dip the entire package in solder.

Continued on next page.



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## Allowable Operation Conditions at Ta = 25°C, $V_{SS}$ = 0V

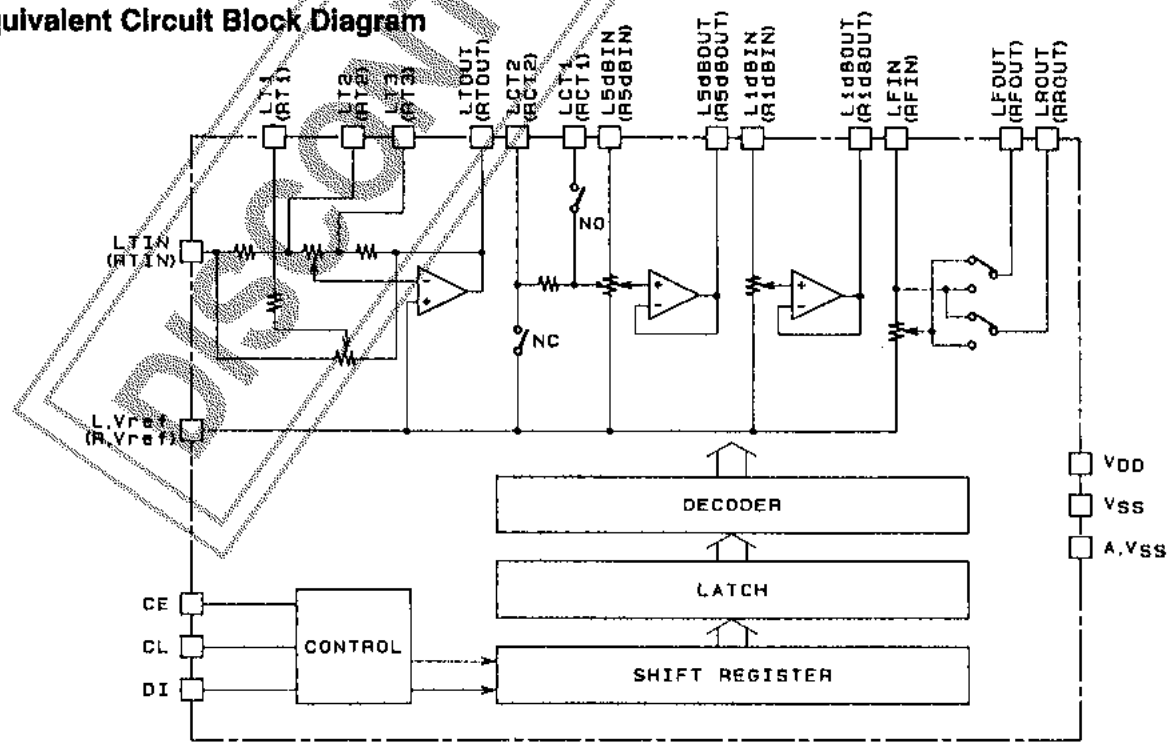
| | | | min | typ | max | unit |
|---|---|---|---|---|---|---|
| Supply voltage | $V_{DD}$ | *2 | 7.0 | | 10.0 | V |
| Input "H" level voltage | $V_{IH}$ | CL, DI, CE | 4.0 | | $V_{DD}$ | V |
| Input "L" level voltage | $V_{IL}$ | CL, DI, CE | $V_{SS}$ | | 1.0 | V |
| Input amplitude voltage | $V_{IN}$ | LTIN, RTIN, L5dBIN, R5dBIN, L1dBIN, R1dBIN, LFIN, RFIN | $V_{SS}$ | | $V_{DD}$ | Vp-p |
| Input pulse width | $t_{\varnothing W}$ | CL | 1 | | | µs |
| Setup time | $t_{SETUP}$ | CL, DI, CE | 1 | | | µs |
| Hold time | $t_{HOLD}$ | CL, DI, CE | 1 | | | µs |
| Operating Frequency | fopg | CL | | | 500 | kHz |

*2 A capacitor rated at 2000 pF or less should be installed between all power supply pins and $V_{SS}$.

## Electrical Characteristics at Ta = 25°C, $V_{DD}$ = 9V, $V_{SS}$ = 0V

| | | | min | typ | max | uint |
|---|---|---|---|---|---|---|
| Total harmonic distortion | THD (1) | $V_{IN}$ = 1Vrms, f = 1kHz, total overall flat | | 0.04 | | % |
| | THD (2) | $V_{IN}$ = 1Vrms, f = 20kHz, total overall flat | | 0.06 | | % |
| Crosstalk | CT | $V_{IN}$ = 1Vrms, f = 1kHz, total overall flat, Rg = 1kΩ | 60 | 87 | | dB |
| Maximum Output Reduction | Vo min | $V_{IN}$ = 1 Vrms, f = 1 kHz, main volume →∞, fader volume →∞, C = 1000 µF between Vref and $V_{SS}$ for L/R | | 82 | | dB |
| All Resistance Value | $R_{VOL}$ (1) | 5dB step | 15 | 25 | 35 | kΩ |
| | $R_{VOL}$ (2) | 1dB step | 12 | 20 | 28 | kΩ |
| | $R_{FADER}$ | | 12 | 20 | 28 | kΩ |
| | $R_{BASS}$ | | 48 | 80 | 112 | kΩ |
| | $R_{TREBLE}$ | | 30 | 50 | 70 | kΩ |
| Input "H" level current | $I_{IH}$ | VI = 9V (CL, CE, DI pins) | | | 10 | µA |
| Input "L" level current | $I_{IL}$ | VI = 0V (CL, CE, DI pins) | −10 | | | µA |
| Output noise voltage | $V_N$ | All overall flat (IHF-A), Rg = 1kΩ | | 7.5 | 15 | µV |
| Current consumption | $I_{DD}$ | $V_{DD}$-$V_{SS}$ = 10V | | 15 | 28 | mA |

## Equivalent Circuit Block Diagram

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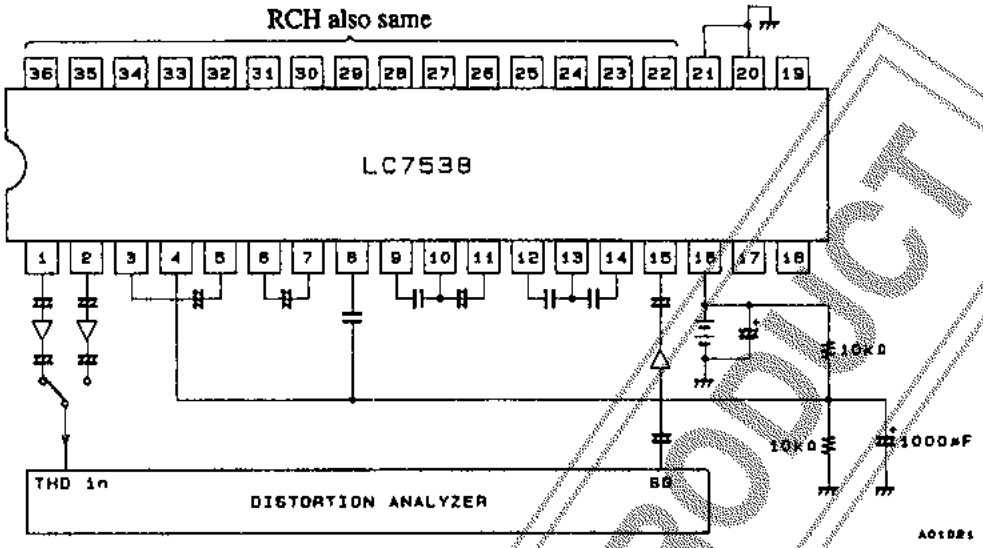
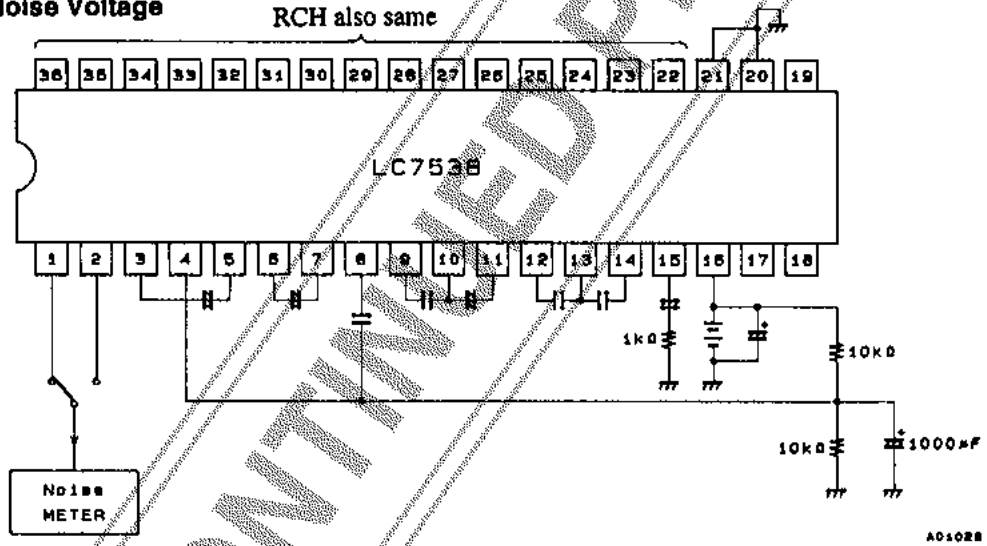
## Test Circuit

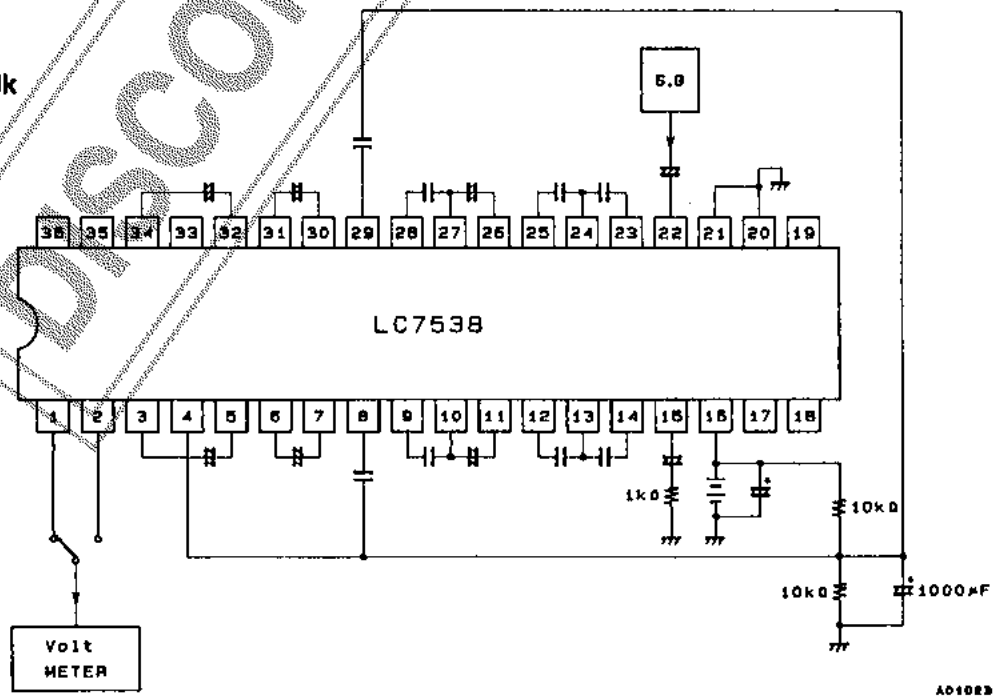
### a) Total Harmonic Distortion



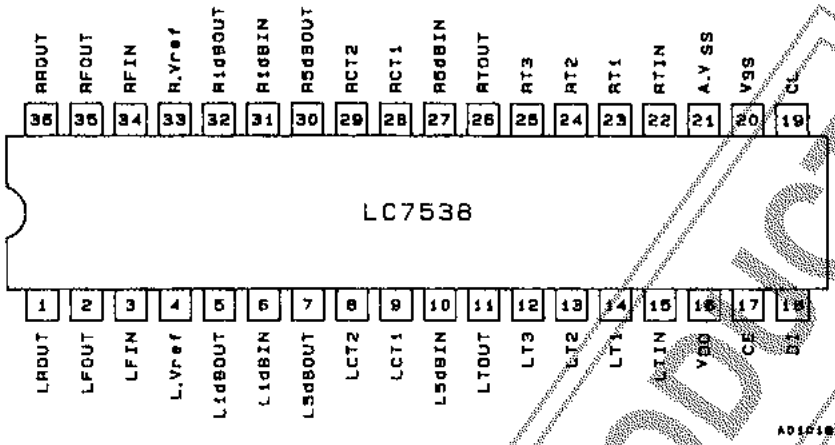

### b) Output Noise Voltage




### c) Crosstalk

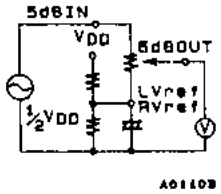


## Pin Assignment






## Pin Descriptions

| Pin Name | Pin No. | Description | Remarks |
|---|---|---|---|
| LROUT | 1 | • These pins function as output pins for the fader. Output reduction for rear and front is performed separately for each. Attenuation capacity is unified for both left and right. Step positioning is designed using an open circuit so that reception is performed using high impedance. | |
| LFOUT | 2 | | |
| RROUT | 36 | | |
| RFOUT | 35 | | |
| LFIN | 3 | • When utilizing the fader function, these pins function as input pins. | |
| RFIN | 34 | • Low impedance driven. | |
| LVref | 4 | • These pins are common pins for fader volume, tone and main volume. The pattern impedance connected here should be lowered as much as possible. |  |
| RVref | 33 | • LVref and RVref are not connected to $V_{SS}$. | |
| | | • Connections for LVref and RVref to $V_{SS}$ should be established externally to match all specifications. Notably, attention should be paid to capacity since capacitors are subject to residual resistance during volume output reduction when installed between LVref (RVref) and $V_{SS}$ as is the case with single power sources. | |
| | | • Normally, high voltage applied from $V_{DD}$. | |
| L1dBOUT | 5 | • These pins are output pins for the 1 dB step attenuator located in the section main volume. | |
| R1dBOUT | 32 | | |
| L1dBIN | 6 | • These pins are input pins for the 1 dB step attenuator located in the section main volume. | VR Resistance: 20kΩ |
| R1dBIN | 31 | • Low impedance driven. | |
| L5dBOUT | 7 | • These pins are output pins for the 5 dB step attenuator located in the section main volume. | |
| R5dBOUT | 30 | | |
| LCT1 | 9 | • These pins are for loudness control. Connect a hi-band compensation capacitor between CT1 to 5dB IN and a low-band compensation capacitor between CT2 to Vref. | |
| LCT2 | 8 | | |
| RCT1 | 28 | | |
| RCT2 | 29 | | |
| L5dBIN | 10 | • These pins are input pins for the 5 dB step attenuator located in the section main volume. | |
| R5dBIN | 27 | • Low impedance driven. | |

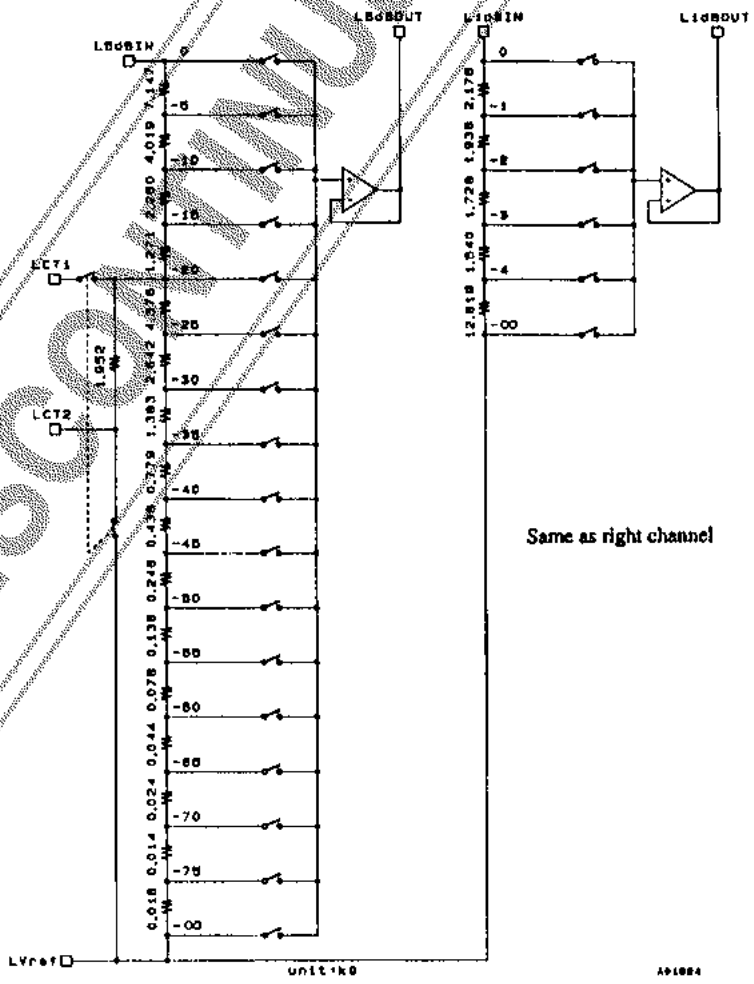
Continued on next page.

Continued from preceding page.

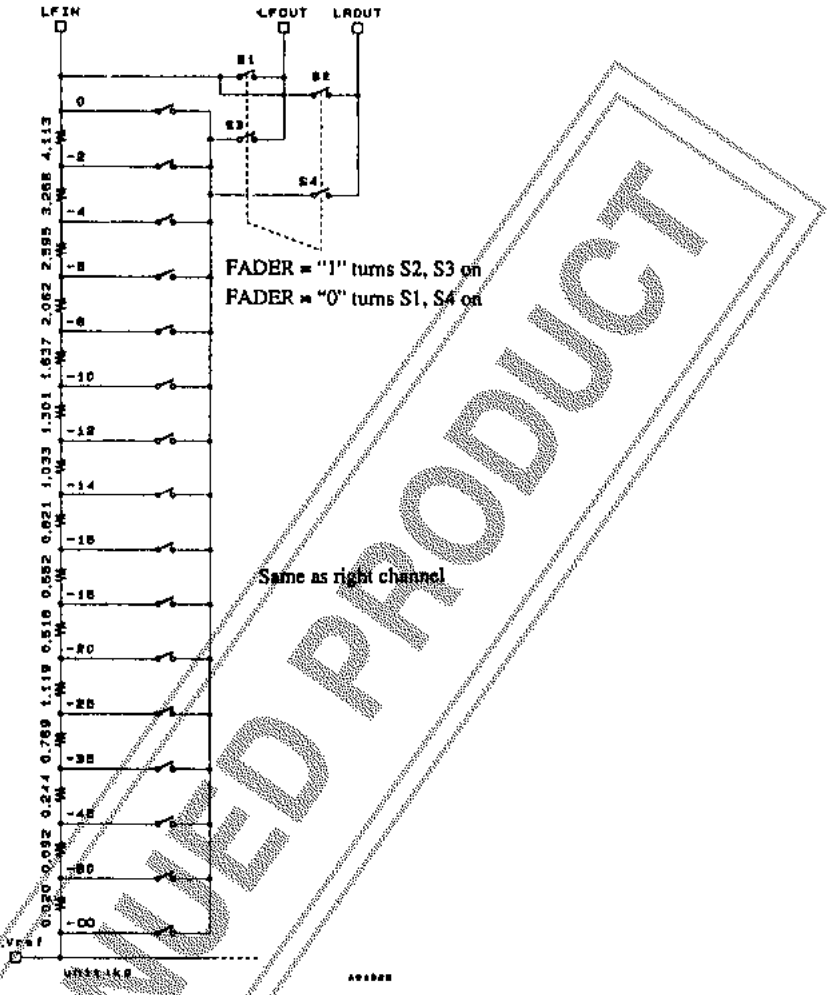
| Pin Name | Pin No. | Description | Remarks |
|---|---|---|---|
| LTOUT | 11 | • These pins are output pins for tone control. | |
| RTOUT | 26 | | |
| LT3 | 12 | • These pins are for connecting bass and treble compensation for the tone circuit.<br>Connect a high-band compensation capacitor between T1 and T2.<br>Connect a low-band compensation capacitor between T2 and T3. | |
| LT2 | 13 | | |
| LT1 | 14 | | |
| RT3 | 25 | | |
| RT2 | 24 | | |
| RT1 | 23 | | |
| LTIN | 15 | • These pins are tone control input pins.<br>• Low impedance driven. | |
| RTIN | 22 | | |
| $V_{DD}$ | 16 | • These pins are for connecting all power supplies. | |
| A. $V_{SS}$ | 21 | | |
| $V_{SS}$ | 20 | | |
| CE | 17 | • This is the chip enable pin. According to the timing of the switch from high to low, data is written to an internal latch and all analog switches operate.<br>Data transfer with high level switches to enable. | |
| DI | 18 | • These are input pins for the clock and serial data for control. | |
| CL | 19 | | |



## Equivalent Circuit for Main Volume Section

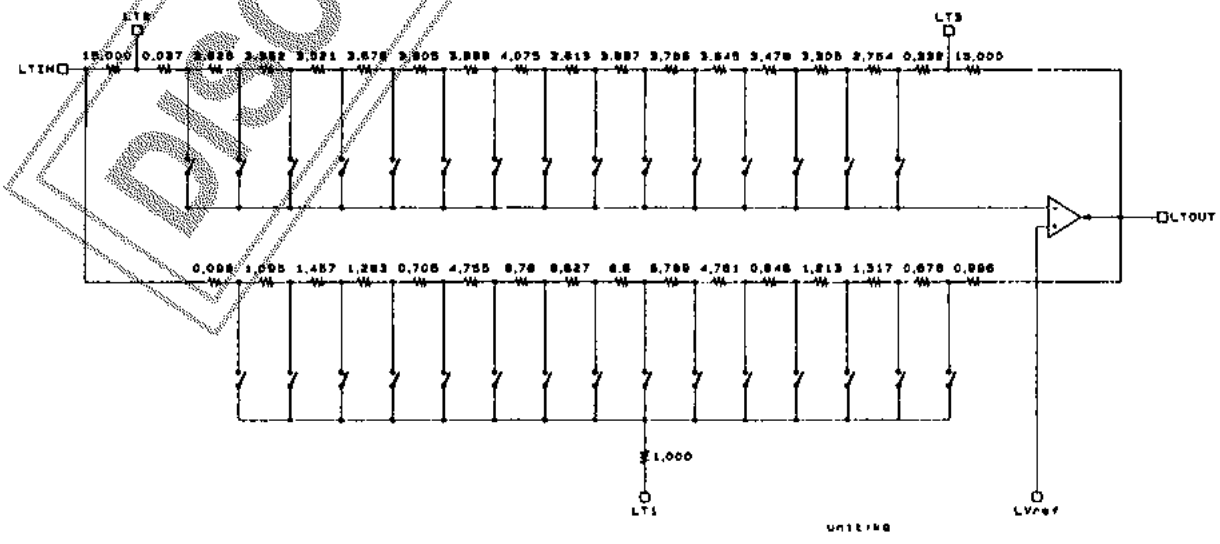


## Equivalent Circuit for Fader Volume Section



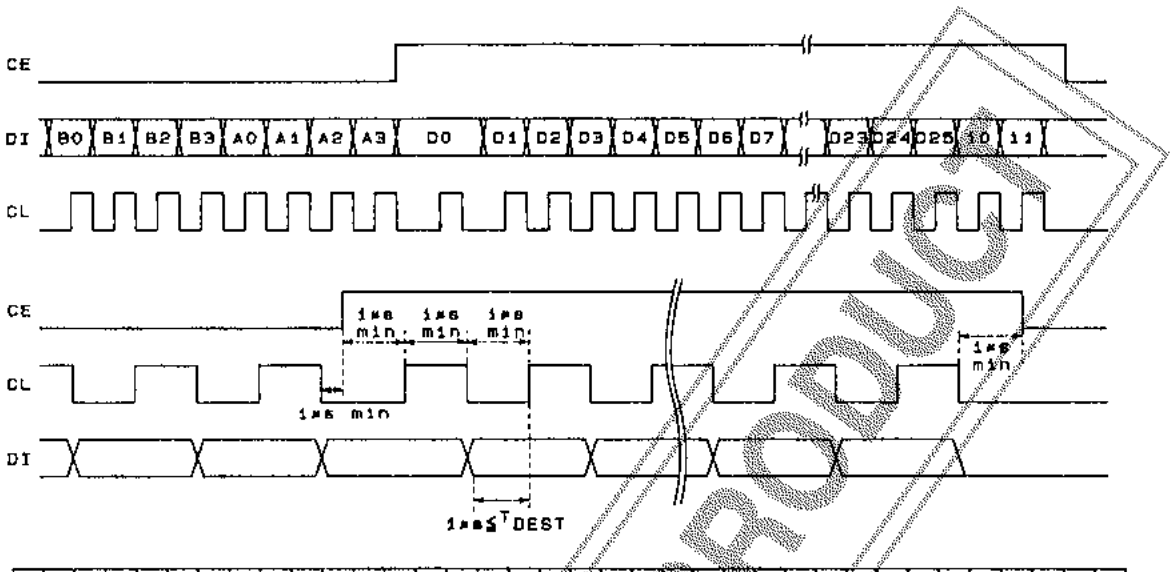

When data of $-\infty$ is transferred to main volume control 1 dB step, S1 and S2 open and are turned on simultaneously.

## Equivalent Circuit for Tone Section



## Control System Timing and Data Format

Controlling of LC7538NM involves the input of regulating serial data to CE, CL and DI pins. Data format consists of 36 bits composed of an 8-bit address and 28-bit data.




| B0 | B1 | B2 | B3 | A0 | A1 | A2 | A3 | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | D8 | D9 | D10 | D11 | D12 | D13 | D14 | D15 | D16 | D17 | D18 | D19 | D20 | D21 | D22 | D23 | D24 | D25 | 0 | 1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

Address Code

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

Don't care

Channel Selection

| | | | | |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | |
| 1 | 0 | 0 | 0 | :Rch |
| 0 | 1 | 0 | 0 | :Lch |
| 1 | 1 | 0 | 0 | :L/R simultaneously |

1 dB Step Control

| | | | | |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | :-∞ |
| 1 | 0 | 0 | 0 | :-4dB |
| 0 | 1 | 0 | 0 | :-3dB |
| 1 | 1 | 0 | 0 | :-2dB |
| 0 | 0 | 1 | 0 | :-1dB |
| 1 | 0 | 1 | 0 | : 0dB |

Rear/Front Control

| | |
|---|---|
| 0 | Rear |
| 1 | Front |

Loudness Control

| | |
|---|---|
| 0 | OFF |
| 1 | ON |

BASS Control

| | | | | |
|---|---|---|---|---|
| 1 | 1 | 1 | 0 | :Step15 |
| 0 | 1 | 1 | 0 | :Step14 |
| 1 | 0 | 1 | 0 | :Step13 |
| 0 | 0 | 1 | 0 | :Step12 |
| 1 | 1 | 0 | 0 | :Step11 |
| 0 | 1 | 0 | 0 | :Step10 |
| 1 | 0 | 0 | 0 | :Step9 |
| 0 | 0 | 0 | 0 | :Step8 |
| 1 | 0 | 0 | 1 | :Step7 |
| 0 | 1 | 0 | 1 | :Step6 |
| 1 | 1 | 0 | 1 | :Step5 |
| 0 | 0 | 1 | 1 | :Step4 |
| 1 | 0 | 1 | 1 | :Step3 |
| 0 | 1 | 1 | 1 | :Step2 |
| 1 | 1 | 1 | 1 | :Step1 |

TREBLE Control

| | | | | |
|---|---|---|---|---|
| 1 | 1 | 1 | 0 | :Step15 |
| 0 | 1 | 1 | 0 | :Step14 |
| 1 | 0 | 1 | 0 | :Step13 |
| 0 | 0 | 1 | 0 | :Step12 |
| 1 | 1 | 0 | 0 | :Step11 |
| 0 | 1 | 0 | 0 | :Step10 |
| 1 | 0 | 0 | 0 | :Step9 |
| 0 | 0 | 0 | 0 | :Step8 |
| 1 | 0 | 0 | 1 | :Step7 |
| 0 | 1 | 0 | 1 | :Step6 |
| 1 | 1 | 0 | 1 | :Step5 |
| 0 | 0 | 1 | 1 | :Step4 |
| 1 | 0 | 1 | 1 | :Step3 |
| 0 | 1 | 1 | 1 | :Step2 |
| 1 | 1 | 1 | 1 | :Step1 |

5dB Step Control

| | | | | |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | :-75dB |
| 1 | 0 | 0 | 0 | :-70dB |
| 0 | 1 | 0 | 0 | :-65dB |
| 1 | 1 | 0 | 0 | :-60dB |
| 0 | 0 | 1 | 0 | :-55dB |
| 1 | 0 | 1 | 0 | :-50dB |
| 0 | 1 | 1 | 0 | :-45dB |
| 1 | 1 | 1 | 0 | :-40dB |
| 0 | 0 | 0 | 1 | :-35dB |
| 1 | 0 | 0 | 1 | :-30dB |
| 0 | 1 | 0 | 1 | :-25dB |
| 1 | 1 | 0 | 1 | :-20dB |
| 0 | 0 | 1 | 1 | :-15dB |
| 1 | 0 | 1 | 1 | :-10dB |
| 0 | 1 | 1 | 1 | :- 5dB |
| 1 | 1 | 1 | 1 | : 0dB |

Fader Step Control

| | | | | |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | :-∞ |
| 1 | 0 | 0 | 0 | :-60dB |
| 0 | 1 | 0 | 0 | :-45dB |
| 1 | 1 | 0 | 0 | :-35dB |
| 0 | 0 | 1 | 0 | :-25dB |
| 1 | 0 | 1 | 0 | :-20dB |
| 0 | 1 | 1 | 0 | :-18dB |
| 1 | 1 | 1 | 0 | :-16dB |
| 0 | 0 | 0 | 1 | :-14dB |
| 1 | 0 | 0 | 1 | :-12dB |
| 0 | 1 | 0 | 1 | :-10dB |
| 1 | 1 | 0 | 1 | :- 8dB |
| 0 | 0 | 1 | 1 | :- 6dB |
| 1 | 0 | 1 | 1 | :- 4dB |
| 0 | 1 | 1 | 1 | :- 2dB |
| 1 | 1 | 1 | 1 | : 0dB |



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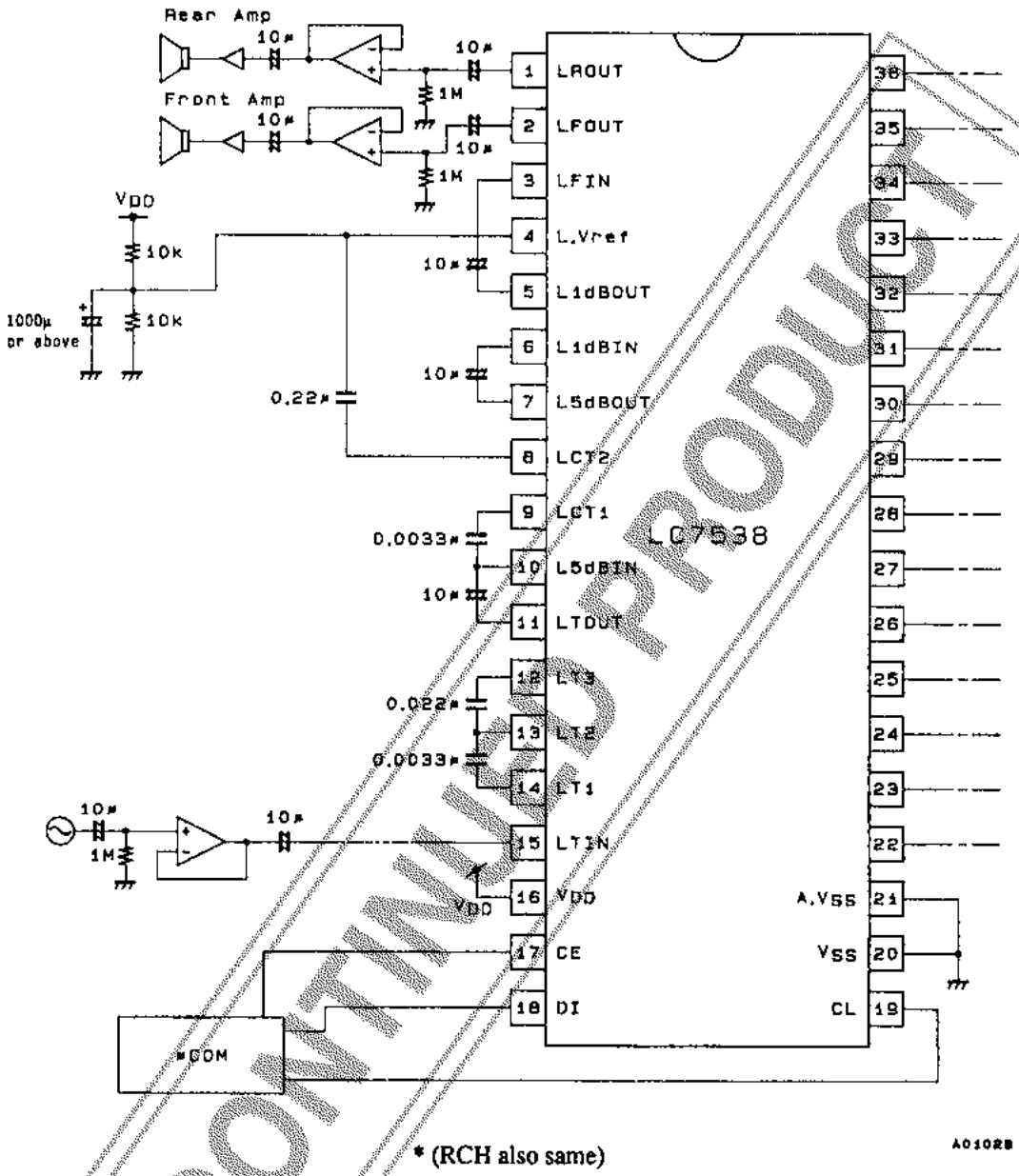
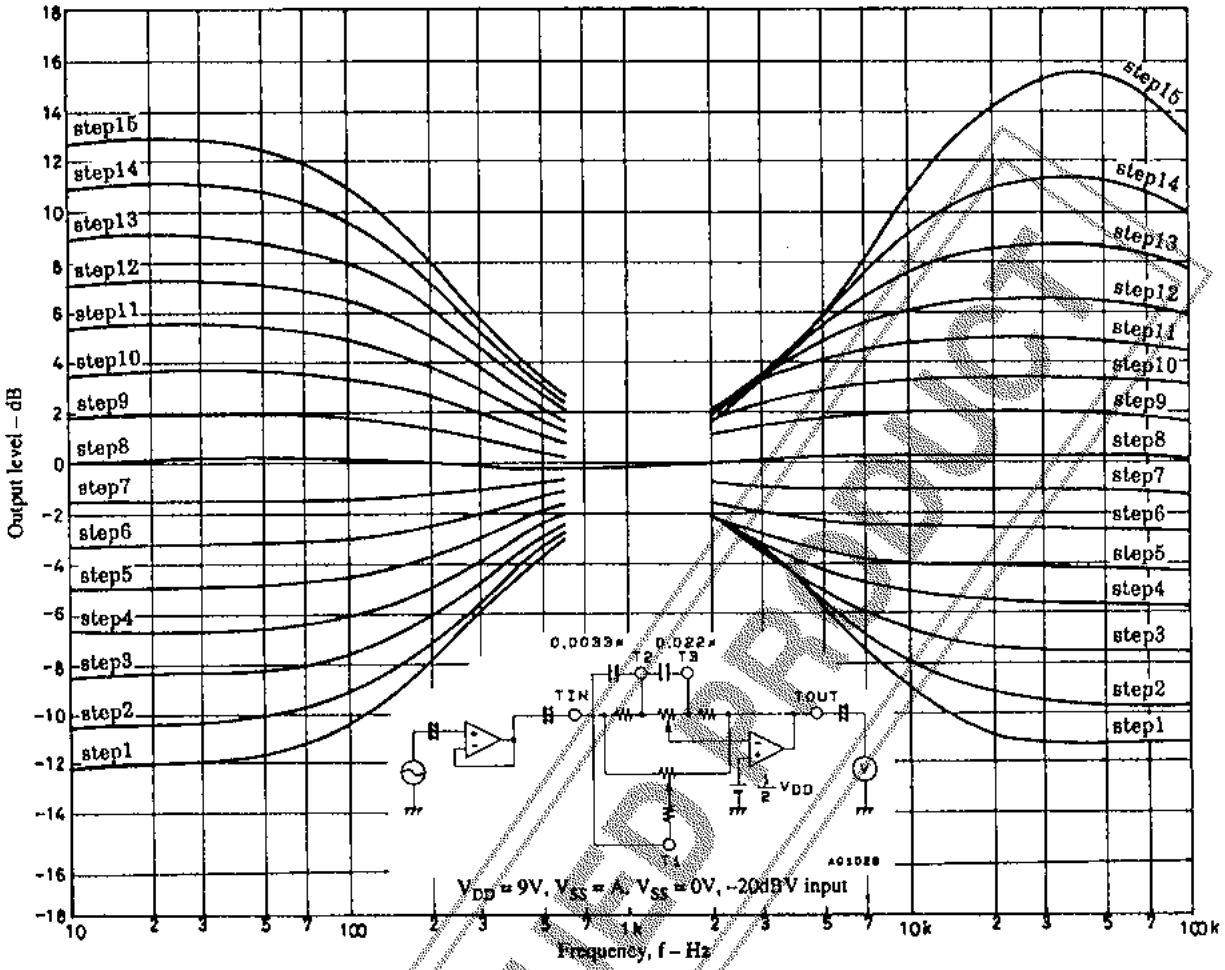
## Application Circuit Example



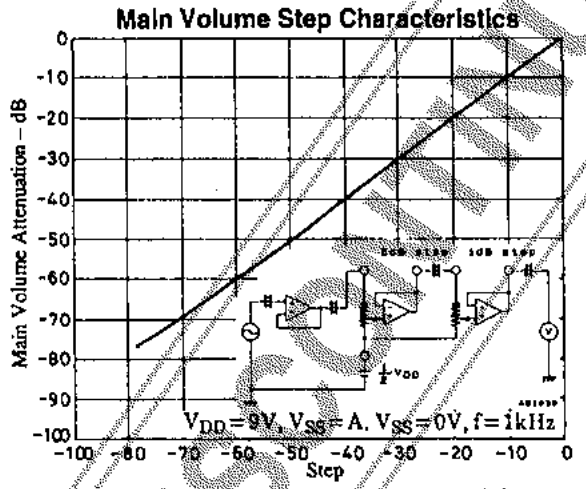

* (RCH also same)

Note: Bipolar electrolytic capacitors should be used as widely as possible others are not recommended directly.

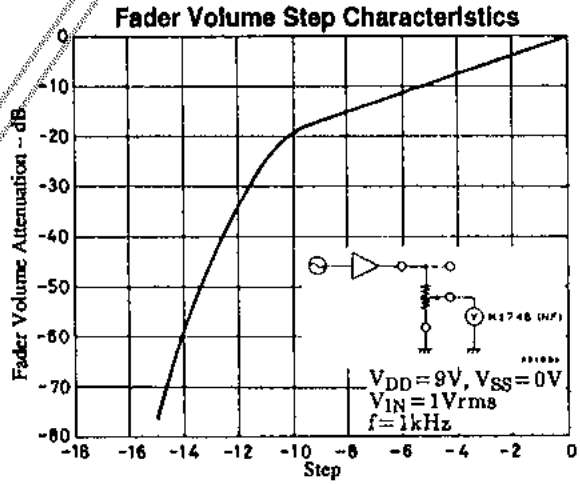
## Tone Characteristics



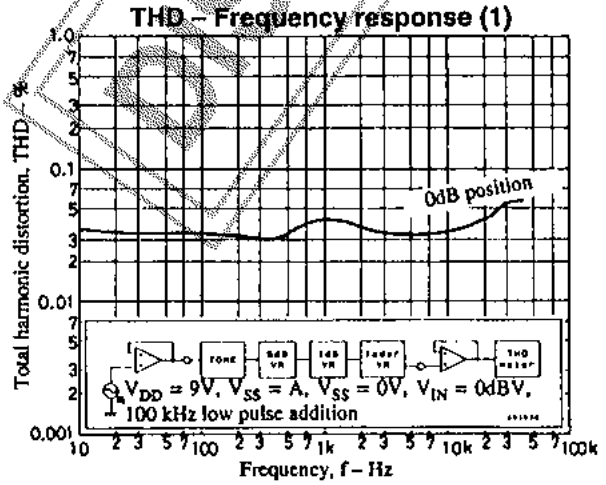

## Main Volume Step Characteristics



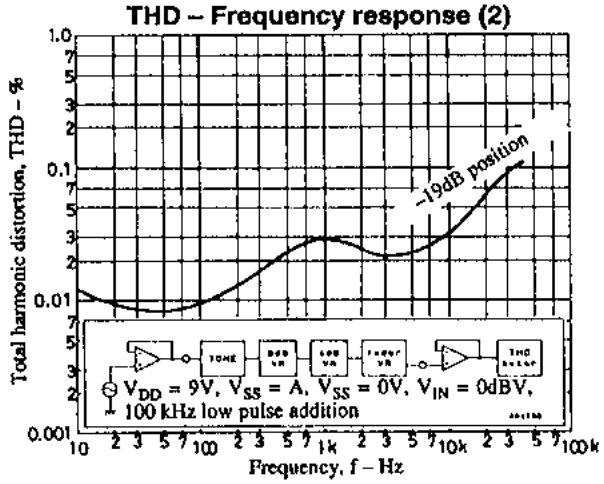

## Fader Volume Step Characteristics



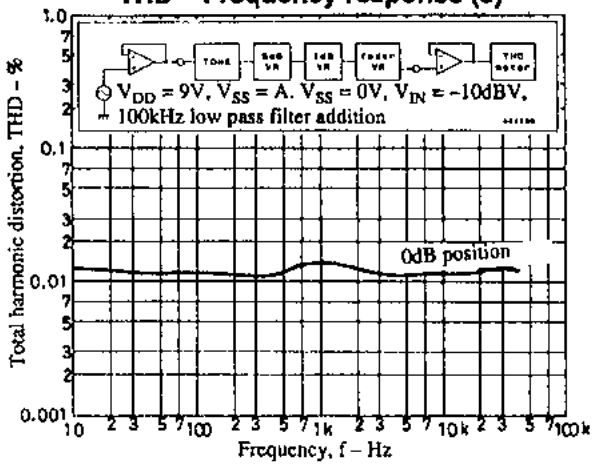

## THD – Frequency response (1)



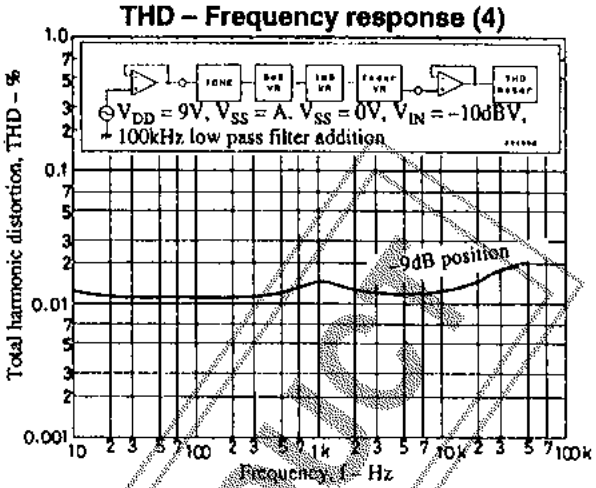

## THD – Frequency response (2)



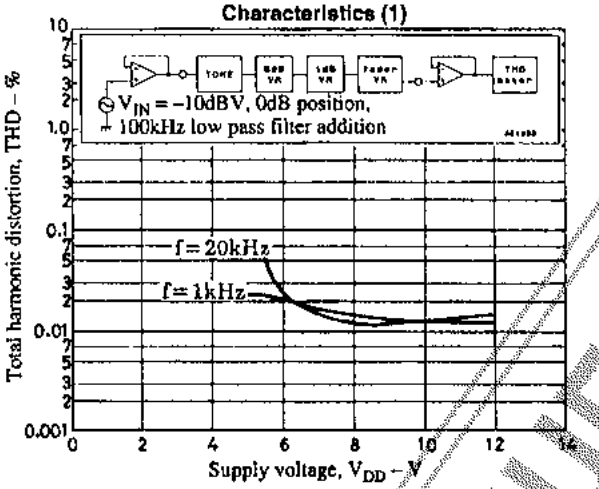
## THD – Frequency response (3)



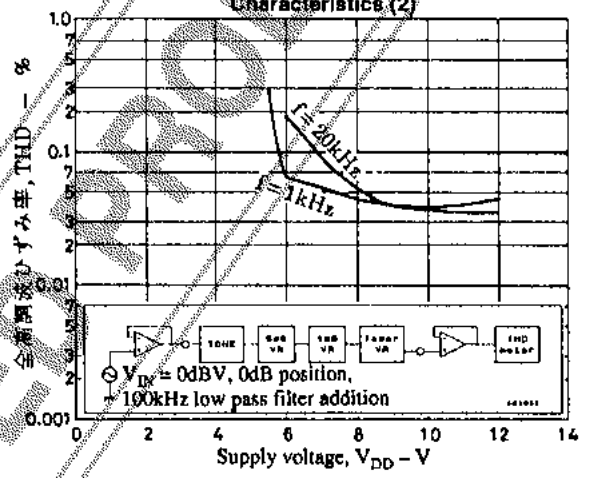

## THD – Frequency response (4)



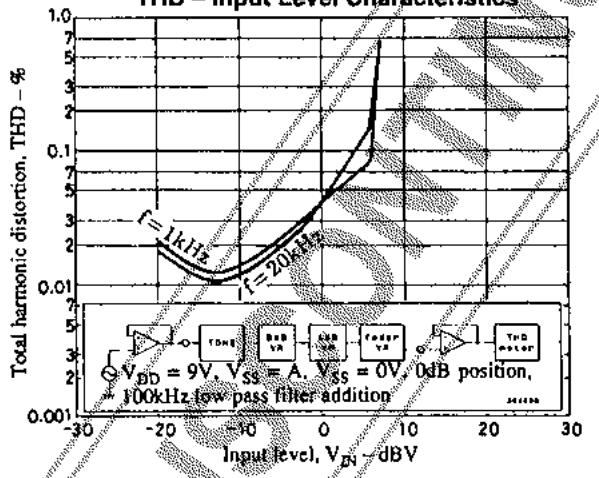

## THD – Power Supply Voltage Characteristics (1)



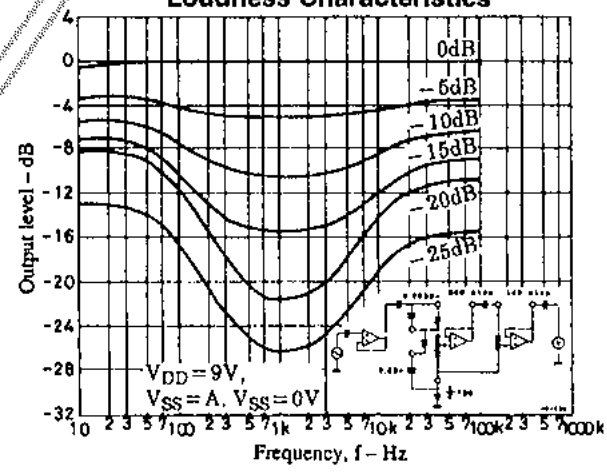

## THD – Power Supply Voltage Characteristics (2)




## THD – Input Level Characteristics




## Loudness Characteristics



## Loudness External Constant Calculation Sample

First, refer to page 5 where the 5 dB step internal equivalent circuit for the LC7538NM is shown. Using this information, an external constant for loudness can be added to establish a simplified circuit for computation as shown in figure 1. Computations gaining a 5 dB boost with f = 100 Hz using this configuration are shown in the following.
(f = 100 Hz and 5 dB boost)
Within figure 1, when R and C are defined as:

R1 = R2 = 10 kΩ
R3 = 1 kΩ
C1 =Z1, C2 = Z2, then the following equation can be established:

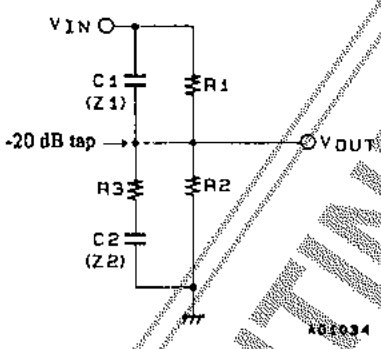
$$\underset{(at = 1kHz)}{VOUT} = \frac{\frac{R2\,(R3 + Z2)}{R2 + R3 + Z2}}{\frac{R1 \cdot Z1}{R1 + Z1} + \frac{R2\,(R3 + Z2)}{R2 + R3 + Z2}} = -20dB$$

$$\underset{(at = 100Hz)}{VOUT} = \frac{\frac{R2\,(R3 + 10 \cdot Z2)}{R2 + R3 + 10 \cdot Z2}}{\frac{R1 \cdot 10 \cdot Z1}{R1 + 10 \cdot Z1} + \frac{R2(R3 + 10 \cdot Z2)}{R2 + R3 + 10 \cdot Z2}} = -15dB$$

thereby resulting in,

Z1 ≒ 178.3 kΩ and Z2 = 176 Ω.

Under such conditions where f = 1 kHz, specifications may be satisfied if C (capacitor) having these impedances is supplied externally. The end result being that C1 = 893 pF and C2 = 0.9 μF.




R1, R2 and R3 : LC7538NM on-chip resistors
C1 : External high-band compensation capacitor
C2 : External low-band compensation capacitor

Figure 1

Notes for Above Applications

- When the power supply is turned on, the internal analog switch inexact. Until data is set, counter measures such as those required for muting are performed externally.
- In order to prevent crossover into the analog system of high-frequency digital signals transferred to the CL, DI and CE pins, transfer along these signal lines should occur along shielded lines or prevented using the grounding pattern or the circuit.