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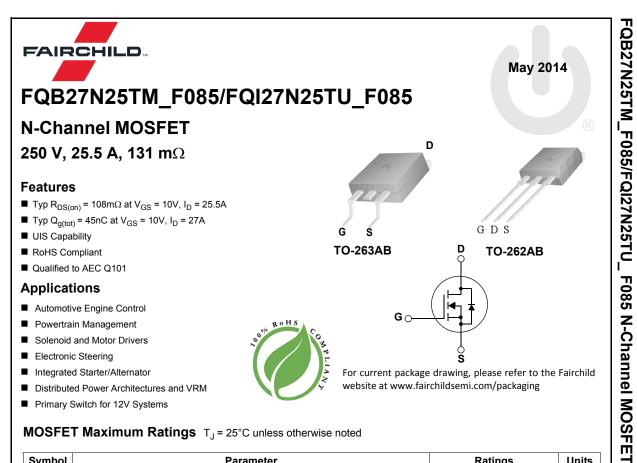


ON Semiconductor®

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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

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Symbol	Parameter		Ratings	Units
V _{DSS}	Drain to Source Voltage		250	V
V _{GS}	Gate to Source Voltage		±30	V
I _D	Drain Current - Continuous (V _{GS} =10) (Note 1)	T _C =25°C	25.5	
	Pulsed Drain Current	T _C = 25°C	See Figure 4	A
E _{AS}	Single Pulse Avalanche Energy (Note 2)		972	mJ
P _D	Power Dissipation		417	W
	Derate above 25°C		3.3	W/ºC
T _J , T _{STG}	Operating and Storage Temperature		-55 to + 150	°C
$R_{\theta JC}$	Thermal Resistance, Junction to Case		0.3	°C/W
$R_{\theta JA}$	Maximum Thermal Resistance, Junction to Ambient (Note 3)		43	°C/W

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FQB27N25TM	FQB27N25TM_F085	TO-263AB	330mm	24mm	800 units
FQI27N25TU	FQI27N25TU_F085	TO-262AB	Tube	N/A	50 units

Notes:

1: Current is limited by bondwire configuration.

Starting T_J = 25°C, L = 4.67mH, I_{AS} = 20.4A, V_{DD} = 100V during inductor charging and V_{DD} = 0V during time in avalanche.
 R_{θJA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{θJC} is guaranteed by design while R_{θJA} is determined by the user's board design. The maximum rating presented here is based on mounting on a 1 in² pad of 2oz copper.

Symbol	Parameter	Test	Conditions	Min.	Тур.	Max.	Unit
Off Cha	racteristics						
BVDSS	Drain to Source Breakdown Voltage	I _D = 250μA, V	/ _{GS} = 0V	250	-	-	V
	Drain to Source Leakage Current	V _{DS} =250V,	$T_J = 25^{\circ}C$	-	-	1	μA
DSS	Drain to Source Leakage Current	$V_{GS} = 0V$	$T_{J} = 150^{\circ}C(Note 4)$	-	-	250	uA
GSS	Gate to Source Leakage Current	$V_{GS} = \pm 30V$		-	-	±100	nA
GS(th)	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu A$ $I_D = 25.5A, T_J = 25^{\circ}C$		3.0	4.1	5.0	V mO
	racteristics				4		
				-	108	131	mΩ
DS(on)	Drain to Source On Resistance	V _{GS} = 10V	$T_{\rm J} = 150^{\rm o} {\rm C}({\rm Note}\;4)$	-	265	310	mΩ
nami s	Input Capacitance Output Capacitance	− V _{DS} = 25V, V _{GS} = 0V, − f = 1MHz		-	1800 350	-	pF pF
rss	Reverse Transfer Capacitance			-	45	-	pF
₹g	Gate Resistance	f = 1MHz		-	0.82	-	Ω
Q _{g(ToT)}	Total Gate Charge at 10V	V _{GS} = 0 to 10	V V _{DD} = 125V	-	45	49	nC
Q _{g(th)}	Threshold Gate Charge	$V_{GS} = 0$ to $2V$	/ I _D = 27A	-	3.3	4	nC
) _{gs}	Gate to Source Gate Charge			-	12	-	nC
2 _{gd}	Gate to Drain "Miller" Charge			-	23	-	nC

Switching Characteristics

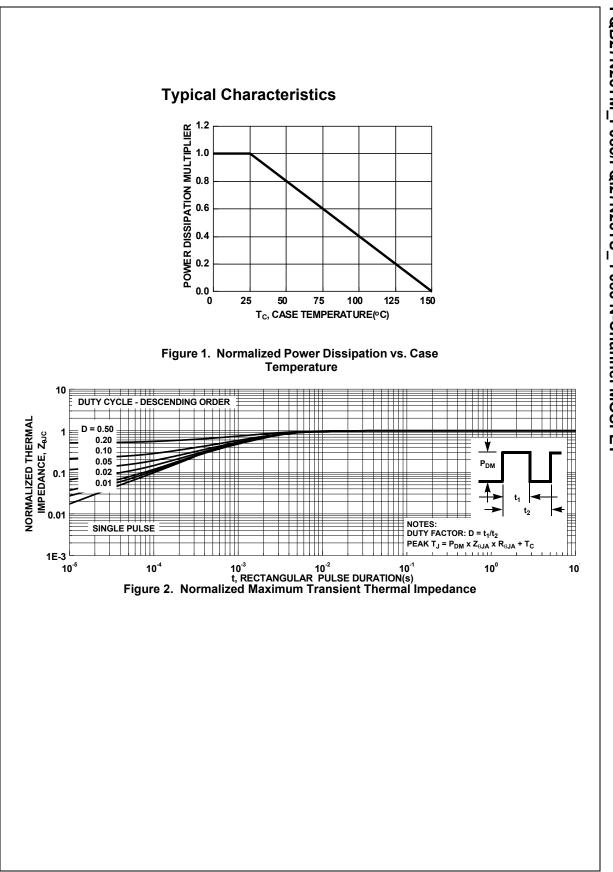
t _{on}	Turn-On Time		-	-	196	ns
t _{d(on)}	Turn-On Delay		-	36	-	ns
t _r	Rise Time	V _{DD} = 125V, I _D = 27A, V _{GS} = 10V, R _{GEN} = 25Ω	-	122	-	ns
t _{d(off)}	Turn-Off Delay	V _{GS} = 10V, R _{GEN} = 25Ω	-	81	-	ns
t _f	Fall Time		-	60	-	ns
t _{off}	Turn-Off Time		-	-	164	ns

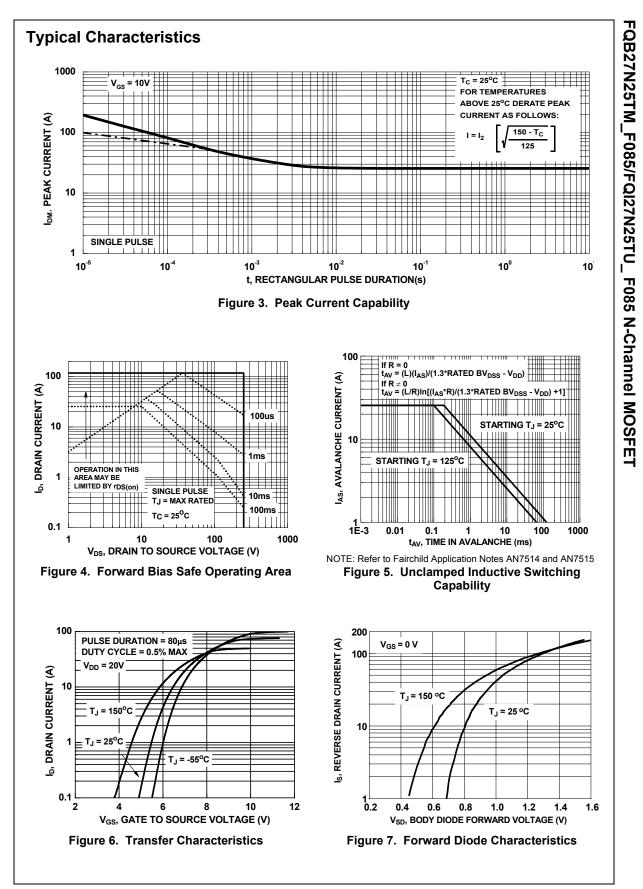
Drain-Source Diode Characteristics

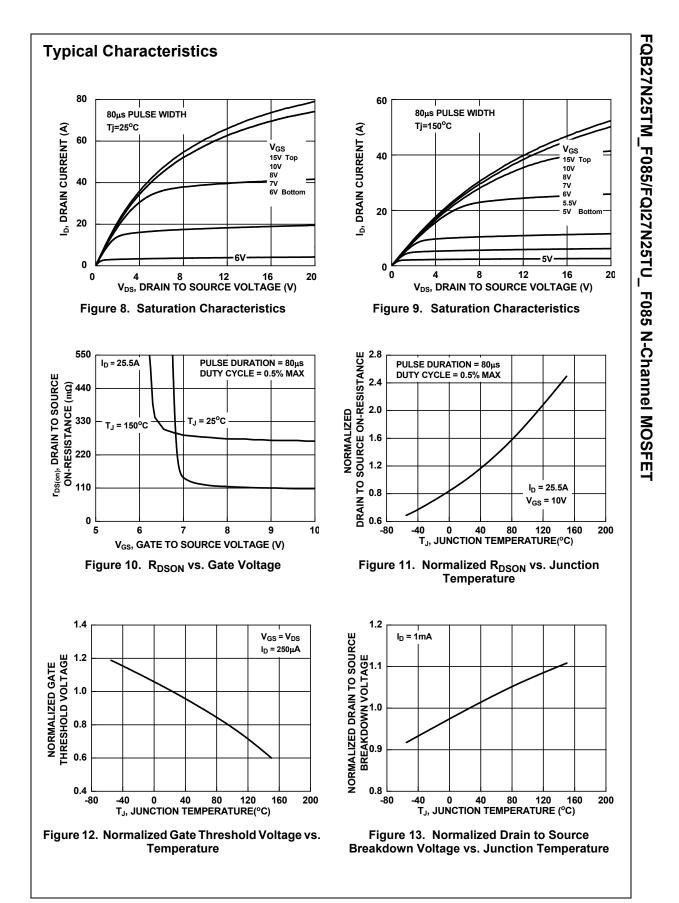
V _{SD}	Source to Drain Diode Voltage	I _{SD} = 25.5A, V _{GS} = 0V	-	-	1.5	V
		I _{SD} = 12.75A, V _{GS} = 0V	-	-	1.25	V
t _{rr}	ReverseRecovery Time	I _F = 27A, dI _{SD} /dt = 100A/μs,	-	205	238	ns
Q _{rr}	ReverseRecovery Charge	V _{DD} =200V	-	1.8	2.3	nC

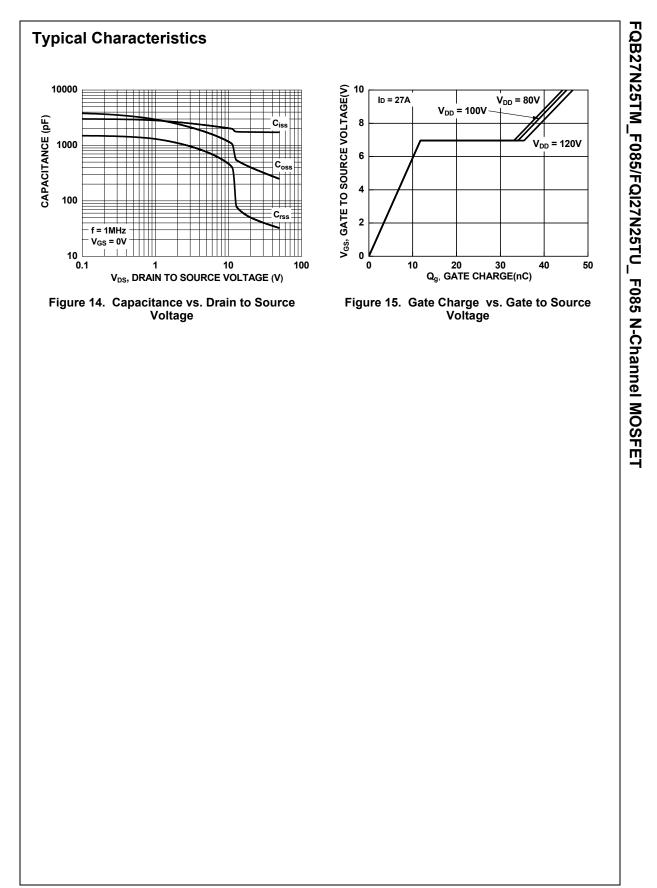
Notes:

4: The maximum value is specified by design at T_J = 150°C. Product is not tested to this condition in production.











Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed Full Production		Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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