

# BL6552 Professional chip for three phase power monitoring and analysis Data sheet

V1.1

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# 1. Product description

Bl6552 is a 7-channel three-phase power monitoring and analysis chip, which is suitable for three-phase intelligent circuit breaker, three-phase guide rail meter, electrical measuring instrument, power supply monitoring of high-power equipment and other applications, with high cost performance.

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BL6552 integrates seven high-precision Sigma-Delta ADCs, reference voltage circuits, temperature sensors and other analog circuit modules, as well as digital signal processing circuits for processing electrical parameters such as power, effective value, energy, and temperature. It can be used to measure three-phase and The total (fundamental and harmonic) active power and energy, reactive power and energy, apparent power and energy of the combined phase; and fundamental active power and energy, reactive power and energy; and the effective value of current and voltage of each phase , Power factor and other parameters; with current loss monitoring, current and voltage peak detection, zero-crossing detection and other power quality management; it can give real-time waveforms.

bl6552 integrates spi and uart interfaces to facilitate the transfer of metering parameters and calibration parameters with external MCUs.

bl6552 internally uses data flow calculation methods to process various signals, and has good reliability in the case of external interference. The internal voltage monitoring circuit can ensure normal operation when power is turned on and off.

# 2、 Basic Features

#### 2.1 main feature

✓ High precision, the non-linear error of active power within the input dynamic range of 8000:1 is less than 0.1%

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- ✓ High stability, the output pulse signal bounces within the input dynamic range of 8000:1<0.02%@Ib</p>
- ✓ Provide zero-line current input sampling
- ✓ Give each phase and total (fundamental and harmonic) active, reactive, and apparent power (24bit, support two calculation methods); and fundamental active and reactive power (24bit)
- ✓ Given the effective value of each phase voltage and current (24bit), the relative error within the detection range of 3000:1 is less than 0.1%
- Provide waveform sampling data of each phase voltage, current and neutral current (24bit)
- ✓ Give the total (fundamental and harmonic) active, reactive, and apparent energy (24bit)
- ✓ Give the total (fundamental and harmonic) active and reactive line period energy
- ✓ Give the total (fundamental and harmonic) positive and negative active energy
- ✓ Give the combined and four-quadrant reactive energy
- ✓ Gives 300 real-time waveforms per week
- ✓ Give power factor
- ✓ With fast effective value output
- ✓ Give voltage and current phase angle measurement
- ✓ Fast pulse output with active energy and reactive energy
- $\checkmark$  With voltage loss and phase failure detection function

- With current loss detection function
- ✓ With current and voltage peak detection and zero-crossing detection functions
- ✓ With frequency detection
- ✓ Programmable anti-creep threshold setting
- ✓ Programmable adjustment of pulse output frequency
- Programmable active power, reactive power, apparent power error and gain adjustment
- ✓ Programmable input active phase compensation
- ✓ The interrupt request signal can be given as needed to facilitate the control with the external MCU
- ✓ With uarttspi communication interface for easy data transmission
- ✓ Built-in 1.2v reference voltage source
- ✓ Single power supply 3.3v
- ✓ QFN36 PACKAGE

2.2 System Block Diagram



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It is mainly divided into analog signal processing and digital signal processing. The analog part mainly includes 7-channel high-precision Sigma-Delta ADC and related analog modules, and the digital part is a digital signal processor and related modules.

#### 2.3 Pin arrangement

#### QFN36 PACKAGE

Se		in	
ri		pu	
al	na	t	descerintion
nu	me	0u	description
mb		tp	
er		ut	

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1	IN P	en te r	ositive terminal input of neutral current channel						
2	VR EF	in pu t Ou tp ut	Reference voltage 1.2v						
3	VA N	en te r	A phase voltage channel negative terminal input, the maximum differential voltage of each pair of pins is $\pm 0.7 v$						
4	VA P	en te r	A phase voltage channel positive input						
5	VB N	en te r	B-phase voltage channel negative terminal input, the maximum differential voltage of each pair of pins is $\pm 0.7 v$						
6	VB P	en te r	B-phase voltage channel positive terminal input						
7 $VC$ en C-phase voltage channel negative terminal N te maximum differential voltage of each pair $\pm 0.7v$			C-phase voltage channel negative terminal input, the maximum differential voltage of each pair of pins is $\pm 0.7 v$						
8	VC P	en te r	C-phase voltage channel positive terminal input						
9	NR ST	en te r	Reset, active low						
10	AG ND	Po we r gr ou nd	Analog ground						
11	DG ND	Po we r gr ou nd	Digitally						

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12	_C S	en te r	SPI CHIP SELECTION UART RATE SELECTION					
13	SD O	Ou tp ut	SPIIUART SEND TX					
14	SD I	en te r	SPIIUART RECEIVES RX					
15	SC LK	en te r	SPI CLOCK UART RATE SELECTION					
16	_I RQ 1	Ou tp ut	Interrupt status logic output 1					
17	_I RQ 2	Ou tp ut	Interrupt status logic output 2					
18	CL KO UT	Ou tp ut	Crystal pin					
19	CL KI N	en te r	Crystal oscillator pin, external crystal oscillator frequency 8MHz					
20	VP P	po we r su pp ly	Reserved, can be suspended					
21	CF 1	Ou tp ut	Calibration pulse 1 (active power)					
22	CF 2	Ou tp ut	Calibration pulse 2 (reactive power)					
23	AT 1	Ou tp ut	Logic output pin, configurable output indication 1					
24	AT 2	Ou tp ut	Logic output pin, configurable output indication 2					

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95	AT	0u	Levie autout ain confirmable autout indication 2						
20	3	ut ut	Logic output pin, configurable output indication 5						
	DV	Ou							
26	DD	tp	Digital module voltage 1.8V, external 0.1uF filter						
	18	ut	capacitor						
	SE	en							
27	L	te	Default O, select Uart; 1, select SPI						
		r							
		we							
	DV	r							
28	DD	su	Power 3.3v						
		pp							
		1y							
		ро							
		we							
29	AV	r	Power 3.3v						
	DD	su							
		pp							
		en	C-phase current channel negative terminal input, the						
30	IC	te	maximum differential voltage of each pair of pins is						
	Ν	r	±0.7v						
	IC P	en							
31		te	C-phase current channel positive terminal input						
		r							
20	IB	en	B-phase current channel negative terminal input, the						
32	Ν	te	maximum differential voltage of each pair of pins is						
		n En							
33	ΙB	te	B-phase current channel positive terminal input						
	Р	r	r r r r r r r r r r r r r r r r r r r						
	ТΛ	en	A phase current channel negative terminal input, the						
34	IA N	te	maximum differential voltage of each pair of pins is						
	11	r	$\pm 0.7 v$						
0.5	IA	en							
35	Р	te	A phase current channel positive terminal input						
		Г оп	The negative terminal input of the neutral current						
36	IN	te	channel, the maximum differential voltage of each pair of						
50	Ν	r	pins is $\pm 0.7v$						



# 2.4 Performance

# 2.4.1 Electrical parameter performance index

Parameter	Symbol	Test Condition	Measure Pin	Min	Тур	Max	Unit
Active power measurement error	watt <sub>err</sub>	8000:1 input DR			0.1		%
Reactive power	var <sub>err</sub>	8000:1 input DR			0.1		%
measurement							
error							
Phase angle							
between channels	$pf08c_{\rm err}$	Phase lead 37°			0.1		%
causes	$pf051_{err}$	Phase lag 60°			0.1		%
measurement							
errors							
(PF=0.8							
CAPACITIVE)							
(PF=0.5							
INDUCTIVE)							
AC POWER SUPPLY	$ac_{psrr}$	Current channel			0.01		%
SUPPRESSION	$dc_{psrr}$	current input pin			0.1		%
(Change in		IP\IN@100mV, voltage					
output frequency		channel input pin					
range)		VP\VN=100mV,					
DC POWER SUPPLY							
SUPPRESSION							
(Change in							
output frequency							
range)							
Voltage RMS	$vrms_{\rm err}$	3000:1 input DR			0.1		%
measurement							
accuracy,							
relative error							
Current RMS	$irms_{\rm err}$	3000:1 input DR			0.1		%
measurement							
accuracy,							
relative error							
Analog input							
Input level		Differential input				1000	mV
(peak)				370			kΩ
input resistance					14		kHz

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		<b>BIG55</b>	Three phase	e power ma	onitoring a	and analys	eis and a second
Bandwidth (-3dB)		External 1.25				4	%
Gain error		reference voltage				3	%
Phase gain		External 1.25					
matching error		reference voltage					
Internal voltage	Vref				1.2		V
reference	$Vref_{err}$						mV
Baseline	TempCoef				20		ppm/℃
deviation							
Temperature							
Coefficient							
Logic input							
NRST, RXXSDI,							
SCLK,, CS		DVDD=3. $3V \pm 2.5\%$					
Input high level		DVDD=3. $3V \pm 2.5\%$		2.6			V
Input low level						0.8	V
Logic output							
TXXSDO,							
CF1_WATT,							
CF2_VAR		DVDD=3. $3V \pm 2.5\%$		2.6			V
Output high		DVDD=3.3V $\pm$ 2.5%				1	V
level							
Output low level							
power supply							
AVDD, DVDD	$V_{\mathrm{avdd}}$			3	3.3	3.6	V
DVDD18	$V_{\rm dvdd18}$	DVDD18=1.8V		1.6	1.8	2	V
AVDD	$I_{\rm avdd}$	AVDD=3.3			6	9	mA
DVDD	$I_{dvdd}$	DVDD=3.3			6	9	mA

# 2.4.2 Limit range

$(T = 25 \ ^{\circ}C)$			
project	symbol	extremum	unit
Power supply voltage vdd	AVDD, DVDD	-0.3 ~ +4	V
Power supply voltage dvdd18	DVDD18	-0.3 ~ +2.5	V
Programming voltage	VPP	-0.3 ~ +15	V
Analog input voltage (relative to gnd)	ICN, ICP, IBN, IBP, IAN, IAP, INN, INP, VCN, VCP, VBN, VBP, VAN, VAP	$-1 \sim +AVDD$	V
Analog output voltage (relative to gnd)	VREF	-0.3 ~ +AVDD	V

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Digital input voltage	SEL, NRST, RXXSDI, SCLK,,	-0.3 ~	V
(relative to gnd)	CS, SEL	AVDD+0.3	v
Digital output voltage	CE mott CE wor TVVSDO	-0.3 ~	V
(relative to gnd)	CF_watt, CF_var, TAASDO	AVDD+0.3	v
Operating temperature	Topr	$-40$ $\sim$ $+85$	°C
Storage temperature	Tstr	$-55$ $^{\sim}$ $+150$	°C
Power consumption	D	200	wW
(qfn36)	Γ	200	ШW

# 3, working principle

# 3.1 Principle of current and voltage waveform generation

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A total of 7 high-precision ADCs, using double-ended differential signal input: channel N input signal VP[N] and VN[N]. 7 channels of waveform output, including 4 channels of current and 3 channels of voltage. In each channel (The current and voltage are the same), the input signal passes the analog module amplifier (PGA) and highprecision analog-to-digital conversion (ADC) to get 1bit PDM to the digital module, the digital module is phase-calibrated, down-sampling filter (SINC3), optional high-pass After the filter (HPF) or the fundamental low-pass filter, through the gain and offset correction modules, the required current waveform data and voltage waveform data (I(N)\_WAVE, V(N)\_WAVE) are obtained.

The 7-channel pga gain is adjustable (0000=1; 0001=2; 0010=8; 0011=16), see the gain register for adjustment.

address	Name	Bit width	Defaults	description
60	GAIN1	24	0x000000	Channel pga gain adjustment register:

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Ê				<b>16552</b> Three phase power monitoring and analysis
				[11:8]:C-PHASE CURRENT
				[15:12]:B PHASE CURRENT
				[19:16]:A PHASE CURRENT
				[23:20]:Neutral line current
				Channel pga gain adjustment register:
(1	CADIO	AIN2 20	0x00000	[11:8]:A PHASE VOLTAGE
01	GAIN2			[15:12]: PHASE B VOLTAGE
				[19:16]:C PHASE VOLTAGE

#### 3.1.1 Active phase compensation

At the adc output position, a digital calibration method for small phase errors is provided. It can introduce a small time delay or lead into the signal processing circuit to compensate for small phase errors. Because this compensation must be timely, this This method is only suitable for small phase errors of <0.574 (range. Using time-shift technology to correct large phase errors will introduce significant phase errors in higher harmonics.

Since the transformer at the analog input terminal may have inconsistent angle differences when input signals of different amplitudes, increase the angle differential section compensation setting to allow three-section angle differential compensation.





#### Current channel angle differential segment definition register:

address	Name	Bit width	Defaults	description
				The angle difference segment point defines
62	IRMS_P1	24	0x010000	P1, which satisfies
				IRMSmin <p1<p2<irmsmax< td=""></p1<p2<irmsmax<>
63 IRMS_P2			The angle difference segment point defines	
	IRMS_P2	24	0x200000	P2, which satisfies
				IRMSmin <p1<p2<irmsmax< td=""></p1<p2<irmsmax<>

The phase calibration register is a binary 24-bit register, and the data format of each

register is as follows:

address	Name	Bit width	Defaults	description

	Na m	iia <i>"</i>		
	SHANGHAI BELL		BG	<b>552</b> Three phase power monitoring and analysis
				A phase current channel angle difference
				correction register, when
				IRMSmin <effective input<="" of="" td="" value=""></effective>
				current <p1, [7:0]="" channel<="" current="" is="" td="" the=""></p1,>
				phase used for correction, [7] is the enable
				bit, the minimum adjustment delay time is
				250ns, corresponding to 0.0045 Degree
		AL 24 0	0x000000	1LSB, the maximum adjustable is $\pm 0.574$
64	IA PHCAI			degrees). When P1 <effective of<="" td="" value=""></effective>
01				input current <p2, [15:8]="" correct<="" is="" td="" to="" used=""></p2,>
				the current channel phase, [15] is the
				enable bit, and the adjustment accuracy is
				the same as above. When P2 <the< td=""></the<>
				effective value of input current <irmsmax,< td=""></irmsmax,<>
				[23:16] is the current channel phase used
				for correction, [23] is the enable bit, and
				the adjustment accuracy is the same as
			above.	
65	IB PHCAL	24	0x000000	B-phase current channel angle difference
			5400000	correction register (same as above)

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66	IC PHCAI	24	0*000000	C-phase current channel angle difference
00	IC_ITICAL	27		correction register (same as above)
				Phase A voltage channel angle correction
				register, when IRMSmin <effective of<="" td="" value=""></effective>
				input current <p1, [7:0]="" is="" td="" the="" voltage<=""></p1,>
				channel phase used for correction, [7] is
				the enable bit, the minimum adjustment
				delay time is 250ns, corresponding to
				0.0045 Degree 1LSB, maximum adjustable
		A_PHCAL 24		$\pm$ 0.574 degrees). When P1 <effective< td=""></effective<>
67	VA_PHCAL		0x000000	value of input current <p2, [15:8]="" is="" td="" to<="" used=""></p2,>
			correct the current the enable bit, and is the same as above effective value of the current <irmsmaxe correct the phase of [23] is the enable b</irmsmaxe 	correct the current channel phase, [15] is
				the enable bit, and the adjustment accuracy
				is the same as above. When P2 <the< td=""></the<>
				effective value of the input
				current <irmsmax, [23:16]="" is="" td="" to<="" used=""></irmsmax,>
				correct the phase of the voltage channel,
				[23] is the enable bit, and the adjustment
				accuracy is the same as above.
68	VB DUCAL	24	0000000	B-phase voltage channel angle difference
00	vD_rHCAL	24	0x000000	correction register (same as above)

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· 1			

60	VC BHCAI	24	0000000	C-phase voltage channel angle difference
09		24	0x000000	correction register (same as above)
				IN phase current channel angle difference
				correction register, when
				IRMSmin <effective input<="" of="" td="" value=""></effective>
				current <p1, [7:0]="" correct="" is="" td="" the<="" to="" used=""></p1,>
				current channel phase, [7] is the enable bit,
				the minimum adjustment delay time is
				250ns, corresponding to 0.0045 Degree
				1LSB, maximum adjustable $\pm 0.574$
			degrees). When IRMSmin <effective td="" value<=""></effective>	
90	IN_PHCAL	24	0x000000	of input current <p1, [7:0]="" is="" td="" to<="" used=""></p1,>
			correct the current channel phase, [7] is the	
			enable bit, and the minimum adjustment	
				delay time is 280ns , Corresponding to
			0.005 degrees 1LSB, the maximum	
			adjustable is $\pm 0.625$ degrees). When	
				P1 <effective current<p2,<="" input="" of="" td="" value=""></effective>
				[15:8] is used to correct the phase of the
			current channel, [15] is the enable bit, and	
				the adjustment accuracy is the same as

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		above .When P2 <effective input<="" of="" th="" value=""></effective>
		current <irmsmax, [23:16]="" is="" td="" to<="" used=""></irmsmax,>
		correct the current channel phase, [23] is
		the enable bit, and the adjustment accuracy
		is the same as above.

#### 3.1.2 Channel offset correction

Contains 7 16-bit channel offset calibration registers CHOS[N], the default value is 0x0000.

These registers can be used for digital calibration or error pre-calibration before leaving the factory.

They use the data in the form of 2's complement to eliminate the deviation caused by the analog-to-digital conversion of the current channel and the voltage channel. The deviation here may be caused by the input and the offset generated by the analog-todigital conversion circuit itself. The deviation correction can be used in no load In this case, the waveform offset is 0.

address	Name	Bit width	Defaults	description
10		5 16 0x00	0,0000	Corresponding channel offset adjustment
AC	IC_CHOS		0x0000	register, complement
		0-0000	Corresponding channel offset adjustment	
πD	ID_CHOS	10	0x0000	register, complement

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	8			R GF	52 Three phase power monitoring and analysis
_	ΔE	IA CHOS	16	00000	Corresponding channel offset adjustment
		M_CHO5	10	0x0000	register, complement
	AF	IN CHOS	16	0x0000	Corresponding channel offset adjustment
	711		10		register, complement
	B2	VA CHOS	16	0-0000	Corresponding channel offset adjustment
	02	VA_0103	10	0x0000	register, complement
	B3	VB CHOS	16	0~0000	Corresponding channel offset adjustment
	05	VD_C1103	10	0x0000	register, complement
	B4	VC CHOS	16	0~0000	Corresponding channel offset adjustment
	D4	vC_CHO3	10	020000	register, complement

These registers are used for channel deviation calibration

Correction formula:

#### WAVE[N] = WAVE0[N] + CHOS[N] \* 2

Among them, wave0[n] is the measured value of the nth channel, chos[n] is the

calibration value, and wave[n] is the output value after calibration.

#### 3.1.3 Channel gain correction

Contains 7 16-bit channel gain calibration registers CHGN[N], the default value is

0x0000.

These registers can be used for digital calibration or error pre-calibration before

leaving the factory.

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They use 2's complement data to adjust the gain error caused by the analog-todigital conversion of the current channel and the voltage channel. The error here may be caused by the input and the analog-to-digital conversion circuit itself. The gain correction can be made in the range of  $\pm$  50% Internal adjustment.

address	Name	Bit width	Defaults	description
Δ.1	IC CHON	16	00000	Corresponding channel gain adjustment
Δ	IC_CHGN	10	0x0000	register, complement
4.2	IB CHCN	16	0x0000	Corresponding channel gain adjustment
ΠZ	ID_CHGN	10	0x0000	register, complement
A 3	IA CHCN	16	0x0000	Corresponding channel gain adjustment
ΛJ	IA_CHGN	10	0x0000	register, complement
A A	IN CHCN	16	0x0000	Corresponding channel gain adjustment
114	IN_CITON	10	0x0000	register, complement
Α7	VA CHCN	16	0×0000	Corresponding channel gain adjustment
11/	WI_CHON	10	0x0000	register, complement
4.0	VR CHCN	16	00000	Corresponding channel gain adjustment
110	VD_CHGN	10	0x0000	register, complement
4.0	VC CHCN	16	0x0000 ft 0x0000 ft 0x0000 ft 0x0000 ft 0x0000 ft	Corresponding channel gain adjustment
177	VC_CHGN	10	0x0000	register, complement

These registers are used for channel gain calibration.



Correction formula:

$$WAVE[N] = WAVE0[N] * (1 + \frac{CHGN[N]}{2^{16}})$$

Among them, wave0[n] is the measured value of the nth channel, chgn[n] is the gain calibration value, and wave[n] is the calibration output value.

#### 3.1.4 Current and voltage waveform output

The current load current and voltage waveform data can be collected, the sampling current and voltage are updated at a rate of 15.6ksps, and 300 points can be sampled per cycle. Each sampled data is a 24bit signed number and stored in the waveform register (I(N)\_WAVE), V[N]\_WAVE). The SPI rate is greater than 1.5Mbps, and the waveform values of multiple channels can be read continuously.

The channel can be selected through hpf and fundamental lpf, and finally a 7channel waveform is obtained.

address	Name	Bit width	Defaults	description
2	IC WAVE	24	0x000000	C-PHASE CURRENT WAVEFORM
				REGISTER
3	IB_WAVE	24	0x000000	Phase b current waveform register
4	IA_WAVE	24	0x000000	Phase a current waveform register
5	IN_WAVE	24	0x000000	Neutral current waveform register
8	VA_WAVE	24	0x000000	Phase a voltage waveform register
9	VB_WAVE	24	0x000000	Phase b voltage waveform register

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А	VC_WAVE	24	0x000000	C-phase voltage waveform register

The waveform is divided into full wave and fundamental wave. Through hpf, the AC measurement mode is used to output the full wave waveform. The fundamental wave lpf is the fundamental wave measurement mode and the fundamental wave waveform is output.

The waveform output selection is fixed, and it is set by the user mode register mode1[23].

0x96	MODE1	Working mode register		
No.	name	default value	description	
			Current wave waveform register output	
	411.0	selection, default 0 selects the waveform of		
[23]	WAVE_REG_SEL	I DU	the normal current channel, and 1 selects the	
			waveform output of the leakage channel	



#### 3.2 Principle of active power calculation



The three-phase current and voltage waveforms are respectively subjected to digital multiplication, and then through low-pass filter, gain and deviation calibration, anticreeping judgment and averaging processing in order to obtain the split-phase power signal, which is added to obtain the total active power.

#### 3.2.1 Active power output

The corresponding 3-phase current is multiplied by the 3-phase voltage to obtain the 3-phase power signal, which is added to obtain the total power.

address	Name	Bit width	Defaults	description
22	WATT A	24	0.2000000	A-phase active power register (full wave
	w/111_/1	27	0x000000	and fundamental wave optional)
23	W/A/T*T B	24	0000000	B-phase active power register (full wave
23	WATI_D	24	0x000000	and fundamental wave optional)

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24	4 WATT_C	24 (	0×000000	C-phase active power register (full wave
24			02000000	and fundamental wave optional)
25	W/A/T*T	24	0.000000	Combined active power register (full
23	WALL 24	27	0x000000	wave and fundamental wave optional)

<u>htan IIA</u> //

Active power calculation formula: WATT =  $\frac{994*I_N(A)*V(V)}{Vref^2} = \frac{994*P0}{Vref^2}$ 

among them, $I_N(A)$ , V(V)Is the effective value input by the channel pin, P0 is the actual power of the applied load, vref is the built-in reference voltage, the typical value is 1.2V. The value 994 is the coefficient (determined by the actual test, the batch is consistent).

It can be set by the add\_sel register, and the power sum is absolute value addition or algebraic sum addition.

0x98	MODE3	Working mode register		
No.	name	default value	description	
[8]	add_sel	1 <b>'</b> b0	watt and var conjoint sum addition method: 0-absolute value addition, $ a + b + c $ ; 1-algebraic sum	
			addition, a+b+c	

#### 3.2.2 Active power calibration

Contains three 16-bit active power offset correction registers WATTOS\_AABBC and three 16-bit active power gain correction registers WATTGN\_AABBC, the default value is 0x0000.

These registers can be used for digital calibration or error pre-calibration before leaving the factory.

Wattos is used to eliminate the DC deviation in the active power calculation, and wattgn is used to eliminate the gain deviation in the active power calculation. The deviation here may be caused by the crosstalk between the two channels generated on the PCB board and the integrated circuit itself in the power calculation. , It may also be the gain deviation of the adc channel itself.

Deviation correction can make the value in the active power register close to 0 under no load.

address	Name	Bit width	Defaults	description
D.C.	WATTON A	16	00000	Corresponding channel active power gain
DU	wAIIGN_A	10	0x0000	adjustment register, complement
<b>B</b> 7	WATTON B	16	00000	Corresponding channel active power gain
D7	wATIGN_D	10	0x0000	adjustment register, complement
DO	WATTON	16	0-0000	Corresponding channel active power gain
Do	WATIGN_C	10	0x0000	adjustment register, complement

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62	WATTOS A	16	00000	Corresponding channel active power bias
	WAT105_A	10	0x0000	adjustment register, complement
C <sup>2</sup>	WATTOS B	16	0x0000	Corresponding channel active power bias
0.5	WA1105_D	10		adjustment register, complement
C 4	WATTOS	16	0-0000	Corresponding channel active power bias
C4	WATTOS_C	16	0x0000	adjustment register, complement

Correction result of active power:

#### WATT=WATTO\*(1+WATTGN/2^16) + WATTOS/2

Where watt is the active power after the nth phase is corrected, and watt0 is the active power before the nth phase is corrected.

#### 3.2.3 Active power anti-creeping

It has a patented power anti-submarine function to ensure that the power output is 0 when there is no current input.

The active anti-creep threshold register (WA\_CREEP) is a 12-bit unsigned number, and the default is 0x04C. This value is internally expanded by 1 and compared with the absolute value of the input active power signal. When the absolute value of the input active power signal is less than this value, the output The active power is set to zero. This can make the value output to the active power register 0 under no-load conditions, even if there is a small noise signal.

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address	Name	Bit width	Defaults	description
				[23:12] is the reactive anti-creeping
00	VAR_CREEP/	24	0x04C04C	power threshold register [11:0] is the
00	WA_CREEP			active anti-creeping power threshold
				register

Corresponding to CREEP value =  $\frac{Corresponding \ power \ register \ value}{2}$ 

You can set wa\_creep according to the watt value of the power register, and their corresponding relationship. The anti-submarine value generally takes 20 parts per million of the power full scale.

When the channel is in the anti-submarine state, the power of the channel below the threshold does not participate in the energy accumulation.

The total active anti-creep threshold register (WA\_CREEP2) is a 12bit unsigned number and the default is 00H. This value is internally expanded by 1 and compared with the absolute value of the input active power signal. When the absolute value of the input active power signal is less than this value, The output active power is set to zero. This is used to prevent creeping of the power sum.

address	Name	Bit width	Defaults	description
				[23:12] IS THE TOTAL REACTIVE
20	VAR_CREEP2/	24	0x000000	ANTI-CREEPING POWER
09	WA_CREEP2			THRESHOLD REGISTER
				VAR_CREEP2; [11:0] THE TOTAL

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-	ACTIVE ANTI-CREEPING	
	THRESHOLD REGISTER	
	WA_CREEP 2	

# 3.2.4 Active power small signal compensation

For the calculation of active power, in order to reduce the noise error in the small signal section, the small signal compensation register can be passed to the small signal compensation register to adjust the nonlinear error of the small signal section.

address	Name	Bit width	Defaults	description
82	WA LOS A	24	0x000	[23:12] Corresponding to active power small signal compensation register
01			011000	complement.
				[23:12] Corresponding to active power
83	WA_LOS_B	24	0x000	small signal compensation register,
				complement.
				[23:12] Corresponding to active power
84	WA_LOS_C	24	0x000	small signal compensation register,
				complement.

#### 3.2.5 Active power selection

Active power calculation method, you can select fundamental active power or fullwave active power through watt\_sel, the default is full-wave active power, you can select 7 channels separately:

0x98	MODE3		Working mode register
No.	name	default value	description

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[17]	watt_sel	1'b0	Watt waveform selection: 0-full wave, 1-fundamental
			wave

3.3 Functional energy measurement principle



Provides three-phase energy pulse accumulation. The principle is that the active power of each phase is integrated for a period of time to obtain the functional energy during this period, and the energy is further converted into the corresponding frequency check pulse cf. The more electricity is used, the cf frequency is faster. The cf frequency is slow when the power is low. The accumulation of functional quantities includes positive power accumulation, negative power accumulation, algebra and accumulation.

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#### 3.3.1 Functional output

Counting cf pulses can obtain energy (power consumption), which is stored in the nth phase energy accumulation register cf(n)\_cnt and total energy register cf\_cnt, as shown in the following figure.

address	Name	Bit width	Defaults	description
2F	CF_A_CNT	24	0x000000	Phase a active pulse count, unsigned
30	CF_B_CNT	24	0x000000	B-phase active pulse count, unsigned
31	CE C CNT	24	0000000	C-PHASE ACTIVE PULSE COUNT,
51	CF_C_CNT	24	0x000000	UNSIGNED
32	CF_CNT	24	0x000000	Conjunction active pulse count, no sign
22	CFP_A_CNT	24	0x000000	Phase a positive active pulse count, no
33				sign
24	CFP_B_CNT	24	0x000000	B-phase positive active pulse count,
34				unsigned
25			0x000000	C-PHASE POSITIVE ACTIVE PULSE
35	CFP_C_CN1	24		COUNT, UNSIGNED
26	CFP_CNT	24	0x000000	Conjunction positive active pulse count,
36				no sign

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|--|

37	CFN_A_CNT	24	0x000000	Phase a negative active pulse count, unsigned
38	CFN_B_CNT	24	0x000000	B-phase negative active pulse count, unsigned
39	CFN_C_CNT	24	0x000000	C-PHASE NEGATIVE ACTIVE PULSE COUNT, UNSIGNED
3A	CFN_CNT	24	0x000000	Conjunction negative active pulse count, unsigned

#### 3.3.2 Function output selection

0x98	MODE3		Working mode register
No.	name	default value	description
[9]	cf_enable	1'b0	0-cf disable, default; 1-cf enable
[13:10]	CF_SEL	4 <b>'</b> b0000	Channel cf_watt, cf_var output selection, The default is 0000, turn off cf_watt, cf_var; 0001, the power CF of watt_aavar_a; 0010, the power CF of watt_bbvar_b; 0011, power CF of watt_cevar_c; 0100, power CF of watttvar; 0101, watt_p_aavar1 power CF; 0110, watt_p_bbvar2 power CF; 0111, power CF of watt_p_cevar3; 1000, power CF of watt_ppvar4; 1001, watt_n_aava_a power CF; 1010, watt_n_va_b power CF; 1011,watt_n_ceva_c power CF; 1100,watt_nnva power CF 1101, (SAME AS 0100); 1110, APPARENT POWER CF; 1111, CLOSE CF;

8			<b>BIG552</b> Three phase power monitoring and analysis
			Watt and var energy addition methods: 0-absolute value
[15]	cf_add_sel	1'b0	addition; 1-algebraic sum addition (separation and
			combination)

First set mode3[9]=1 to select cf pin to output electric energy pulse, and then set cf\_sel to choose how to output electric energy pulse.

CF\_add\_sel is used to set how the total energy is added, the algebraic sum or absolute value of each phase is added.

The counting results of CF pulses are stored in the CF\*\_\*\_CNT registers. The number of pulses can also be directly counted from the CF pin through the IIO interrupt. When the cycle of CF is less than 180ms, it is a pulse with a 50% duty cycle, which is greater than When equal to 180ms, the fixed pulse width is 90ms.

The power conversion formula corresponding to 1 cf:

Ecf= 58.6058574\* T<sub>0</sub> \* Vref<sup>2</sup>(KWh)

Where T0 is the sampling interval, the typical value is 2 microseconds, VrefIs the reference voltage, the typical value is 1.2v.

#### 3.3.3 Function output ratio

In the energy accumulation, the speed of energy accumulation can be set through the cf\_div register, each file is 2 times the relationship, a total of 12 files.

These registers can be used for digital calibration or error pre-calibration before leaving the factory. Shanghai Belling Co., Ltd. 35/119 V1.1 810 Yishan Road, Shanghai www.belling.com.cn

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address	Name	Bit width	Defaults	description
CE	CFDIV	12	0x010	Active cf scaling register [11:0]

# 3.4 The calculation principle of the effective

#### value of current and voltage

The calculation principle of the effective value of the channel, as shown below



The original waveform of each channel passes through the square circuit (X^2), the effective value low-pass filter (LPF\_RMS), and the root circuit (ROOT) to obtain the instantaneous value RMS\_t of the effective value, and then average the average value of each channel The values I[N]RMS and V\_RMS.

#### 3.4.1 Effective value output

The effective value calculation result is output and sum to 7 registers.

address	Name	Bit width	Defaults	description
---------	------	-----------	----------	-------------
E	SHANGHAI BELLI	NG I	BG	52 Three phase power monitoring and analysis
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D	IC DMS	24	0.000000	C-phase current effective value register,
D	IC_RMS	24	0x000000	unsigned
Е	IB_RMS	24	0x000000	Phase b current RMS register, unsigned
Б	LA DMS	24	0000000	Phase a current effective value register,
Г	IA_KMS	24	0x000000	unsigned
10	IN_RMS	24	0x000000	Zero wire current RMS register, unsigned
13	VA DMS	24	0000000	Phase a voltage effective value register,
1.5	VA_RW3	24	0x000000	unsigned
14	VR PMS	24	0000000	Phase b voltage effective value register,
14	VD_KW3	24	0x000000	unsigned
15	VC PMS	24	0000000	C-phase voltage effective value register,
13		24	0x000000	unsigned

When the channel is in the anti-submarine state, the effective value of the channel is not measured.

Current RMS conversion formula:  $i_rms = \frac{315021*I(A)}{Vref}$ Voltage RMS conversion formula:  $v_rms = \frac{20194*V(V)}{Vref}$ 

Vref is the reference voltage, and the typical value is 1.2V.

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## 3.4.2 Setting of effective value input signal

Set MODE2[21:0].WAVE\_RMS\_SEL to select the effective value to calculate the

input waveform. Each channel can be selected by two bits, 00-high pass, 01-select

fundamental wave, 11-select sinc for direct output.

0x97	MODE2		Working mode register
No.	name	default value	description
			RMS waveform selection, 00-high pass, 01-
			select fundamental wave, 11-select sinc
			output
			[3,2]: C PHASE CURRENT
[21.0]	WAYE DMC CEL		[5,4]: B-PHASE CURRENT
[21:0]	WAVE_KW5_SEL	11{2 000}	[7,6]: Phase a current
			[9:8]: Neutral line current
			[15,14]: PHASE A VOLTAGE
			[17,16]: PHASE B VOLTAGE
			[19,18]:C-PHASE VOLTAGE

#### 3.4.3 Valid value refresh rate setting

Set MODE2[22].RMS\_UPDATE\_SEL, you can choose the effective value average

refresh time is 525ms or 1050ms, the default is 500ms.

0x97	MODE2	Working mode register
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	8,		BIG.	<b>552</b> Three phase power monitoring and analysis
Ĩ	No.	name	default value	description
				Slow effective value register update speed
	[22]	RMS_UPDATE_SEL	1'b0	selection, 1 is 1050ms, 0 is 525ms, and the
				default selection is 525ms;

#### 3.4.4 Current and voltage RMS calibration

Contains 7 24-bit effective value offset correction registers RMSOS[N] and 7 16-bit effective value gain correction registers RMSGN[N], the default value is 0x0000.

They use the data in the form of 2's complement to calibrate the deviation in the effective value calculation. This deviation may come from input noise, because there is a step of square operation in the effective value calculation, which may introduce a DC offset caused by noise. Gain and offset correction can make the value in the effective value register close to 0 under no load.

address	Name	Bit width	Defaults	description
	IC BMSCN	17	0-0000	Corresponding channel effective value gain
0D	IC_RM5GN	N 16 0x00	0x0000	adjustment register
Œ	ID DMCCN	P. PMSCN 16 0-6		Corresponding channel effective value gain
6E	ID_RM3GN	10	0x0000	adjustment register
		17	0,0000	Corresponding channel effective value gain
01	IA_KIVISGIN	10	0x0000	adjustment register

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		4.6	0.0000	Corresponding channel effective value gain
/0	IN_KMSGN	16	0x0000	adjustment register
72	WA DMSCN	16	00000	Corresponding channel effective value gain
75	VA_KWSGN	10	0x0000	adjustment register
74	VR PMSCN	16	00000	Corresponding channel effective value gain
74	VD_RIVISGIN	10	0x0000	adjustment register
75	VC PMSCN	16	00000	Corresponding channel effective value gain
/5	VC_RIVISGIN	10	0x0000	adjustment register
70	IC PMSOS	24	0000000	Corresponding channel effective value
/0	IC_KW505	24	0x000000	offset correction register
70	IR PMSOS	24	0000000	Corresponding channel effective value
79	ID_KW303	24	0x000000	offset correction register
74	LA PMSOS	24	0000000	Corresponding channel effective value
/11	IA_KW303	24	0x000000	offset correction register
712	IN PMSOS	24	0000000	Corresponding channel effective value
7.D	IIN_KM3O3	24	0x000000	offset correction register
75	VA PMSOS	24	0000000	Corresponding channel effective value
712	VA_RW505	24	0x000000	offset correction register
75	WR PMSOS	24	0000000	Corresponding channel effective value
/ Г'	V D_KIVISUS	2 <del>4</del>	0x000000	offset correction register

Ĺ		BIG	552 Three phase power monitoring and analysis

				Corresponding channel effective value
80	VC_RMSOS	24	0x000000	
				offset correction register

Calibration formula:

 $RMS[N] = \sqrt{RMS[N]_0^2 + RMSOS[N] \times 256}$ 

Here rms[n]0 is the effective value of the nth channel before correction, and rms[n] is the effective value of the nth channel after correction.

#### 3.4.5 Effective value of anti-creeping

It has a patented effective value anti-submarine function to ensure that the effective value output is 0 when there is no current input.

The effective value anti-creep threshold register (RMS\_CREEP) is a 12bit unsigned number, and the default is 0x200. This value is internally expanded by 1 and compared with the absolute value of the input effective value signal. When the input effective value signal is less than this value, the output is valid The value is set to zero. This can make the value output to the effective value register 0 under no load, even if there is a small noise signal.

address	Name	Bit width	Defaults	description
	REVD CREED/			[23:12] is the reverse indication
8A	REVE_CREEF	24	0x04C200	threshold register REVP_CREEP
	NVIS_CREEP			(internal times 2^5, the value is equal to

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-		0.2% Ib, the maximum FFF is equal to
		8% Ib); [11:0] is the effective value small
		signal threshold register RMS_CREEP,
		including zero Line (after internal times
		$2^2$ , the value is equal to 540, and the
		maximum FFF is equal to 16380);

# 3.5 Principle of overcurrent detection

The principle of fast effective value calculation is shown in the figure below.



7 channels have fast effective value registers, which can detect half cycle or cycle effective value. This function can be used for overcurrent detection.

The input waveform is obtained by taking the absolute value and then integrating within the specified time to obtain a fast effective value. This value can be compared with a preset threshold, and a flag can be given if it exceeds.

# 3.5.1 Fast effective value output

The 7-channel fast effective value output register is shown in the figure below

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L		Ű	s	H/	N	HI/		BEI	NG		1	i	H	' H	Ζ.,	Throo nh			* 11101	itorii		lana	luoio
:							10.0	_			 A	Ċ		<u> </u>		III GG IJII	186 J	UTH		11011	<b>IY AIII</b>		1515

address	Name	Bit width	Defaults	description
18	IC FAST BMS	24	0×000000	C-phase current fast effective value
10	IC_17151_1005	27	0x000000	register, unsigned
19	IB FAST RMS	24	0x000000	B-phase current fast effective value
17		27	0x000000	register, unsigned
1.4	IA FAST RMS	24	0x000000	A phase current fast effective value
171		27		register, unsigned
18	IN FAST RMS	LEAST DMS 24 0.000	0~000000	Zero wire current fast effective value
	11 <b>1</b> _17101_11010	27	0x000000	register, unsigned
1F	VA FAST RMS	24	0~000000	A phase voltage fast effective value
	V/1_1/101_1000	27	0x000000	register, unsigned
1F	VB FAST RMS	24	0~000000	B-phase voltage fast effective value
11	VD_1731_RW5	27	0x000000	register, unsigned
20	VC FAST RMS	24	0.2000000	C-phase voltage fast effective value
20	v C_1/2101_R1VI0	27	02000000	register, unsigned

# 3.5.2 Fast effective value input selection

See the channel waveform block diagram for the source of the waveform. You can

choose	to	pass	hpf	and	not pass	hpf.
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0x96	MODE1	Working mode register			
No.	name	default value	description		

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			Leakage selection through high pass, the				
[22]	L_F_SEL	1'b0	default is 0 to select no high pass, and 1 to				
			select high pass				

# 3.5.3 Fast effective value accumulation time and threshold

To calculate the fast effective value, first take the absolute value, and then integrate according to the set cumulative time. Generally, it is an integer multiple of half cycle and cycle time.

address	Name	Bit width	Defaults	description
8B FAST_RMS_CTRL				[23:21] Channel fast effective value
				register refresh time, half cycle and n
	24	0x20FFFF	cycle can be selected, the default is	
				half cycle; [20:0] channel fast
				effective value threshold register

Choose the accumulated time by FAST\_RMS\_CTRL[23:21], which is divided into six types: 000-10ms, 001-20ms, 010-40ms, 011-80ms, 100-160ms, 101-320ms. The default selection of half-cycle cumulative response time is 20ms, cumulative The longer the time, the smaller the beating.

FAST\_RMS\_CTRL[20:0] is used to set the fast effective value exceeding threshold, once exceeded, the output flag flag[N] is 1.



# $FAST\_RMS\_CTRL[20:0] = \frac{I[N]\_FAST\_RMS}{8}$

#### 3.5.4 Grid frequency selection

In addition, it is necessary to distinguish between 50Hz and 60Hz half cycle time

(AC\_FREQ\_SEL).

0x97	MODE2		Working mode register
No.	name	default value	description
[23]	AC EDEO SEL	11-0	AC frequency selection, 1 is 60Hz, 0 is
	AC_FREQ_SEL	I DU	50Hz, default selection is 50Hz

# 3.6 Reactive power calculation

The principle of reactive power calculation is shown in the figure below



After the current and voltage waveforms of each phase pass through the Hilbert filter, digital multiplication is performed, and then the reactive power signal can be obtained after the low-pass filter, gain and deviation calibration, anti-creeping judgment and averaging processing in order. Obtained after integration Reactive energy pulse accumulation.

#### 3.6.1 Reactive phase compensation

At the adc output position, a method for digital calibration of small phase errors is provided. It can introduce a small time delay or lead into the signal processing circuit to compensate for small phase errors. Since this compensation must be timely, this This method is only suitable for small phase errors of <0.6 (range. Using time-shift



technology to correct large phase errors will introduce significant phase errors in higher harmonics.

For the current and voltage signals of reactive power calculation, use a 4-bit register

to adjust:

address	Name	Bit width	Defaults	description
				Reactive phase correction (fine tuning):
				[3:0] bits fine-tune the phase of the $\Lambda$ -
				phase current channel in the reactive
				power calculation; [7:4] bits fine-tune the
				phase of the B-phase current channel in
				the reactive power calculation; [11:8] Bit
			0x0000	to fine-tune the phase of the C-phase
				current channel in the calculation of
0/1	VAR_PHCAL_I	15		reactive power; [11], [7], [3] are the
				enable bits, the minimum adjustment
				delay time is 560ns, corresponding to
				0.01 degrees and 1LSB, and the
				maximum adjustable is $\pm 0.08$ degrees ,
				The default is 0.04 degrees. Reactive
				power phase correction (coarse
				adjustment): [12] is the

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	SHANGHAL BELLIN			VAR PHCAL2 IA register, when it is 1,
				the IA channel reactive power delay is
				64us; [13] is the VAR PHCAL2 IB
				register when it is 1, the IB channel
				regative power delay is 1 64ya [14] is the
				reactive power delay is 1. 64us; [14] is the
				VAR_PHCAL2_IC register, when it is 1,
				the IC channel reactive power delay is
				64us;
				Reactive power phase correction (fine
				tuning): [3:0] bits fine-tune the phase of
				the A-phase voltage channel in the
				reactive power calculation; [7:4] bits fine-
				tune the phase of the B-phase voltage
				channel in the reactive power calculation;
6B	VAR_PHCAL_V	15	0x0000	[11:8] Bit to fine-tune the phase of the
				C-phase voltage channel in the reactive
				power calculation; [11], [7], and [3] are
				the enable bits, the minimum adjustment
				delay time is 560ns, corresponding to
				0.01 degrees and 1LSB, and the
				maximum adjustable is $\pm 0.08$ degrees ,

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The default is 0.04 degrees. Reactive
power phase correction (coarse
adjustment): [12] is the
VAR_PHCAL2_VA register, when it is
1, the VA channel reactive power delay is
64us; [13] is the VAR_PHCAL2_VB
register, when it is 1, the VB channel
reactive power delay is 1. 64us; [14] is the
VAR_PHCAL2_VC register, when it is
1, the VC channel reactive power delay is
64us;

# 3.6.2 Reactive power output

Output 3 phase and combined phase reactive power, fundamental wave and full wave

reactive power are given at the same time.

address	Name	Bit width	Defaults	description
	VAD A	24	0x000000	Phase a (full wave) reactive power
5A	VAK_A			register
5D	VAD D	_B 24 0x00000	0-000000	Phase b (full wave) reactive power
5B	VAK_B		0x000000	register

e,			BIG-5	52 Three phase power monitoring and analysis
50	VAR C	24	0×000000	C-phase (full wave) reactive power
50	VIIIC_C	24	0x000000	register
5D	VAR	24	0000000	Combined phase (full wave) reactive
50	VIII	24	0x000000	power register
24	Ενάρα	24	0000000	Phase a (fundamental wave) reactive
211		24	0x000000	power register
28	EVAR B	24	0×000000	Phase b (fundamental wave) reactive
20		24	0x000000	power register
20	EVAR C	24	0×000000	C-phase (fundamental wave) reactive
20		24	0x000000	power register
2D	FVAR	24	0×000000	Combined phase (fundamental) reactive
		24	0x000000	power register

#### 3.6.3 Reactive power calibration

Contains three 16-bit reactive power offset correction registers VAROS and three 16-bit reactive gain correction registers VARGN, the default value is 0x0000.

Contains three 16-bit fundamental reactive power offset correction registers

FVAROS and three 16-bit fundamental reactive gain correction registers FVARGN, the

default value is 0x0000.

These registers can be used for digital calibration or error pre-calibration before

leaving the factory.

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They use data in the form of 2's complement to calibrate the deviation in the reactive power calculation. This deviation may come from input noise or phase difference, which may introduce DC offset and gain errors caused by noise. Gain and deviation correction can be Correct the reactive power measurement curve.

address	Name	Bit width	Defaults	description
DO	MADONIA	16	0.0000	Corresponding channel reactive power gain
D9	VARGN_A	10	0x0000	adjustment register, complement
₽A	VADON B	16	00000	Corresponding channel reactive power gain
DΛ	VARGN_D	10	0x0000	adjustment register, complement
DD	WARCN C	16	0x0000	Corresponding channel reactive power gain
DD	VARGN_C	10		adjustment register, complement
C5	WAROS A	16	00000	Corresponding channel reactive power bias
0.5	VARO5_A	10	0x0000	adjustment register, complement
66	VAPOS B	16	00000	Corresponding channel reactive power bias
0	VARO5_D	10	0x0000	adjustment register, complement
<u> </u>	WAROS C	4.4	00000	Corresponding channel reactive power bias
	VARUS_C	10	0x0000	adjustment register, complement

address	Name	Bit width	Defaults	description
DC	FVARGN_A	16	0x0000	Corresponding channel reactive power
DC				gain adjustment register, complement

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e			BIG.	<b>552</b> Three phase power monitoring and analysis
RD	EVADON B	16	00000	Corresponding channel reactive power
DD		10	0x0000	gain adjustment register, complement
BE	EVARCN C	16	0x0000	Corresponding channel reactive power
DL		10	0x0000	gain adjustment register, complement
68	EVAROS A	16	0x0000	Corresponding channel reactive power bias
0	1.110021	10		adjustment register, complement
C0	EVAROS B	16	0x0000	Corresponding channel reactive power bias
09	TV/IRO5_D	10	0x0000	adjustment register, complement
CA	EVAROS C	16	0x0000	Corresponding channel reactive power bias
CA	FVAKOS_C		0x0000	adjustment register, complement

Reactive power correction result:

VAR=VAR0\*(1+VARGN/2^16) + VAROS\*2

Where var is the active power after correction, and var0 is the reactive power before

correction.

Correction result of fundamental reactive power:

FVAR=FVAR0\*(1+FVARGN/2^16) + FVAROS\*2

Where fvar is the active power after correction, and fvar0 is the reactive power

before correction.

#### 3.6.4 Anti-creeping of reactive power

It has a patented power anti-submarine function to ensure that the power output is 0 when there is no current input.

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The reactive power anti-creep threshold register (VAR\_CREEP) is a 12-bit unsigned number, and the default is 0x04C. This value is internally expanded by 1 and compared with the absolute value of the input reactive power signal. When the absolute value of the input reactive power signal is less than this value The output reactive power is set to zero. This can make the value of the output to the reactive power register 0 in the case of reactive power measurement, even if there is a small noise signal.

address	Name	Bit width	Defaults	description
88	VAR_CREEP/ WA_CREEP	24	0x04C04C	[23:12] IS THE REACTIVE ANTI- CREEPING POWER THRESHOLD REGISTER VAR_CREEP (INTERNAL TIMES 2^0); [11:0] IS THE ACTIVE ANTI-CREEPING POWER THRESHOLD REGISTER
				WA_CREEP (INTERNAL TIMES 2^0)

Var\_creep can be set according to the var value of the power register, and their corresponding relationship. The anti-submarine value generally takes 20 parts per million to 200 parts per million of the full scale of reactive power.

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When the channel is in the anti-submarine state, the power of the channel below

the threshold does not participate in the energy accumulation.

#### 3.6.5 Reactive power small signal compensation

For the calculation of reactive power, in order to reduce the noise error in the small signal section, the small signal compensation register can be passed to the small signal compensation register to adjust the nonlinear error of the small signal section.

addr ess	Name	Bit width	Defa ults	description
02	VAR_LO	24	0x00	[11:0] Corresponding to the small reactive power
82	S_A	24	0	compensation register, complement.
0.2	VAR_LO	24	0x00	[11:0] Corresponding to the small reactive power
83	S_B	24	0	compensation register, complement.
	VAR_LO		0x00	[11:0] Corresponding to the small reactive power
84	S_C	24	0	compensation register, complement.
	FVAR_L		0x00	[11:0] Corresponding to reactive power (fundamental
85	OS_A	24	0	wave) small signal compensation register, complement.
0.6	FVAR_L	24	0x00	[11:0] Corresponding to reactive power (fundamental
86	OS_B	24	0	wave) small signal compensation register, complement.
07	FVAR_L	24	0x00	[11:0] Corresponding to reactive power (fundamental
87	OS_C	24	0	wave) small signal compensation register, complement.

#### 3.6.6 Reactive energy output

Reactive energy can be obtained by counting reactive cf pulses, which is stored in

the	reactive	energy	accumu	lation	register	cfq	cnt,	as shown	in t	he figure	below.
		8/			8		,		0		

address	Name	Bit width	Defaults	description
3B	CFQ_A_CNT	24	0x000000	Phase a reactive pulse count, unsigned
3C	CFQ_B_CNT	24	0x000000	Phase b reactive pulse count, unsigned

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2D	CEO C CNT	24	0000000	C-PHASE REACTIVE PULSE
ענ	CFQ_C_CN1	24	0x000000	COUNT, UNSIGNED
<b>3</b> E	CEO CNT	24	0x000000	Combination reactive pulse count, no
512		27	0x000000	sign
<b>3</b> F	CEO1 CNT	24	0000000	Reactive pulse count in the first quadrant,
51		27	0x000000	unsigned
40	CEO2 CNT	24	0x000000	Second quadrant reactive pulse count, no
10			0x000000	sign
41	CEO3 CNT	24	0x000000	Third quadrant reactive pulse count, no
11			0x000000	sign
42	CFO4 CNT	24	0.000000	Fourth quadrant reactive pulse count,
42	CFQ4_CNT	24	02000000	unsigned

Reactive energy calculation method, you can select fundamental reactive power or full-wave reactive power through var\_sel, the default is fundamental reactive power:

0x98	MODE3	Working mode register			
No.	name	default value description			
[16]	var_sel	1'b0	Var energy selection: 0-fundamental wave; 1-full wave		

# 3.7 Apparent and power factor calculation

See the figure below for the apparent calculation principle



There are two ways of apparent calculation:

One is the digital multiplication of the effective values of current and voltage, and then gain and deviation calibration in order to obtain the reactive power signal. After integration, the reactive energy pulse accumulation is obtained. The active power is divided by the apparent power to obtain the power factor.

The second is obtained by adding the square of active power to the square of reactive power, and then opening the root sign.

The reactive power and power factor calculated in the second way have better accuracy when measuring small signals.

#### 3.7.1 Apparent power and energy output

The output only has split-phase and combined-phase apparent power and energy.

address	Name	Bit width	Defaults	description
26	X7A A	24	0.000000	A PHASE APPARENT POWER
20	VA_A	24	0x000000	REGISTER
27	VA D	24	0.000000	B-PHASE APPARENT POWER
27	VA_B	24	0x000000	REGISTER
20	VA C	24	0-000000	C PHASE APPARENT POWER
28	VA_C	24	0x000000	REGISTER
29	VA	24	0x000000	Conjunct apparent power register
42	CFS_A_CNT	24	0x000000	A PHASE APPARENT PULSE
43				COUNT, UNSIGNED
4.4		24	0x000000	B-PHASE APPARENT PULSE
44	CF5_D_CN1			COUNT, UNSIGNED
45	CES C CNIT	24	0-000000	C-PHASE APPARENT PULSE
45	CF5_C_CN1	24	0x000000	COUNT, UNSIGNED
16	CFS_CNT	24	0x000000	Conjunction apparent pulse count, no
40				sign

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#### 3.7.2 Apparent power calibration

Contains three 16-bit apparent offset correction registers VAOS and three 16-bit apparent gain correction registers VAGN, the default value is 0x0000.

These registers can be used for digital calibration or error pre-calibration before leaving the factory.

They use 2's complement data to calibrate the deviation in the apparent calculation.

This deviation may come from the previous stage, which may introduce offset and gain errors. Gain and deviation correction can correct the apparent measurement curve.

address	Name	Bit width	Defaults	description
DE	MACNIA	16	00000	Corresponding channel apparent power gain
DΓ	VAGN_A	10	0x0000	adjustment register, complement
CO	VACN B	16	0x0000	Corresponding channel apparent power gain
CO	VIION_D	10	0x0000	adjustment register, complement
C1	VAGN_C	16	0x0000	Corresponding channel apparent power gain
CI				adjustment register, complement
CB	VAOS_A	16	0x0000	Corresponding channel apparent power bias
CD				adjustment register, complement
AND	WAOS B	16	00000	Corresponding channel apparent power bias
CC	VAOS_B	10	0x0000	adjustment register, complement
CD	WAOS C	16	0-0000	Corresponding channel apparent power bias
	VAOS_C		0x0000	adjustment register, complement



Correction result of apparent power:

 $VA=VA0*(1+VAGN/2^{16}) + VAOS*2$ 

Where va is the apparent power after correction, and va0 is the apparent power

before correction.

#### 3.7.3 Power factor

			1 1	
address	Name	Bit width	Defaults	description
47	PF_A	24	0x000000	Phase a power factor register
19	DE B	24	0x000000	B-PHASE POWER FACTOR
40	PF_D	24		REGISTER
40	DE C	24	0-000000	C-PHASE POWER FACTOR
49	PF_C	24	0x000000	REGISTER
4A	PF	24	0x000000	Sum power factor register

Output split-phase and combined-phase power factor.

24-bit signed number, complement. Bit[23] is the sign bit,

Power factor 
$$=\frac{PF}{2^{23}}$$

The calculation method of apparent power and power factor is selected by the

va\_sel register.

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No.	name	default value	description				
[7]	ma aal	11,0	va algorithm selection: 0-rmsi^2+rmsv^2; 1-				
[/]	va_ser	1 DO	(watt^2+var^2)^0.5				

# 3.8 Calculation of three-phase current sum

#### 3.8.1 The output of the current sum

The three-phase current sum can be selected from algebraic sum calculation,

address	Name	Bit width	Defaults	description
F7	LCUM	24	0.000000	Three-phase current instantaneous
57	1_50M	24	0x000000	waveform and
				The effective value of the three-
58	I_SUM_RMS	24	0x000000	phase current instantaneous
				waveform sum, unsigned
				The fast effective value of the three-
59	I_SUM_FAST_RMS	24	0x000000	phase current instantaneous
				waveform sum, unsigned

algebraic sum calculation, or fast effective value calculation, and output to:

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#### 3.8.2 Adjustment of current sum

Contains a 24-bit current and effective value offset correction register isum\_rmsos and a 16-bit current and effective value gain correction register isum+rmsgn, the default value is 0000h.

address	Name	Bit width	Defaults	description
01	ICHM DMCON	16	0x0000	Corresponding channel effective value
91	ISUM_KMSGIN			gain adjustment register
02	ISTIM DWOOD	24	0-000000	Corresponding channel effective value
92	ISUM_RMSOS	24	0x000000	offset correction register

#### 3.8.3 Comparison of current sum

For the comparison of the neutral current, see the following registers:

0x98	MODE3	Working mode register		
No.	name	default value	description	
			When it is 0, compare the effective value of isumlvl and	
[4] isumlvl_sel	1'b0	NI_RMS output neutral current; when it is 1, the		
		effective value of the sum of instantaneous waveforms		
			of isumlvl and the output three-phase current;	

	address N	Name	Bit width	Defaults	description
--	-----------	------	-----------	----------	-------------

	E	SHANGHAI BELL		BGS	<b>52</b> Three phase power monitoring and analysis
_					Current comparison threshold register,
					select NI_RMS to compare with the
					ISUMLVL register, if IN_RMS is less
					than ISUMLVL, the interrupt state
					ISUMLVL_out is 0; if IN_RMS is less
					than ISUMLVL, the interrupt state
	8D	ISUMLVL	24	0xFFFFFF	ISUMLVL_out is 1. Note that IN_RMS
					can be selected as the effective value of
					the algebraic sum of three-phase transient
					currents Or the zero line actually
					measures the effective value. The
					function is the same as PKLVL.
					Mode3[4]

# 3.9 Small signal compensation

For the calculation of active power (fundamental wave and full wave), reactive power (fundamental wave and full wave), and apparent power, in order to reduce the noise error in the small signal section, you can pass to the small signal compensation register to adjust the small signal section Non-linear error.

address	Name	Bit width	Defaults	description
---------	------	-----------	----------	-------------

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				[23:12] Corresponding to a phase active
	WA LOS A/			small signal compensation register,
82	VAR LOS A	24	0x000000	complement. [11:0] Corresponding to a
	V/III_105_/I			phase reactive small signal compensation
				register, complement.
				[23:12] Corresponds to b-phase active
	WALOS R/			small signal compensation register,
83	WAR LOS R	24	0x000000	complement. [11:0] Corresponds to b-
	VAR_LOS_D			phase reactive small signal compensation
				register, complement.
				[23:12] CORRESPONDS TO THE C-
				PHASE ACTIVE SMALL SIGNAL
				COMPENSATION REGISTER,
0.4	WA_LOS_C/	24	0.000000	COMPLEMENT. [11:0]
84	VAR_LOS_C	24	0x000000	CORRESPONDS TO THE C-PHASE
				REACTIVE SMALL SIGNAL
				COMPENSATION REGISTER,
				COMPLEMENT.
				[11:0] Corresponding to the reactive
85	FWALUS_A	24	0x000000	power small signal compensation
	/FVAK_LOS_A			register, complement.

8			BGÐ	<b>52</b> Three phase power monitoring and analysis
	ENVALOS D/			[11:0] Corresponding to the reactive
86	FWALLOS_B/	24	0x000000	power small signal compensation
	FVAR_LOS_B			register, complement.
				[11:0] Corresponding to the reactive
87	FWA_LOS_C/	24	0x000000	power small signal compensation
	FVAR_LOS_C			register, complement.

# 3.10 Temperature measurement

Provide internal temperature measurement.

address	Name	Bit width	Defaults	description
5E	TPS1	10	0x0000	Internal temperature value register

# 3.11 Electrical parameter measurement

#### 3.11.1 Line cycle measurement

With line cycle energy accumulation calculator, including active and reactive power.

address	Name	Bit width	Defaults	description
4B	LINE_	24	0x000000	Line cycle cumulative active energy register
4D	WATTHR	24	0x000000	The cycle cumulative active energy register
10	LINE_	24	0-000000	Line cycle cumulative reactive energy
4C	VARHR	24	0x000000	register



The number of line cycles can be selected through the linecyc register:

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#### 3.11.2 Line frequency measurement

For the grid frequency test, develop a voltage channel test.

The count of the line period recorded in the PERIOD register, if the input signal

deviates from 50Hzz60Hz, the corresponding count value will change.

address Nam	e Bit width	Defaults	description
-------------	-------------	----------	-------------

8			<b>B</b> G.	<b>552</b> Three phase power monitoring and analysis
2E	PERIOD	20	0x000000	Line voltage frequency period register
				(optional channel)

				(optional channel)	
Measure	the frequency of	the sine w	vave signal o	of the voltage channel.	

*Line voltage frequency* 
$$= \frac{10000000}{PERIOD}$$
 Hz

#### 3.11.3 Phase angle calculation

Phase angle measurement principle, see the figure below



The phase difference is obtained by calculating the time difference between the positive zero crossing of the current and the voltage, and the corresponding time value is updated to the register corner(n), and each register is a 16-bit unsigned number.

address	Name	Bit width	Defaults	description
(17)	4E ANGLE_AB 16 0	4.4		Is the phase-to-phase time register of
4£		0x0000	voltage a phase and voltage b phase	
4F	ANGLE_BC	16	0x0000	Is the phase-to-phase time register of
				voltage b-phase and voltage c-phase
50	ANCLE AC	16	0x0000	Is the phase-to-phase time register of
50	ANGLE_AC	10		voltage a phase and voltage c phase

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51	ANGLE_A	16	0x0000	Output a phase voltage and current time register
52	ANGLE_B	16	0x0000	Output B-phase voltage and current time register
53	ANGLE_C	16	0x0000	Output c-phase voltage and current time register

Phase angle conversion formula:  $2*pi*ANGLE[N]*\frac{f_c}{f_0}$ The unit is radians among them,  $f_c$ Is the measurement frequency of the AC signal source, the default is 50Hz,  $f_0$ Is the sampling frequency, the typical value is 1MHz.

#### 3.11.4 Power sign bit

Ξ

For power pulse cf output such as active and reactive power, there is a sign bit register indicating the direction of each cf. This direction indicates the direction of the corresponding accumulated energy (electricity or power supply) from the last cf to the current cf pulse.

address	Name	Bit width	Defaults	description
4D	SIGN	24	0x0000	CF SIGN BIT

0	CF_A_CNT	8	CFN_A_CNT	16	CFQ1_CNT
1	CF_B_CNT	9	CFN_B_CNT	17	CFQ2_CNT
2	CF_C_CNT	10	CFN_C_CNT	18	CFQ3_CNT

#### SIGN[0]~ SIGN[23] CORRESPOND TO THE FOLLOWING CF

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**BIG552** Three phase power monitoring and analysis GHAI BELLING CFN CNT CF\_CNT 11 19 CFQ4 CNT 3 CFS\_A\_CNT 4 CFP\_A\_CNT 12 CFQ\_A\_CNT 20 5 13 CFQ\_B\_CNT 21 CFP\_B\_CNT CFS\_B\_CNT 6 22 CFP\_C\_CNT 14 CFQ\_C\_CNT CFS\_C\_CNT 7 23 CFP CNT 15 CFQ\_CNT CFS\_CNT

#### 3.12 Fault detection

#### 3.12.1 Zero crossing detection

Provides voltage zero-crossing detection. The zero-crossing signal is directly output from the pin ZS. ZS is zero to indicate the positive half cycle of the waveform, and zx is 1 to indicate the negative half cycle of the waveform. The delay from the actual input signal is about 570us.



3.12.2 Peak overrun

The threshold value of the effective value of current and voltage can be set by

programming, which is set by the peak threshold register (i\_pklvl, v\_pklvl).

address	Name	Bit width	Defaults	description
---------	------	-----------	----------	-------------

<b>BL6552</b> Three phase power monitoring and analysis						
				[23:12] Current peak value threshold		
8C	I_FKLVL/	24	0xFFFFFF	register i_pklvl; [11:0] Voltage peak value		
	V_PKLVL			threshold register v_pklvl		

For example, when the fast effective value of the channel ia current is greater than the threshold set by the current peak threshold register (i\_pklvl), the current overload indication pk\_ia is given. If the corresponding pk\_ia enable position in the interrupt mask register (mask1) is logic 1, then The irq logic output becomes active low.

Other current and voltage channels are similar, the output is placed in the status1 register

address	Name	Bit width	Defaults	description
54	STATUS1	24	0x000000	Interrupt status register 1, unsigned

The corresponding positions are as follows:

position	Interrupt flag	Defaults	description
			Indicates that the peak value of the effective
13	PK_VA	0	value of the a-phase voltage channel exceeds
			pkvlvl interrupt, which is 1
			Indicates that the peak value of the effective
14	PK_IA	0	value of the phase a current channel exceeds
			the pkilvl interrupt, which is 1

		BI	<b>5552</b> Three phase power monitoring and analysis
			Indicates that the peak value of the effective
15	PK_VB	0	value of the phase b voltage channel exceeds
			the pkvlvl interrupt, which is 1
			Indicates that the peak value of the effective
16	PK_IB	0	value of the phase b current channel exceeds
			the pkilvl interrupt, which is 1
			Indicates that the peak value of the effective
17	PK_VC	0	value of the c-phase voltage channel exceeds
			pkvlvl interrupt, which is 1
			Indicates that the peak value of the effective
18	PK_IC	0	value of the c-phase current channel exceeds
			the pkilvl interrupt, which is 1
			Indicates that the peak value of the effective
19	PK_NI	0	value of the n-phase current channel exceeds
			the pkilvl interrupt, which is 1

#### 3.12.3 Line voltage drop

It can be indicated by programming. When the effective value of the line voltage is lower than a certain peak value for more than a certain number of half cycles, an indication of the line voltage drop is given.





As shown in the figure above, when the effective value of the voltage is less than the threshold set in the drop voltage threshold register (saglvl) and the drop time exceeds the set time in the drop line cycle register (sagcyc) (the figure shows after the sixth half cycle, sagcyc[11:0]=06h), the line voltage drop event is recorded by setting the sag flag bit in the interrupt status status1 register.

position	Interrupt flag	Defaults	description
0 SAG_A		0	Indicates that a phase line voltage drop
	SAG_A		interrupt is generated, and the drop is 1
1	SAG_B	0	Indicates that the voltage drop of phase b is
			interrupted, and the drop is 1
2 8	SAG_C		Indicates that the voltage drop interruption of
		0	phase c is generated, and the drop is 1

If the corresponding sag enable position in the interrupt mask register (mask1) is

logic 1, the irq logic output becomes active low.

address	Name	Bit width	Defaults	description	
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	SAGCYC/ ZXTOUT	24	0x04FFFF	[23:16] Fall line period register sageyc,	
				default 04h. [15:0] Zero-crossing timeout	
8F				register zxtout, if there is no zero-crossing	
				signal within the time indicated by this	
				register, a zero-crossing timeout interrupt	
				will be generated, default ffffh.	
	SAGLVL/ LINECYC	24	0x100009	[23:12] The drop voltage threshold	
				register SAGLVL, the voltage channel	
				input is continuously lower than the value	
				of this register for more than the time in	
				SAGCYC, and the line voltage drop	
8F				interrupt will be generated. The default is	
01				100H, about 1116 full amplitude voltage	
				input; [11: 0] Line energy accumulation	
				cycle number register LINECYC, default	
				009H, representing 10 cycles. Line cycle is	
				related to external crystal oscillator,	
				recommended crystal oscillator is 8MHz	

The drop voltage threshold register (SAGLVL) can be written or read by the user, and the initial value is FFFH. The drop line period register (SAGCYC) can also be
written or read by the user, and the initial value is FFH. The resolution of this register is 10mss LSB, the maximum delay time of such an interrupt is limited to 2.55s.

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#### 3.12.4 Zero crossing timeout

The zero-crossing detection circuit is also connected to a register zxtout that detects the zero-crossing signal timeout. Whenever the detection voltage channel has a zerocrossing signal, zxtout is set to the initial value. If there is no zero-crossing signal, it will decrement. When the zero signal is output, the value in this register will become 0. At this time, the corresponding bit zxto in the interrupt status register is set to 1. If the corresponding enable bit zxto in the interrupt mask register is also 1, the zero crossing signal Timeout events are also reflected on the interrupt pin irq. Regardless of whether the corresponding enable bit in the interrupt register is set or not, the zxto flag bit in the interrupt status register (mask) is always set to be valid when the zxtout register is reduced to 0 1.

address	Name	Bit width	Defaults	description
8E	SAGCYC/ ZXTOUT	24	0x04FFFF	<ul> <li>[23:16] Fall line period register sagcyc,</li> <li>default 04h. [15:0] Zero-crossing timeout</li> <li>register zxtout, if there is no zero-crossing</li> <li>signal within the time indicated by this</li> </ul>
				register, a zero-crossing timeout interrupt will be generated, default ffffh.



The zero-crossing timeout register ZXTOUT can be written or read by the user, the initial value is FFFFH. The resolution of this register is 70.5uss LSB, so the maximum delay time of an interrupt is limited to 4.369s.

The following figure shows the mechanism of detecting zero-crossing timeout when the line voltage is always a fixed DC signal:



The comparison result is placed in the status1 register, corresponding to the

location:

position	Interrupt flag	Defaults description	
		0	Indicate the generation of a phase zero
5	ZATO_A	0	crossing timeout interrupt, the timeout is 1
			Indicates that the phase b zero-crossing
4	ZXTO_B	0	timeout interrupt is generated, and the
			timeout is 1
5	ZXTO_C	0	Indicate the generation of phase c zero-
		0	crossing timeout interrupt, the timeout is 1



## 3.12.5 Zero crossing indicator

The result is placed in the status1 register, corresponding to the location:

position	Interrupt flag	Defaults	description
		0	Indicate the sign bit of a phase voltage
0		0	waveform
7	ZV 14	0	Indicate the sign bit of phase a current
7		0	waveform
0		0	Indicate the sign bit of the b-phase voltage
δ	8 ZX_VB 0		waveform
			Indicate the sign bit of phase b current
9	ZX_IB	0	waveform
10	TX NC	0	Indicate the sign bit of the c-phase voltage
10	ZX_VC	0	waveform
11		0	Indicate the sign bit of the c-phase current
11	ZX_IC 0		waveform
10	ZV NI	0	Indicates the sign bit of the n-phase current
12	ZX_IN 0		waveform

#### 3.12.6 Power supply indication

Contains an on-chip power monitoring circuit that can continuously detect analog power (avdd). If the power supply voltage is less than  $2.7v \pm 5\%$ , the entire circuit is not



activated (not working), that is to say, when the power supply voltage is less than 2.7v, it is not performed Energy accumulation. This approach can ensure that the device maintains correct operation when the power is powered on. This power monitoring circuit has a hysteresis and filtering mechanism, which can eliminate false triggers caused by noise to a large extent. Generally, the power supply The decoupling part of the power supply should ensure that the ripple on the avdd does not exceed 3.3v (5%.



## 4. Internal register

# 4.1 Electrical parameter register (external read)

address	Name	Bit width	Defaults	description
2	IC WAVE	24	0000000	C-PHASE CURRENT WAVEFORM
2	IC_WAVE	24	0x000000	REGISTER
3	IB_WAVE	24	0x000000	Phase b current waveform register
4	IA_WAVE	24	0x000000	Phase a current waveform register
5	IN_WAVE	24	0x000000	Neutral current waveform register
8	VA_WAVE	24	0x000000	Phase a voltage waveform register
9	VB_WAVE	24	0x000000	Phase b voltage waveform register
А	VC_WAVE	24	0x000000	C-phase voltage waveform register
D	IC BMS	24	0000000	C-phase current effective value register,
D	IC_RW5	24	0x000000	unsigned
Е	IB_RMS	24	0x000000	Phase b current RMS register, unsigned
Б		24	0000000	Phase a current effective value register,
1		24	0x000000	unsigned
10	IN PMS	24	0000000	Zero wire current RMS register,
10		24	0x000000	unsigned
13	VA RMS	24	0~00000	Phase a voltage effective value register,
15	v / 1_INIVIO	24	02000000	unsigned



14	VB_RMS	24	0x000000	Phase b voltage effective value register, unsigned
15	VC_RMS	24	0x000000	C-phase voltage effective value register, unsigned
18	IC_FAST_RMS	24	0x000000	C-phase current fast effective value register, unsigned
19	IB_FAST_RMS	24	0x000000	B-phase current fast effective value register, unsigned
1A	IA_FAST_RMS	24	0x000000	A phase current fast effective value register, unsigned
1B	IN_FAST_RMS	24	0x000000	Zero wire current fast effective value register, unsigned
1E	VA_FAST_RMS	24	0x000000	A phase voltage fast effective value register, unsigned
1F	VB_FAST_RMS	24	0x000000	B-phase voltage fast effective value register, unsigned
20	VC_FAST_RMS	24	0x000000	C-phase voltage fast effective value register, unsigned
22	WATT_A	24	0x000000	A-phase active power register (full wave and fundamental wave optional)

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22	WATT B	24	0000000	B-phase active power register (full wave
23	WATT_D	24	0x000000	and fundamental wave optional)
24	WATT C	24	0000000	C-phase active power register (full wave
24	WATI_C	24	0x000000	and fundamental wave optional)
25	W7 A 'T*T	24	0-000000	Combined active power register (full
23	WATT	24	0x000000	wave and fundamental wave optional)
26	XZA A	24	0-000000	A PHASE APPARENT POWER
20		24	0x000000	REGISTER
27	VA D	24	0.000000	B-PHASE APPARENT POWER
27	VA_D	24	0x000000	REGISTER
20	VA C	24	0000000	C PHASE APPARENT POWER
20	VA_C	24	0x000000	REGISTER
29	VA	24	0x000000	Conjunct apparent power register
24		24	0000000	Phase a (fundamental wave) reactive
		24	0x000000	power register
212	EWAD B	24	0000000	Phase b (fundamental wave) reactive
20		24	0x000000	power register
20	EVAR C	24	0x000000	C-phase (fundamental wave) reactive
	I'VAR_C	24	0x000000	power register
2D	EVAP	24	0000000	Combined phase (fundamental) reactive
		24	0x000000	power register



2E	PERIOD	20	0x000000	Line voltage frequency period register (optional channel)
2F	CF_A_CNT	24	0x000000	Phase a active pulse count, unsigned
30	CF_B_CNT	24	0x000000	B-phase active pulse count, unsigned
31	CF_C_CNT	24	0x000000	C-PHASE ACTIVE PULSE COUNT, UNSIGNED
32	CF_CNT	24	0x000000	Conjunction active pulse count, no sign
33	CFP_A_CNT	24	0x000000	Phase a positive active pulse count, no sign
34	CFP_B_CNT	24	0x000000	B-phase positive active pulse count, unsigned
35	CFP_C_CNT	24	0x000000	C-PHASE POSITIVE ACTIVE PULSE COUNT, UNSIGNED
36	CFP_CNT	24	0x000000	Conjunction positive active pulse count, no sign
37	CFN_A_CNT	24	0x000000	Phase a negative active pulse count, unsigned
38	CFN_B_CNT	24	0x000000	B-phase negative active pulse count, unsigned
39	CFN_C_CNT	24	0x000000	C-PHASE NEGATIVE ACTIVE PULSE COUNT, UNSIGNED

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3A	CFN_CNT	24	0x000000	Conjunction negative active pulse count, unsigned
3В	CFQ_A_CNT	24	0x000000	Phase a reactive pulse count, unsigned
3C	CFQ_B_CNT	24	0x000000	Phase b reactive pulse count, unsigned
2D		24	0.000000	C-PHASE REACTIVE PULSE
30	CFQ_C_CN1	24	0x000000	COUNT, UNSIGNED
215	CEO CNT	24	0-000000	Combination reactive pulse count, no
эE	CFQ_CN1	24	0x000000	sign
215	CEO1 CNT	24	0-000000	Reactive pulse count in the first
ЭГ	CFQI_CNI	24	0x000000	quadrant, unsigned
40	CEO2 CNT	24	0000000	Second quadrant reactive pulse count,
40	CFQ2_CN1	24	0x000000	no sign
41	CEO3 CNT	24	0000000	Third quadrant reactive pulse count, no
41	CFQ5_CF	24	0x000000	sign
42	CEO4 CNT	24	0000000	Fourth quadrant reactive pulse count,
42	CFQ4_CIVI	24	0x000000	unsigned
13	CES A CNIT	24	0000000	A PHASE APPARENT PULSE
43	CF5_A_CN1	24	0x000000	COUNT, UNSIGNED
4.4	CES B CN'T	24	0000000	B-PHASE APPARENT PULSE
44	CL2_D_CN1	2 <del>4</del>	0x000000	COUNT, UNSIGNED

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45	CFS_C_CNT	24	0x000000	C-PHASE APPARENT PULSE COUNT, UNSIGNED
46	CFS CNT	24	0x000000	Conjunction apparent pulse count, no
10		21	0.000000	sign
47	PF_A	24	0x000000	Phase a power factor register
18	DE B	24	0x000000	B-PHASE POWER FACTOR
40		24	0x000000	REGISTER
49	PF C	24	0×000000	C-PHASE POWER FACTOR
47	11_C	24	0x000000	REGISTER
4A	PF	24	0x000000	Sum power factor register
4B			0.000000	Line cycle cumulative active energy
40	LINE_ WATTIN	24	0x000000	register
40	IINE VARHR	24	0×000000	Line cycle cumulative reactive energy
10		27	0x000000	register
4D	SIGN	24	0x0000	CF SIGN BIT
4F	ANGLE AB	16	0x0000	Is the phase-to-phase time register of
712	MINULE_MD	10	0x0000	voltage a phase and voltage b phase
4F	ANGLE BC	16	0x0000	Is the phase-to-phase time register of
		10	020000	voltage b-phase and voltage c-phase
50	ANGLE AC	16	0x0000	Is the phase-to-phase time register of
50		16 0x000		voltage a phase and voltage c phase

# 

51	ANGLE A	16	0x0000	Output a phase voltage and current
	_			time register
50	ANCLE R	16	00000	Output B-phase voltage and current
52	ANGLE_D	10		time register
52		16	0.0000	Output c-phase voltage and current
53	ANGLE_C	16	0x0000	time register
54	STATUS1	24	0x000000	Interrupt status register 1, unsigned
55	STATUS2	24	0x000000	Interrupt status register 2, unsigned
56	STATUS3	24	0x000000	Interrupt status register 3, unsigned
- 7	I_SUM	24	0x000000	Three-phase current instantaneous
57				waveform and
		24	0x000000	The effective value of the three-phase
58	I_SUM_RMS			current instantaneous waveform sum,
				unsigned
				The fast effective value of the three-
59	I_SUM_FAST_RMS	5 24 (	0x000000	phase current instantaneous waveform
				sum, unsigned
5.4	ναρα	24	0000000	Phase a (full wave) reactive power
5/1	VAR_A	24	0x000000	register
512	VAD B		0000000	Phase b (full wave) reactive power
30	VAR_D	24	0x000000	register

B	655	Three phase power monitoring and analysis

50	5C VAR_C 24	24	0000000	C-phase (full wave) reactive power
50		0x000000	register	
5D	VAR	24	0x000000	Combined phase (full wave) reactive
50	VIII	27	0x000000	power register
5E	TPS1	10	0x0000	Internal temperature value register

# 4.2 Calibration register (external write)

address	Name	Bit width	Defaults	description
60	GAIN1	24	0x000000	Channel pga gain adjustment register, see "Front-end gain adjustment" description for details. [11:8]:C-PHASE CURRENT [15:12]:B PHASE CURRENT
				[19:16]:A PHASE CURRENT [23:20]:Neutral line current Channel pga gain adjustment register,
61	GAIN2	20	0x00000	see "Front-end gain adjustment" description for details. [11:8]:A PHASE VOLTAGE [15:12]: PHASE B VOLTAGE [19:16]:C PHASE VOLTAGE

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				The angle difference segment point
62	IRMS_P1	24	0x010000	defines P1, which satisfies
				IRMSmin <p1<p2<irmsmax< td=""></p1<p2<irmsmax<>
				The angle difference segment point
63	IRMS_P2	24	0x200000	defines P2, which satisfies
				IRMSmin <p1<p2<irmsmax< td=""></p1<p2<irmsmax<>
				A phase current channel angle
				difference correction register, when
				IRMSmin <effective input<="" of="" td="" value=""></effective>
				current <p1, [7:0]="" channel<="" current="" is="" td="" the=""></p1,>
				phase used for correction, [7] is the
				enable bit, the minimum adjustment
				delay time is 250ns, corresponding to
64	IA_PHCAL	24	0x000000	0.0045 Degree 1LSB, the maximum
				adjustable is $\pm 0.574$ degrees). When
				P1 <effective input<="" of="" td="" value=""></effective>
				current <p2, [15:8]="" correct<="" is="" td="" to="" used=""></p2,>
				the current channel phase, [15] is the
				enable bit, and the adjustment accuracy
				is the same as above. When P2 <the< td=""></the<>
				effective value of input

E			Gəfə	Three phase power monitoring and analysis
				current <irmsmax, [23:16]="" is="" td="" the<=""></irmsmax,>
				current channel phase used for
				correction, [23] is the enable bit, and
				the adjustment accuracy is the same as
				above.
				B-phase current channel angle
65	IB_PHCAL	24	0x000000	difference correction register (same as
			above)	
				C-phase current channel angle
66	IC_PHCAL	24	0x000000	difference correction register (same as
				above)
				Phase A voltage channel angle
				correction register, when
				IRMSmin <effective input<="" of="" td="" value=""></effective>
				current <p1, [7:0]="" channel<="" is="" td="" the="" voltage=""></p1,>
67	VA PHCAL	24	0x000000	phase used for correction, [7] is the
0,		21		enable bit, the minimum adjustment
				delay time is 250ns, corresponding to
				0.0045 Degree 1LSB, maximum
				adjustable $\pm 0.574$ degrees). When
				P1 <effective input<="" of="" td="" value=""></effective>

6			GJJ	2 Three phase power monitoring and analysis
				current <p2, [15:8]="" correct<="" is="" td="" to="" used=""></p2,>
				the current channel phase, [15] is the
				enable bit, and the adjustment accuracy
				is the same as above. When P2 <the< td=""></the<>
				effective value of the input
				current <irmsmax, [23:16]="" is="" td="" to<="" used=""></irmsmax,>
				correct the phase of the voltage
				channel, [23] is the enable bit, and the
				adjustment accuracy is the same as
				above.
				B-phase voltage channel angle
68	VB_PHCAL	24	0x000000	difference correction register (same as
				above)
				C-phase voltage channel angle
69	VC_PHCAL	24	0x000000	difference correction register (same as
				above)
				Reactive phase correction (fine tuning):
				[3:0] bits fine-tune the phase of the A-
6A	VAR_PHCAL_I	15	0x0000	phase current channel in the reactive
				power calculation; [7:4] bits fine-tune
				the phase of the B-phase current



channel in the reactive power calculation; [11:8] Bit to fine-tune the phase of the C-phase current channel in the calculation of reactive power; [11], [7], [3] are the enable bits, the minimum adjustment delay time is 560ns, corresponding to 0.01 degrees and 1LSB, and the maximum adjustable is  $\pm 0.08$  degrees , The default is 0.04 degrees. Reactive power phase correction (coarse adjustment): [12] is the VAR\_PHCAL2\_IA register, when it is 1, the IA channel reactive power delay is 64us; [13] is the VAR\_PHCAL2\_IB register, when it is 1, the IB channel reactive power delay is 1. 64us; [14] is the VAR\_PHCAL2\_IC register, when it is 1, the IC channel reactive power delay is 64us;

4		/		
 e			GFF	Three phase power monitoring and analysis
				Reactive power phase correction (fine
				tuning): [3:0] bits fine-tune the phase
				of the A-phase voltage channel in the
				reactive power calculation; [7:4] bits
				fine-tune the phase of the B-phase
				voltage channel in the reactive power
				calculation; [11:8] Bit to fine-tune the
				phase of the C-phase voltage channel
				in the reactive power calculation; [11],
				[7], and [3] are the enable bits, the
6B	VAR_PHCAL_V	15	0x0000	minimum adjustment delay time is
				560ns, corresponding to 0.01 degrees
				and 1LSB, and the maximum
				adjustable is $\pm 0.08$ degrees , The
				default is 0.04 degrees. Reactive power
				phase correction (coarse adjustment):
				[12] is the VAR_PHCAL2_VA
				register, when it is 1, the VA channel
				reactive power delay is 64us; [13] is the
				VAR_PHCAL2_VB register, when it is
				1, the VB channel reactive power delay

6			GJJ	2 Three phase power monitoring and analysis
				is 1. 64us; [14] is the
				VAR_PHCAL2_VC register, when it is
				1, the VC channel reactive power delay
				is 64us;
6D	IC PMSCN	16	0::0000	Corresponding channel effective value
0D	IC_RIVISGN	10	0x0000	gain adjustment register
6E	IR PMSCN	16	0::0000	Corresponding channel effective value
0E	ID_KWSGN	10	0x0000	gain adjustment register
6F	LA RMSCN	16	0x0000	Corresponding channel effective value
01	IA_RWISGIN	10	0x0000	gain adjustment register
70	IN RMSCN	16	0x0000	Corresponding channel effective value
70	111_NW3011	10	0x0000	gain adjustment register
73	VA RMSCN	16	0×0000	Corresponding channel effective value
75	VII_RIVISGIN	10	0x0000	gain adjustment register
74	VB PMSCN	16	0::0000	Corresponding channel effective value
74	VD_KW3GIN	10	0x0000	gain adjustment register
75	VC PMSCN	16	0.0000	Corresponding channel effective value
15	VC_NIVIOGIN	10	0x0000	gain adjustment register
78		24	0×000000	Corresponding channel effective value
10	1C_RIVISUS	24	02000000	offset correction register



70	IB BMSOS 24 0-000000	Corresponding channel effective value		
19	ID_RM303	24	0x000000	offset correction register
				Corresponding channel effective value
/A	IA_RMSOS	24	0x000000	offset correction register
				Corresponding channel effective value
/B	IN_RMSOS	24	0x000000	offset correction register
71	NA DWGGG	24	0.000000	Corresponding channel effective value
/E	VA_KMSOS	24	0x000000	offset correction register
70	VE DMCOC	24	0x000000	Corresponding channel effective value
/F	VB_RMSOS	24		offset correction register
80	VC BMSOS		0x000000	Corresponding channel effective value
80	VC_RMSOS	24		offset correction register
				[23:12] Corresponding to a phase
	WA_LOS_A/			active small signal compensation
00				register, complement. [11:0]
82	VAR_LOS_A	24	0x000000	Corresponding to a phase reactive
				small signal compensation register,
				complement.
	WALOS D/			[23:12] Corresponds to b-phase active
83	WA_LOS_B/ 24 0	0x000000	small signal compensation register,	
	VAK_LOS_B			complement. [11:0] Corresponds to b-



				phase reactive small signal
				compensation register, complement.
				[23:12] CORRESPONDS TO THE C-
				PHASE ACTIVE SMALL SIGNAL
				COMPENSATION REGISTER,
	WA_LOS_C/			COMPLEMENT. [11:0]
84	VAR_LOS_C	24	0x000000	CORRESPONDS TO THE C-
				PHASE REACTIVE SMALL
				SIGNAL COMPENSATION
				REGISTER, COMPLEMENT.
	FWA_LOS_A /FVAR_LOS_A	24	0x000000	[11:0] Corresponding to the reactive
85				power small signal compensation
				register, complement.
	FWA_LOS_B/ FVAR_LOS_B	24	0x000000	[11:0] Corresponding to the reactive
86				power small signal compensation
				register, complement.
				[11:0] Corresponding to the reactive
87	FWA_LOS_C/	24	0x000000	power small signal compensation
	FVAR_LOS_C			register, complement.
	VAR_CREEP/			[23:12] Reactive anti-creeping power
88	WA_CREEP	24	0x04C04C	threshold register



				[11:0] is the active anti-creeping power
				threshold register
				[23:12] is the total reactive power anti-
80	VAR_CREEP2/	24	0000000	creeping power threshold register
09	WA_CREEP2	24	0x000000	[11:0] total active anti-creeping power
				threshold register;
				[23:12] IS THE REVERSE
				INDICATION THRESHOLD
0.4	REVP_CREEP/	24	0x04C200	REGISTER REVP_CREEP;
0/1	RMS_CREEP	24		[11:0] IS THE EFFECTIVE VALUE
				SMALL SIGNAL THRESHOLD
				REGISTER RMS_CREEP
				[23:21] Channel fast effective value
				register refresh time, half cycle and n
8B	FAST_RMS_CTRL	24	0x20FFFF	cycle can be selected, the default is half
				cycle; [20:0] channel fast effective value
				threshold register
				[23:12] Current peak value threshold
8C	I_FKLVL/	24	0xFFFFFF	register i_pklvl; [11:0] Voltage peak
	V_PKLVL			value threshold register v_pklvl

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8D	ISUMLVL	24	0xFFFFFF	Current comparison threshold register, select NI_RMS to compare with the ISUMLVL register, if IN_RMS is less than ISUMLVL, the interrupt state ISUMLVL_out is 0; if IN_RMS is less than ISUMLVL, the interrupt state ISUMLVL_out is 1. Note that IN_RMS can be selected as the effective value of the algebraic sum of three-phase transient currents Or the zero line actually measures the effective value. The function is the same as PKLVL. Mode3[4]
8E	SAGCYC/ ZXTOUT	24	0x04FFFF	[23:16] Fall line period register sagcyc, default 04h. [15:0] Zero-crossing timeout register zxtout, if there is no zero-crossing signal within the time indicated by this register, a zero- crossing timeout interrupt will be generated, default ffffh.

8			Galat	Three phase newer monitoring and analysis
8F	SAGLVL/ LINECYC	24	0x100009	Three phase power monitoring and analysis[23:12] The drop voltage thresholdregister SAGLVL, the voltage channelinput is continuously lower than thevalue of this register for more than thetime in SAGCYC, and the line voltagedrop interrupt will be generated. Thedefault is 100H, about 1116 fullamplitude voltage input; [11: 0] Lineenergy accumulation cycle numberregister LINECYC, default 009H,representing 10 cycles. Line cycle isrelated to external crystal oscillator,recommended crystal oscillator is
90	IN_PHCAL	24	0x000000	IN phase current channel angle difference correction register, when IRMSmin <effective input<br="" of="" value="">current<p1, [7:0]="" correct="" is="" the<br="" to="" used="">current channel phase, [7] is the enable bit, the minimum adjustment delay time is 280ns, corresponding to 0.005</p1,></effective>



Degree 1LSB, maximum adjustable  $\pm$  0.625 degrees). When IRMSmin<effective value of input current<P1, [7:0] is used to correct the current channel phase, [7] is the enable bit, and the minimum adjustment delay time is 280ns, Corresponding to 0.005 degrees 1LSB, the maximum adjustable is  $\pm 0.625$  degrees). When P1<effective value of input current<P2, [15:8] is used to correct the phase of the current channel, [15] is the enable bit, and the adjustment accuracy is the same as above .When P2<effective value of input current<IRMSmax, [23:16] is used to correct the current channel phase, [23] is the enable bit, and the adjustment accuracy is the same as above. Corresponding channel effective value 91 ISUM\_RMSGN 16 0x0000gain adjustment register

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02	ISUM RMSOS	24	0×000000	Corresponding channel effective value
52	150M_AW505	24	0x000000	offset correction register
				Enable control of 7 channels adc
				[2]: C PHASE CURRENT
				[3]: B-PHASE CURRENT
02		11	0.000	[4]: Phase a current
93	ADC_PD	11	0x000	[5]: Neutral line current
				[8]: Phase a voltage
				[9]: B-PHASE VOLTAGE
				[10]:C-PHASE VOLTAGE
				[15] Temperature measurement switch,
0.4	TPS_CTRL	16	0x07FF	0xb1 temperature measurement is off,
94				0xb0 is turned on, default 0xb0,
				temperature measurement is turned on
96	MODE1	24	0x000000	User mode selection register 1
97	MODE2	24	0x000000	User mode selection register 2
98	MODE3	24	0x000000	User mode selection register 3
				Interrupt mask register, which controls
0.4	MASIZI	24	0000000	whether an interrupt generates a valid
94	MASKI		0x000000	irq1 output, see "Interrupt Mask
				Register" description for details

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				Interrupt mask register, which controls
OP			whether an interrupt generates a valid	
96	MASKZ	24	0x000000	irq2 output, see "Interrupt Mask
				Register" description for details
				Energy clearing setting register, see
9D	RST_ENG	24	0x000000	"Energy clearing setting register"
				description for details
9E	USR_WRPROT	16	0x0000	User write protection setting register
				When the input is 5a5a5a, the system is
				reset-only the state machine and
0E	COPT DESET	24	0.000000	registers of the digital part are reset!
9F	SOFI_KESEI	24	0x000000	When the input is 55AA55, the user
				read and write registers are reset-Reset:
				reg60 to reg9f, rega0 to regd0

# 4.3 Calibration p register

Calibration register

address	Name	Bit width	Defaults	description
A 1	IC CHCN	NI 16 0.0000		Corresponding channel gain adjustment
$\Lambda 1$	ic_chow	10	0x0000	register, complement



A2	IB_CHGN	16	0x0000	Corresponding channel gain adjustment register, complement
А3	IA_CHGN	16	0x0000	Corresponding channel gain adjustment register, complement
A4	IN_CHGN	16	0x0000	Corresponding channel gain adjustment register, complement
Α7	VA_CHGN	16	0x0000	Corresponding channel gain adjustment register, complement
A8	VB_CHGN	16	0x0000	Corresponding channel gain adjustment register, complement
A9	VC_CHGN	16	0x0000	Corresponding channel gain adjustment register, complement
AC	IC_CHOS	16	0x0000	Corresponding channel offset adjustment register, complement
AD	IB_CHOS	16	0x0000	Corresponding channel offset adjustment register, complement
AE	IA_CHOS	16	0x0000	Corresponding channel offset adjustment register, complement
AF	IN_CHOS	16	0x0000	Corresponding channel offset adjustment register, complement

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B2	VA_CHOS	16	0x0000	Corresponding channel offset adjustment register, complement
В3	VB_CHOS	16	0x0000	Corresponding channel offset adjustment
B4	VC_CHOS	16	0x0000	Corresponding channel offset adjustment register, complement
B6	WATTGN_A	16	0x0000	Corresponding channel active power gain adjustment register, complement
B7	WATTGN_B	16	0x0000	Corresponding channel active power gain adjustment register, complement
B8	WATTGN_C	16	0x0000	Corresponding channel active power gain adjustment register, complement
В9	VARGN_A	16	0x0000	Corresponding channel reactive power gain adjustment register, complement
ВА	VARGN_B	16	0x0000	Corresponding channel reactive power gain adjustment register, complement
BB	VARGN_C	16	0x0000	Corresponding channel reactive power gain adjustment register, complement
ВС	FVARGN_A	16	0x0000	Corresponding channel reactive power gain adjustment register, complement

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BD	FVARGN_B	16	0x0000	Corresponding channel reactive power gain adjustment register, complement
BE	FVARGN_C	16	0x0000	Corresponding channel reactive power gain
				adjustment register, complement
BF	VAGN A	16	0x0000	Corresponding channel apparent power gain
	_			adjustment register, complement
CO	VAGN B	16	0x0000	Corresponding channel apparent power gain
		10	ONOUGO	adjustment register, complement
C1	VACN C	16	0x0000	Corresponding channel apparent power gain
CI	VIION_C	10	0x0000	adjustment register, complement
C2	WATTOS A	16	0x0000	Corresponding channel active power bias
02	w//1105_//	10	0x0000	adjustment register, complement
C3	WATTOS B	16	0x0000	Corresponding channel active power bias
0.5	w//105_b	10	0x0000	adjustment register, complement
C4	WATTOS C	16	0::0000	Corresponding channel active power bias
C4	wATTO5_C	10	0x0000	adjustment register, complement
CE	WAROS A	16	0-0000	Corresponding channel reactive power bias
	VAKOS_A	16	0x0000	adjustment register, complement
66	WAROS P	16	0-0000	Corresponding channel reactive power bias
	VARU5_B	10	0x0000	adjustment register, complement

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С7	VAROS_C	16	0x0000	Corresponding channel reactive power bias adjustment register, complement
C8	FVAROS A	16	0x0000	Corresponding channel reactive power bias
	_			adjustment register, complement
<u> </u>	EVAROS B	16	0x0000	Corresponding channel reactive power bias
	1 //11(00_1)	10	0.0000	adjustment register, complement
CA	EVAROS C	16	0x0000	Corresponding channel reactive power bias
CII	1 111105_0	10	0x0000	adjustment register, complement
CB	VAOS A	16	0x0000	Corresponding channel apparent power bias
CD	V1105_11	10	0x0000	adjustment register, complement
AND	VAOS B	16	00000	Corresponding channel apparent power bias
СС	VAO5_B	10	0x0000	adjustment register, complement
CD	VAOS C	16	0x0000	Corresponding channel apparent power bias
CD	V1105_C	10	0x0000	adjustment register, complement
CE	CFDIV	12	0x010	Active cf scaling register [11:0]
				Calibration register checksum, checksum
D0	checksum	16	0x0010	has problems and restores to the default
				value



## 4.4 Mode register

### 4.4.1 Mode register 1

0x96	MODE1		Working mode register
No.	name	default value	description
[10:0]		00	Keep
[21:11]		00	Keep
			Leakage selection through high pass, the
[22]	L_F_SEL	1'b0	default is 0 to select no high pass, and 1 to
			select high pass
			Current wave waveform register output
[23]	WAVE DEC SEI	1150	selection, default 0 selects the waveform of
[23]	WAVE_REG_SEL	1.00	the normal current channel, and 1 selects the
			waveform output of the leakage channel

## 4.4.2 Mode register 2

0x97	MODE2		Working mode register
No.	name	default value	description
			RMS waveform selection, 00-high pass, 01-
[21.0]	WAVE DMC CEI	11{2 <b>'</b> b00}	select fundamental wave, 11-select sinc
[21:0]	WAVE_RM3_SEL		output
			[3,2]: C PHASE CURRENT

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			[5,4]: B-PHASE CURRENT
			[7,6]: Phase a current
			[8,9]: Neutral line current
			[15,14]: PHASE A VOLTAGE
			[17,16]: PHASE B VOLTAGE
			[19,18]:C-PHASE VOLTAGE
			Slow effective value register update speed
[22]	RMS_UPDATE_SEL	1 <b>'</b> b0	selection, 1 is 1000ms, 0 is 500ms, 500ms is
			selected by default;
[23]	AC EREO SEL	150	AC frequency selection, 1 is 60Hz, 0 is
	AC_PREQ_SEL	1 DU	50Hz, default selection is 50Hz

## 4.4.3 Mode register 3

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0x98	MODE3		Working mode register
No.	name	default value	description
			When it is 0, compare the effective value of isumlvl and
[4]		411.0	NI_RMS output neutral current; when it is 1, the
[4]	isumivi_sei	1'ЪО	effective value of the sum of instantaneous waveforms
			of isumlvl and the output three-phase current;
[( []	1 1	2100	Line voltage frequency cycle channel selection 2'b00-A;
[0:5]	period_sel	2.00	2'b01-B; 2'b10-C; 2'b11-A

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[7]	1	111.0	va algorithm selection: 0-rmsi^2+rmsv^2; 1-
[/]	va_sel	1'60	(watt^2+var^2)^0.5
			watt and var conjoint sum addition method: 0-absolute
[8]	add_sel	1'b0	value addition, $ a + b + c $ ; 1-algebraic sum
			addition, a+b+c
[9]	cf_enable	1'b0	0-cf disable, default; 1-cf enable
[13:10]	CF_SEL	4'b0000	Channel cf_watt, cf_var output selection, The default is 0000, turn off cf_watt, cf_var; 0001, the power CF of watt_aavar_a; 0010, the power CF of watt_bbvar_b; 0011, power CF of watt_ccvar_c; 0100, power CF of watttvar; 0101, watt_p_aavar1 power CF; 0110, watt_p_bbvar2 power CF; 0111, power CF of watt_p_ccvar3; 1000, power CF of watt_ppvar4; 1001, watt_n_aava_a power CF; 1010, watt_n_va_b power CF; 1011,watt_n_ccva_c power CF; 1100,watt_nnva power CF; 1101, (SAME AS 0100); 1110, APPARENT POWER CF; 1111, CLOSE CF;
[14]			Keep
[15]	cf_add_sel	1'Ь0	Watt and var energy addition methods: 0-absolute value addition; 1-algebraic sum addition (separation and combination)
[16]	var_sel	1'b0	Var energy selection: 0-fundamental wave; 1-full wave
[17]	watt_sel	1'b0	Watt waveform selection: 0-full wave, determined by mode1[10:0]; 1-fundamental wave, determined by mode1[21:11]
[18]	IRQ_SEL	1'b0	0-OUTPUT IRQ112, DEFAULT;



## 4.5 Interrupt status register

#### 4.5.1 STATUS1 REGISTER

Interrupt register 1 0x54

Bit	Interrupt flag	Defaults	description
0		0	Indicates that a phase line voltage drop interrupt is
0	SAG_A	0	generated, and the drop is 1
1	SAC B	0	Indicates that the voltage drop of phase b is interrupted, and
1	5/10_0	0	the drop is 1
2		0	Indicates that the voltage drop interruption of phase c is
2	SAG_C	0	generated, and the drop is 1
2		0	Indicate the generation of a phase zero crossing timeout
3	ZXIO_A	0	interrupt, the timeout is 1
4	ZVTO P	0	Indicates that the phase b zero-crossing timeout interrupt is
4	ZAIO_D	0	generated, and the timeout is 1
F		0	Indicate the generation of phase c zero-crossing timeout
5	ZATO_C	0	interrupt, the timeout is 1
6	ZX_VA	0	Indicate the sign bit of a phase voltage waveform
7	ZX_IA		Indicate the sign bit of phase a current waveform
8	ZX_VB		Indicate the sign bit of the b-phase voltage waveform
9	ZX_IB		Indicate the sign bit of phase b current waveform
10	ZX_VC		Indicate the sign bit of the c-phase voltage waveform

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11	ZX_IC		Indicate the sign bit of the c-phase current waveform
12	ZX_IN		Indicates the sign bit of the n-phase current waveform
12		0	Indicates that the peak value of the effective value of the a-
15	rk_vA	0	phase voltage channel exceeds pkvlvl interrupt, which is 1
			Indicates that the peak value of the effective value of the
14	PK_IA	0	phase a current channel exceeds the pkilvl interrupt, which is
			1
			Indicates that the peak value of the effective value of the
15	PK_VB	0	phase b voltage channel exceeds the pkvlvl interrupt, which
			is 1
			Indicates that the peak value of the effective value of the
		4	
16	PK_IB	0	phase b current channel exceeds the pkilvl interrupt, which is
16	PK_IB	0	phase b current channel exceeds the pkilvl interrupt, which is 1
16	PK_IB	0	phase b current channel exceeds the pkilvl interrupt, which is 1 Indicates that the peak value of the effective value of the c-
16	PK_IB PK_VC	0	phase b current channel exceeds the pkilvl interrupt, which is 1 Indicates that the peak value of the effective value of the c- phase voltage channel exceeds pkvlvl interrupt, which is 1
16	PK_IB PK_VC	0	phase b current channel exceeds the pkilvl interrupt, which is 1 Indicates that the peak value of the effective value of the c- phase voltage channel exceeds pkvlvl interrupt, which is 1 Indicates that the peak value of the effective value of the c-
16 17 18	PK_IB PK_VC PK_IC	0 0 0 0	phase b current channel exceeds the pkilvl interrupt, which is 1 Indicates that the peak value of the effective value of the c- phase voltage channel exceeds pkvlvl interrupt, which is 1 Indicates that the peak value of the effective value of the c- phase current channel exceeds the pkilvl interrupt, which is 1
16 17 18	PK_IB PK_VC PK_IC	0 0 0 0	phase b current channel exceeds the pkilvl interrupt, which is 1 Indicates that the peak value of the effective value of the c- phase voltage channel exceeds pkvlvl interrupt, which is 1 Indicates that the peak value of the effective value of the c- phase current channel exceeds the pkilvl interrupt, which is 1 Indicates that the peak value of the effective value of the n-
16 17 18 19	PK_IB PK_VC PK_IC PK_NI	0 0 0 0	phase b current channel exceeds the pkilvl interrupt, which is 1 Indicates that the peak value of the effective value of the c- phase voltage channel exceeds pkvlvl interrupt, which is 1 Indicates that the peak value of the effective value of the c- phase current channel exceeds the pkilvl interrupt, which is 1 Indicates that the peak value of the effective value of the n- phase current channel exceeds the pkilvl interrupt, which is 1

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			Voltage phase sequence, 0 is normal, 1 is reverse phase
21	PS_V	0	sequence, suitable for three-phase four-wire. When there is a
			phase failure, the output is 0;
			Indicate the current phase sequence, 0 is normal, 1 is the
			reverse phase sequence, the current phase sequence
22	PS_I	0	detection is only accurate when the current value is greater
			than 5%Ib; when there is a phase failure, the output is 0;

suitable for three-phase four-wire;

## 4.5.2 STATUS2 REGISTER

Interrupt register 2 0x55

B it	Interrupt flag	Defa ults	description
0	REVP_WAT	0	Indicates that the sign of phase a active power calculation has
	T_A		changed
1	REVP_WAT	0	Indicates that the sign of phase b active power calculation has
	T_B		changed
2	REVP_WAT	0	Indicates that the sign of the c-phase active power calculation
	T_C		has changed
3	REVP_VAR	0	Indicates that the sign of a phase reactive power calculation has
			changed
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		0	Indicates that the sign of phase b reactive power calculation has	
4	REVP_VAR	0	changed	
5	REVP_VAR	0	Indicates the sign change of c-phase reactive power calculation	
			Indicates that the sign of the phase a fundamental reactive power	
6	REVP_FVAR	0	calculation has changed	
_			Indicates that the sign of the phase b fundamental reactive	
/	REVP_FVAR	0	power calculation has changed	
		0	Indicate the sign change of c-phase fundamental reactive power	
8	KEVP_FVAR	0	calculation	
0	REVP_FWA		Indicate the sign change of the fundamental active power	
9	TT_A		calculation of phase a	
1	DEVD	0	Indicates that the sign of the fundamental active power	
0	REVP_ 0		calculation of phase b has changed	
1	REVP_FWA	0	Indicates that the sign of the c-phase fundamental active power	
1	0 TT_C		calculation has changed	
1			Indicates a sign change in the apparent power calculation of	
2	REVP_VA_A 0		phase a	
1	REVP_VA_B 0		Indicates that the apparent power calculation of phase b has a	
3			sign change	
1			Indicates that the apparent power calculation of phase c has a	
4	KEVI_VA_C	0	sign change	

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1	REVP_WAT		Indicates the sign change of the total active power calculation of			
5	Т	0	the combined phase			
1	REVP_FWA	_	Indicates the sign change of the total fundamental active power			
6	TT	0	calculation of the combined phase			
	REVP_WAT					
1	T_OR/		Indicates the sign change of the fundamental active power			
7	REVP_FWA	0	calculation of any one phase of the three-phase active power rate			
	TT_OR					
1	REVP_VAR_		Indicate the sign change of any phase reactive power calculation			
8	OR	0	in the three phases			
1	REVP_FAVR		Indicates that the fundamental reactive power calculation of any			
9	_OR	0	one of the three phases has a sign change			
2	REVP_VA_O		Indicates that the apparent power calculation of any one of the			
0	R	0	three phases has a sign change			
2			Indicates that the reference voltage value is low, when it is 1,			
1	VREF_LOW	0	vref<1v; when it is 0, it is normal			
2	SPI_INPUT_		SPI INPUT CHECK, WHEN IT IS 1, THE CHECKSUM IS			
2	ERR	0	WRONG; WHEN IT IS 0, IT IS NORMAL			
2	UART_INPU		UART INPUT CHECK, WHEN IT IS 1, THE CHECKSUM			
3	T_ERR	0	IS WRONG; WHEN IT IS 0, IT IS NORMAL			



# 5. Communication Interface

Register data are all sent in 3 bytes (24bit), register data less than 3 bytes, unused

bits are filled with 0, and 3 bytes are sent together.

Select by pin sel, when sel=1, it is spi, when sel=0, it is uart

# 5.1 SPI

#### 5.1.1 Overview

- ✓ Slave mode, half-duplex communication, maximum communication speed 1.5m
- ✓ 8-bit data transmission, MSB first, LSB behind
- ✓ Fix a clock polarity phase (cpol=0, cpha=1)

#### 5.1.2 Operating mode

The master device works in Mode1: CPOL=0, CPHA=1, that is, in the idle state,

SCLK is at low level, and the data transmission is on the first edge, that is, the transition of SCLK from low to high, so Data sampling is on the falling edge, and data

transmission is on the rising edge.



#### 5.1.3 Frame structure

In the communication mode, first send the 8bit identification byte (0x81) or (0x82), (0x82) is the read identification byte, (0x81) is the write identification byte, and then the register address byte is sent to determine the address of the access register (Please refer to the BL6552 register list). The following figure shows the data transfer sequence of read and write operations respectively. After one frame of data transfer is completed, BL6552 re-enters the communication mode. The number of SCLK pulses required for each read and write operation Both are 48 bits.

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There are two types of frame structures, which are explained as follows:

1) Write register

Cmd: {0x81}+ Addr+Data\_H+Data\_M+Data\_L+SUM

{0x81} is the frame identification byte of the write operation;

Addr is the internal register address of BL6552 corresponding to the write

operation;

The checksum byte CHECKSUM is

(((0x81)+ADDR+DATA\_H+DATA\_M+DATA\_L)& 0xFF) and then inverted by bit.

				-		
写操作帧	0x81	ADDR[7:0]	DATA_H[7:0]	DATA_M[7:0]	DATA_L[7:0]	CHECKSUM[7:0]

2) Read register

 $Cmd: \{0x82\} + Addr$ 

Returns: Data\_H+Data\_M+Data\_L+SUM

{0x82} is the frame identification byte of the read operation;

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Addr is the internal register address of BL6552 corresponding to the read operation (0x00-0xff);

Among them, the checksum byte CHECKSUM is

(((0x82)+ADDR+DATA\_H+DATA\_M+DATA\_L)& 0xFF) and then inverted by bit.

读命令帧	0x82	ADDR[7:0]				
读数据帧			DATA_H[7:0]	DATA_M[7:0]	DATA_L[7:0]	CHECKSUM[7:0]

### 5.1.4 Read operation timing

During the data read operation of bl6552, at the rising edge of sclk, bl6552 shifts the corresponding data out to the dout logic output pin. During the next time when the sclk is 1, the dout value remains unchanged, that is, at the next At the falling edge, the external device can sample the dout value. Like the data write operation, the MCU must first send the identification byte and address byte before the data read operation.



When BL6552 is in communication mode, the frame identification byte {0x82} indicates that the next data transfer operation is read. Then the byte immediately following is the address of the target register to be read. BL6552 starts to move out of the register on the rising edge of SCLK All the remaining bits of the register data are shifted out on the subsequent rising edge of SCLK. Therefore, on the falling edge, the external device can sample the output data of the SPI. Once the read operation is over, the serial interface will re-enter the communication mode At this time, the DOUT logic output enters a high impedance state on the falling edge of the last SCLK signal.

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### 5.1.5 Write operation timing

The serial writing sequence is carried out in the following manner. The frame identification byte {0x81} indicates that it is written during data transfer operations. The MCU will prepare the data bits that need to be written to BL6552 before the lower edge of SCLK, and at this clock of SCLK The lower edge of the SCLK starts to shift in the register data. All the remaining bits of the register data are also shifted to the left on the lower edge of the SCLK.



#### 5.1.6 Fault tolerance mechanism of spi interface

1) If the frame recognition byte is wrong or the sum byte is wrong, the frame data is abandoned.

2) SPI module reset: send 6 bytes of 0xFF through the SPI interface, and the SPI interface can be reset separately;

3) \_CS IS PULLED HIGH TO RESET.



# 5. 2 UART

## 5.2.1 Overview

- $\checkmark$  Select by pin uart\_sel, when sel=1, it is spi, when sel=0, it is uart
- ✓ The communication baud rate is 4800bpss9600bpss19200bpss38400bpss, no parity,

stop bit 1;

Baud rate	4800	9600	19200	38400
setting				
CS PIN	0	0	1	1
SCLK PIN	0	1	0	1

In uart mode, cs and sclk pins are used as baud rate setting pins.

### 5.2.2 Format per byte



Start bit low level duration t1=208us (4800bps);

The valid data bit time lasts t2=208\*8=1664us(4800bps);

Stop bit high level duration t3=2\*208u(4800bps)s;

## 5.2.3 Read timing



The host UART read data sequence is shown in the figure below. The host first sends the command byte (0x35), then the address byte (ADDR) that needs to be read, and then BL6552 sends the data byte in turn, and finally the checksum byte.

 $\{0x35\}$  is the frame identification byte of the read operation;



Addr is the internal register address of BL6552 corresponding to the read operation

(0x00-0xff);

	Description	Min	Туре	Max	Unit
t1	The interval between mcu sending bytes	0		20	mS
t2	Frame interval	0.5			uS
t3	The interval time from the end of MCU sending register address to bl050 sending byte during read operation		110		uS
t4	BL6552 INTERVAL TIME BETWEEN SENDING BYTES		1		Bit

The SUM byte is (Addr+Data\_L+Data\_M+Data\_H)&0xFF reverse;

## 5.2.4 Write timing



The host UART write data sequence is shown in the figure below. The host first sends the command byte (0xCA), then the write address byte (ADDR), then sends the data byte in turn, and finally the checksum byte.

{0xCA} is the frame identification byte of the write operation;

Addr is the internal register address of BL6552 corresponding to the write

operation;



The CHECKSUM byte is ((ADDR+Data\_L+Data\_M+Data\_H)& 0xFF) and then inverted by bit.

## 5.2.5 Protection mechanism of uart interface

- The UART communication of BL6552 provides a time-out protection mechanism.If the interval between bytes exceeds 18.5mS, the UART interface will automatically reset.
- If the frame recognition byte is wrong or the checksum byte is wrong, the frame data is abandoned.
- UART module reset: The RX pin is pulled high after the low level exceeds 32 bps (6.67ms at 4800 bps), and the UART module is reset.

# 6. Package information

BELLING

## 6.1 order information

BL6552 QFN36 PACKAGE

# 6. 2 Package

Moisture sensitivity level MSL 3

Warranty Two years

Packing Taping

smallest packaging 4000/reel

## Package appearance



**BL6552** Three phase power monitoring and analysis

SIDE VIEW



**BL6552** Three phase power monitoring and analysis

SYMBOL	MILLIMETER				
SIMBOL	MIN	NOM	MAX		
Α	0.80 0.85		0.90		
A1	0.00	0.02	0.05		
b	0.18	0.23	0.30		
b1		0.16REF			
с	0.18	0.20	0.23		
D	5.90	6.00	6.10		
D2	3.80	3.90	4.00		
Nd	3.95	4.00	4.05		
e		0. 50BSC			
Е	5.90	6.00	6.10		
E2	3.80	3. 90	4.00		
Ne	3.95	4.00	4.05		
L	0.50	0.55	0.60		
L1	0.10REF				
h	0.30 0.35 0.40				
L/F载体尺寸 (MIL)	181X181				