74LVC2G00 Dual 2-input NAND gate

Rev. 16 — 20 June 2022

1. General description

The 74LVC2G00 is a dual 2-input NAND gate. Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V environments.

Schmitt-trigger action at all inputs makes the circuit tolerant of slower input rise and fall times.

This device is fully specified for partial power down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

2. Features and benefits

- Wide supply voltage range from 1.65 V to 5.5 V
- 5 V tolerant outputs for interfacing with 5 V logic
- High noise immunity
- ±24 mA output drive (V_{CC} = 3.0 V)
- CMOS low power dissipation
- I_{OFF} circuitry provides partial Power-down mode operation
- Complies with JEDEC standard:
 - JESD8-7 (1.65 V to 1.95 V)
 - JESD8-5 (2.3 V to 2.7 V)
 - JESD8-B/JESD36 (2.7 V to 3.6 V)
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels
- Overvoltage tolerant inputs to 5.5 V
- ESD protection:
 - HBM JESD22-A114F exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from -40 °C to +85 °C and -40 °C to +125 °C



3. Ordering information

Table	1. Ordering	information

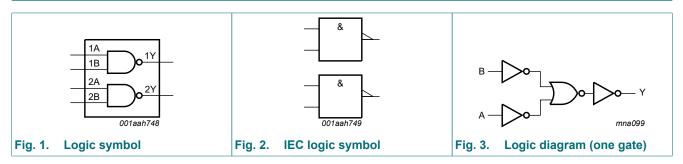
Type number	Package					
	Temperature range	Name	Description	Version		
74LVC2G00DP	-40 °C to +125 °C	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm	<u>SOT505-2</u>		
74LVC2G00DC	-40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	<u>SOT765-1</u>		
74LVC2G00GT	-40 °C to +125 °C	XSON8	plastic extremely thin small outline package; no leads; 8 terminals; body 1 × 1.95 × 0.5 mm	<u>SOT833-1</u>		
74LVC2G00GF	-40 °C to +125 °C	XSON8	extremely thin small outline package; no leads; 8 terminals; body 1.35 × 1 × 0.5 mm	<u>SOT1089</u>		
74LVC2G00GM	-40 °C to +125 °C	XQFN8	plastic, extremely thin quad flat package; no leads; 8 terminals; body 1.6 × 1.6 × 0.5 mm	<u>SOT902-2</u>		
74LVC2G00GN	-40 °C to +125 °C	XSON8	extremely thin small outline package; no leads; 8 terminals; body 1.2 × 1.0 × 0.35 mm	<u>SOT1116</u>		
74LVC2G00GS	-40 °C to +125 °C	XSON8	extremely thin small outline package; no leads; 8 terminals; body 1.35 × 1.0 × 0.35 mm	<u>SOT1203</u>		
74LVC2G00GX	-40 °C to +125 °C	X2SON8	plastic thermal enhanced extremely thin small outline package; no leads; 8 terminals; body 1.35 × 0.8 × 0.32 mm	<u>SOT1233-2</u>		

4. Marking

Table 2. Marking codes	Table 2. Marking codes			
Type number	Marking code[1]			
74LVC2G00DP	V2G00			
74LVC2G00DC	V00			
74LVC2G00GT	V00			
74LVC2G00GF	VA			
74LVC2G00GM	V00			
74LVC2G00GN	VA			
74LVC2G00GS	VA			
74LVC2G00GX	VA			

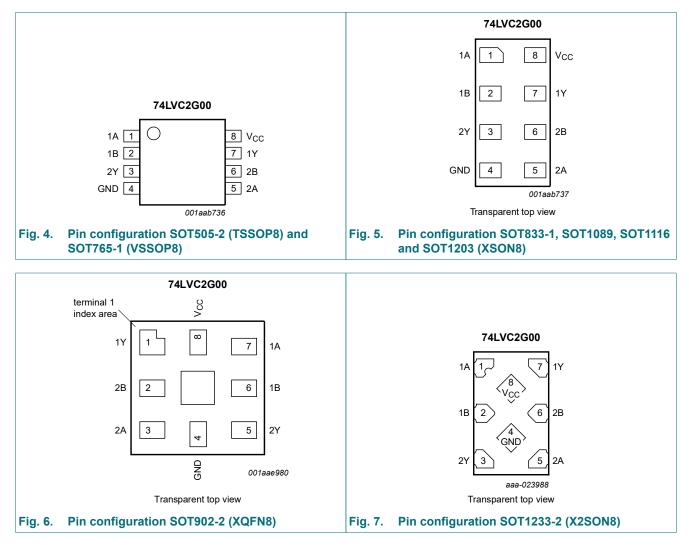
[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram



6. Pinning information





6.2. Pin description

Table 3. Pin des Symbol	cription Pin				
	SOT505-2, SOT765-1, SOT833-1, SOT1089, SOT1116, SOT1203 and SOT1233-2	SOT902-2	Description		
1A, 2A	1, 5	7, 3	data input		
1B, 2B	2, 6	6, 2	data input		
GND	4	4	ground (0 V)		
1Y, 2Y	7, 3	1, 5	data output		
V _{CC}	8	8	supply voltage		

74LVC2G00

7. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level.

Input C		Output
nA	nB	nY
L	L	Н
L	Н	Н
Н	L	Н
Н	Н	L

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{CC}	supply voltage			-0.5	+6.5	V
VI	input voltage		[1]	-0.5	+6.5	V
Vo	output voltage	Active mode	[1]	-0.5	V _{CC} + 0.5	V
		Power-down mode; V_{CC} = 0 V	[1]	-0.5	+6.5	V
I _{IK}	input clamping current	V _I < 0 V		-50	-	mA
I _{OK}	output clamping current	V_{O} < 0 V or V_{O} > V_{CC}		-	±50	mA
I _O	output current	$V_{O} = 0 V \text{ to } V_{CC}$		-	±50	mA
I _{CC}	supply current			-	100	mA
I _{GND}	ground current			-100	-	mA
T _{stg}	storage temperature			-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C				
		All packages except SOT1233-2	[2]	-	250	mW
		SOT1233-2 package	[3]	-	300	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

- [2] For SOT505-2 (TSSOP8) package: P_{tot} derates linearly with 4.6 mW/K above 96 °C.
 For SOT765-1 (VSSOP8) package: P_{tot} derates linearly with 4.9 mW/K above 99 °C.
 For SOT833-1 (XSON8) package: P_{tot} derates linearly with 3.1 mW/K above 68 °C.
 For SOT1089 (XSON8) package: P_{tot} derates linearly with 4.0 mW/K above 88 °C.
 For SOT902-2 (XQFN8) packages: P_{tot} derates linearly with 4.1 mW/K above 89 °C.
 For SOT1116 (XSON8) package: P_{tot} derates linearly with 4.2 mW/K above 90 °C.
 For SOT1203 (XSON8) package: P_{tot} derates linearly with 3.6 mW/K above 81 °C.
- [3] For SOT1233-2 (X2SON8) package: Ptot derates linearly with 7.7 mW/K above 118 °C.

9. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Мах	Unit
V _{CC}	supply voltage		1.65	5.5	V
VI	input voltage		0	5.5	V
Vo	output voltage	Active mode	0	V _{CC}	V
		Power-down mode; V _{CC} = 0 V	0	5.5	V
T _{amb}	ambient temperature		-40	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 1.65 V to 2.7 V	-	20	ns/V
		V _{CC} = 2.7 V to 5.5 V	-	10	ns/V

10. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
T _{amb} = -4	0 °C to +85 °C					
V _{IH} HIC	HIGH-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}	-	-	V
		V _{CC} = 2.3 V to 2.7 V	1.7	-	-	V
		V _{CC} = 2.7 V to 3.6 V	2.0	-	-	V
		V_{CC} = 4.5 V to 5.5 V	0.7 × V _{CC}	-	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 1.65 V to 1.95 V	-	-	0.35 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	-	-	0.7	V
		V _{CC} = 2.7 V to 3.6 V	-	-	0.8	V
		V _{CC} = 4.5 V to 5.5 V	-	-	0.3 × V _{CC}	V
V _{OH}	HIGH-level output voltage	$V_{I} = V_{IH} \text{ or } V_{IL}$				
		I_{O} = -100 µA; V_{CC} = 1.65 V to 5.5 V	V _{CC} - 0.1	-	-	V
		I _O = -4 mA; V _{CC} = 1.65 V	1.2	1.53	-	V
		I _O = -8 mA; V _{CC} = 2.3 V	1.9	2.13	-	V
		I _O = -12 mA; V _{CC} = 2.7 V	2.2	2.50	-	V
		I _O = -24 mA; V _{CC} = 3.0 V	2.3	2.60	-	V
		I _O = -32 mA; V _{CC} = 4.5 V	3.8	4.10	-	V
V _{OL}	LOW-level output voltage	$V_{I} = V_{IH} \text{ or } V_{IL}$				
		I_0 = 100 µA; V_{CC} = 1.65 V to 5.5 V	-	-	0.1	V
		I _O = 4 mA; V _{CC} = 1.65 V	-	0.08	0.45	V
		I _O = 8 mA; V _{CC} = 2.3 V	-	0.14	0.3	V
		I _O = 12 mA; V _{CC} = 2.7 V	-	0.19	0.4	V
		I _O = 24 mA; V _{CC} = 3.0 V	-	0.37	0.55	V
		I _O = 32 mA; V _{CC} = 4.5 V	-	0.43	0.55	V
I _I	input leakage current	V_{I} = 5.5 V or GND; V_{CC} = 0 V to 5.5 V	-	±0.1	±1	μA
I _{OFF}	power-off leakage current	$V_{I} \text{ or } V_{O} = 5.5 \text{ V}; V_{CC} = 0 \text{ V}$	-	±0.1	±2	μA
I _{CC}	supply current	V_{I} = 5.5 V or GND; V_{CC} = 1.65 V to 5.5 V; I_{O} = 0 A	-	0.1	4	μA

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
ΔI _{CC}	additional supply current	per pin; V _I = V _{CC} - 0.6 V; V _{CC} = 2.3 V to 5.5 V; I _O = 0 A	-	5	500	μA
Cı	input capacitance		-	2.5	-	pF
T _{amb} = -4	0 °C to +125 °C					
VIH	HIGH-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}	-	-	V
		V _{CC} = 2.3 V to 2.7 V	1.7	-	-	V
		V _{CC} = 2.7 V to 3.6 V	2.0	-	-	V
		V _{CC} = 4.5 V to 5.5 V	0.7 × V _{CC}	-	-	V
VIL	LOW-level input voltage	V _{CC} = 1.65 V to 1.95 V	-	-	0.35 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	-	-	0.7	V
		V _{CC} = 2.7 V to 3.6 V	-	-	0.8	V
		V_{CC} = 4.5 V to 5.5 V	-	-	$0.3 \times V_{CC}$	V
V _{OH}	HIGH-level output voltage	$V_{I} = V_{IH} \text{ or } V_{IL}$				
		I_{O} = -100 µA; V_{CC} = 1.65 V to 5.5 V	V _{CC} - 0.1	-	-	V
		I _O = -4 mA; V _{CC} = 1.65 V	0.95	-	-	V
		I _O = -8 mA; V _{CC} = 2.3 V	1.7	-	-	V
		I _O = -12 mA; V _{CC} = 2.7 V	1.9	-	-	V
		I _O = -24 mA; V _{CC} = 3.0 V	2.0	-	-	V
		I _O = -32 mA; V _{CC} = 4.5 V	3.4	-	-	V
V _{OL}	LOW-level output voltage	$V_{I} = V_{IH} \text{ or } V_{IL}$				
		I_{O} = 100 µA; V_{CC} = 1.65 V to 5.5 V	-	-	0.1	V
		I _O = 4 mA; V _{CC} = 1.65 V	-	-	0.70	V
		I _O = 8 mA; V _{CC} = 2.3 V	-	-	0.45	V
		I _O = 12 mA; V _{CC} = 2.7 V	-	-	0.60	V
		I _O = 24 mA; V _{CC} = 3.0 V	-	-	0.80	V
		I _O = 32 mA; V _{CC} = 4.5 V	-	-	0.80	V
l _l	input leakage current	V_{I} = 5.5 V or GND; V_{CC} = 0 V to 5.5 V	-	-	±1	μA
I _{OFF}	power-off leakage current	$V_{I} \text{ or } V_{O} = 5.5 \text{ V}; V_{CC} = 0 \text{ V}$	-	-	±2	μA
I _{CC}	supply current	V_{I} = 5.5 V or GND; V_{CC} = 1.65 V to 5.5 V; I_{O} = 0 A	-	-	4	μA
ΔI _{CC}	additional supply current	per pin; V _I = V _{CC} - 0.6 V; V _{CC} = 2.3 V to 5.5 V; I _O = 0 A	-	-	500	μA

[1] All typical values are measured at T_{amb} = 25 °C.

11. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground 0 V); for test circuit see Fig. 9.

Symbol	Parameter	Conditions	T _{amb} = -40 °C to +85 °C			+85 °C T _{amb} = -40 °C to +125 °C		
			Min	Typ <mark>[1]</mark>	Мах	Min	Мах	
t _{pd}	propagation delay	nA, nB to nY; see Fig. 8 [2]						
		V _{CC} = 1.65 V to 1.95 V	1.2	3.5	8.6	1.2	10.8	ns
		V _{CC} = 2.3 V to 2.7 V	0.7	2.3	4.8	0.7	6.0	ns
		V _{CC} = 2.7 V	0.7	3.0	5.6	0.7	7.0	ns
		V _{CC} = 3.0 V to 3.6 V	0.7	2.2	4.3	0.7	5.4	ns
		V_{CC} = 4.5 V to 5.5 V	0.5	1.8	3.3	0.5	4.2	ns
C _{PD}	power dissipation capacitance	per gate; $V_I = GND$ to V_{CC} [3]	-	14	-	-	-	pF

Typical values are measured at nominal V_{CC} and at T_{amb} = 25 °C. [1]

[2]

 t_{pd} is the same as t_{PLH} and t_{PHL} . C_{PD} is used to determine the dynamic power dissipation (P_D in μ W). $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o)$ where: [3]

 f_i = input frequency in MHz;

 $f_o = output$ frequency in MHz;

 C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching; $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

11.1. Waveforms and test circuit

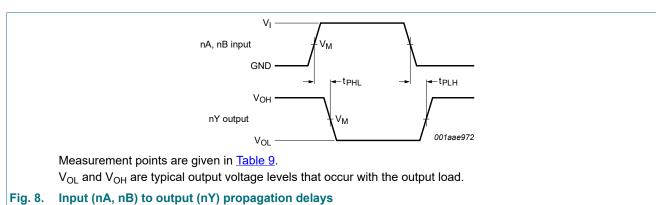
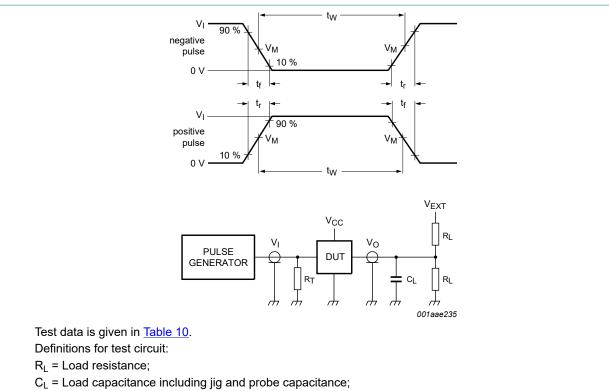


Table 9. Measurement points

Supply voltage	Input	Output
V _{cc}	V _M	V _M
1.65 V to 1.95 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
2.3 V to 2.7 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
2.7 V	1.5 V	1.5 V
3.0 V to 3.6 V	1.5 V	1.5 V
4.5 V to 5.5 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$

Dual 2-input NAND gate



 R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator;

 V_{EXT} = Test voltage for switching times.

Fig. 9. Test circuit for measuring switching times

Table 10. Test data

Supply voltage	Input		Load	Load	
V _{cc}	VI	t _r , t _f	CL	RL	t _{PLH} , t _{PHL}
1.65 V to 1.95 V	V _{CC}	≤ 2.0 ns	30 pF	1 kΩ	open
2.3 V to 2.7 V	V _{CC}	≤ 2.0 ns	30 pF	500 Ω	open
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open
4.5 V to 5.5 V	V _{CC}	≤ 2.5 ns	50 pF	500 Ω	open

12. Package outline

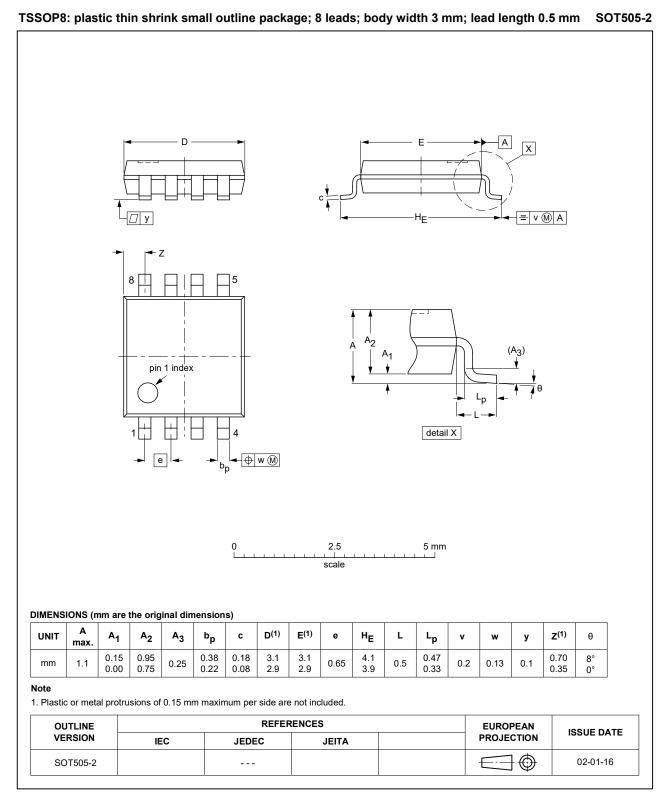


Fig. 10. Package outline SOT505-2 (TSSOP8)

74LVC2G00

Dual 2-input NAND gate

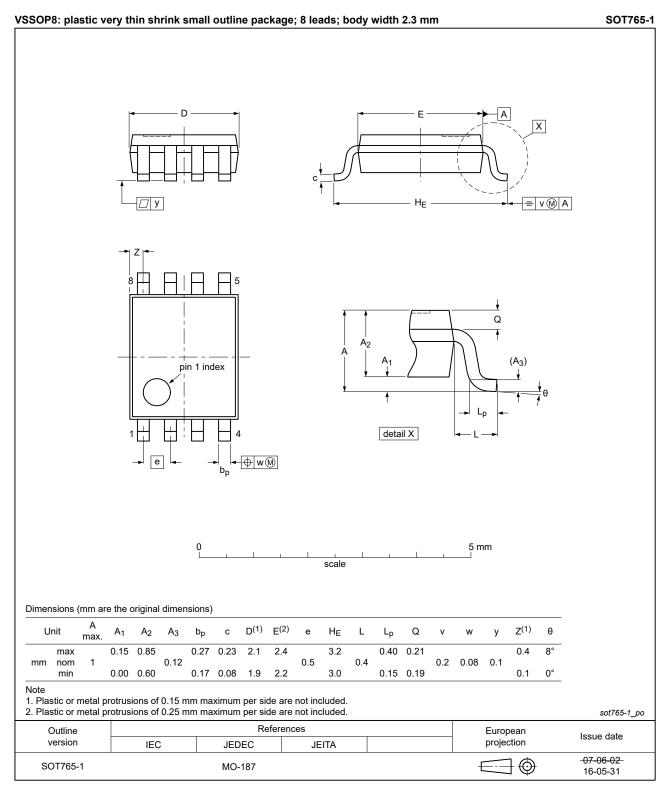


Fig. 11. Package outline SOT765-1 (VSSOP8)

Dual 2-input NAND gate

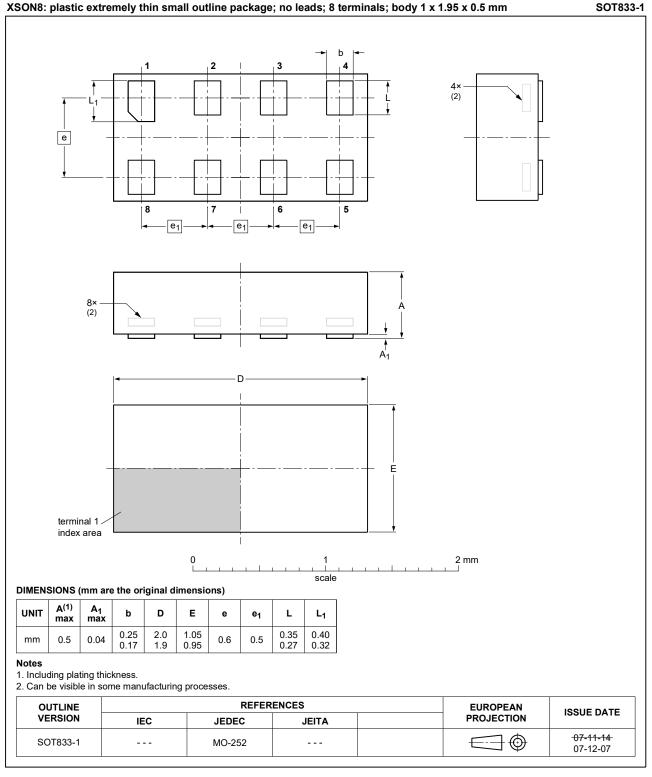
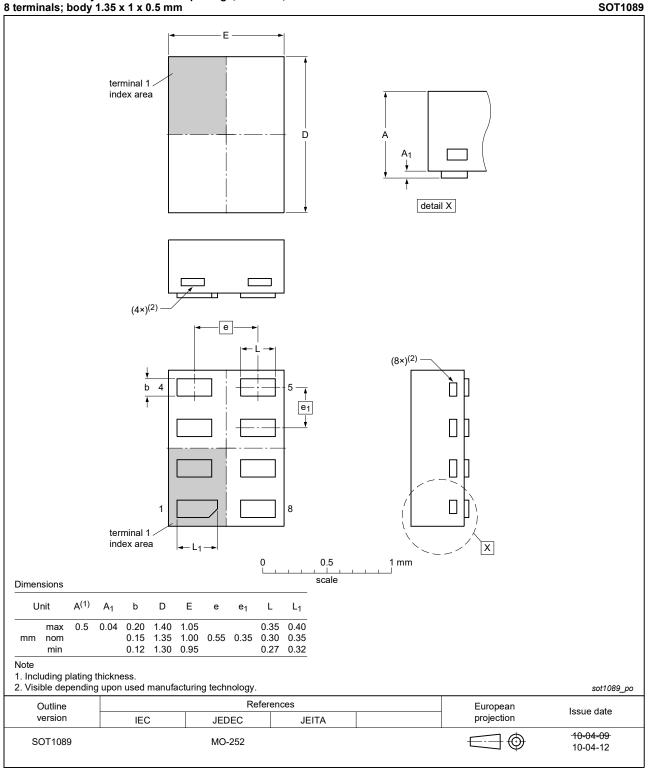


Fig. 12. Package outline SOT833-1 (XSON8)

Dual 2-input NAND gate



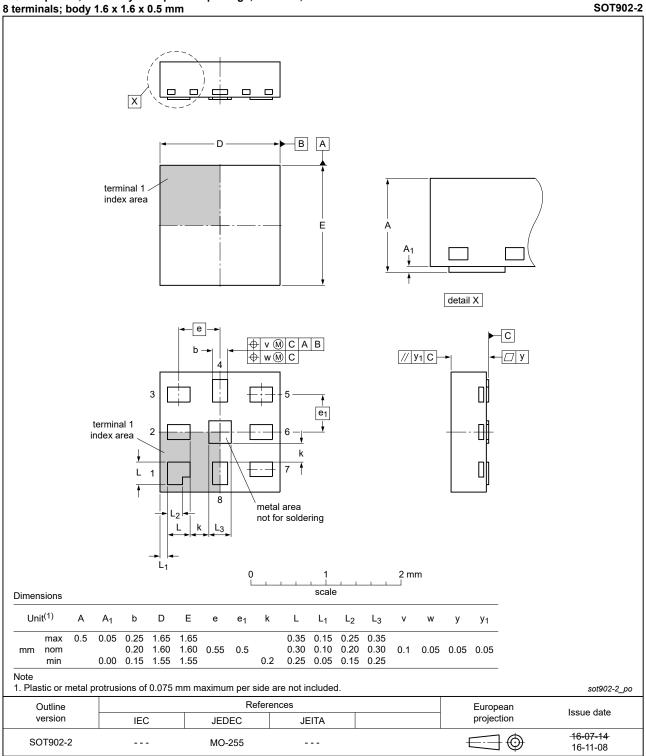
XSON8: extremely thin small outline package; no leads; 8 terminals; body 1.35 x 1 x 0.5 mm

Fig. 13. Package outline SOT1089 (XSON8)

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Dual 2-input NAND gate



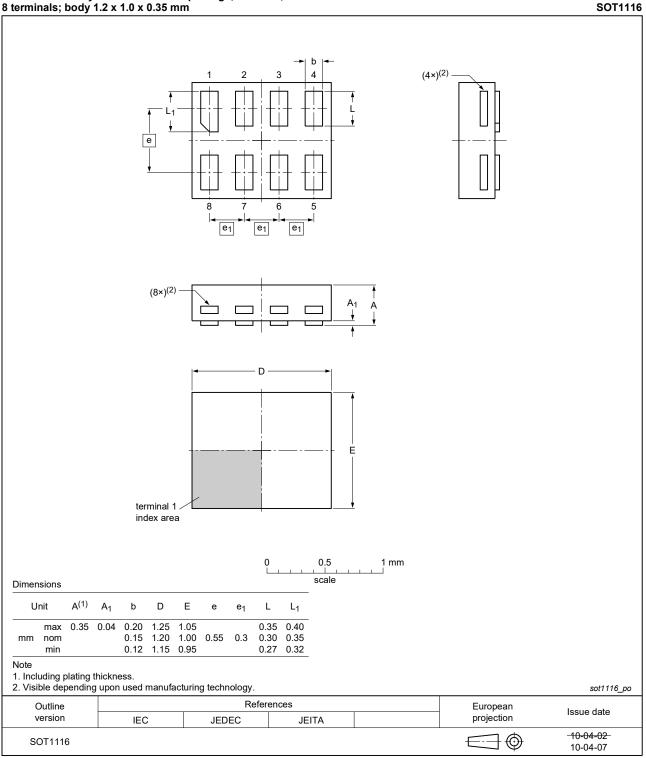
XQFN8: plastic, extremely thin quad flat package; no leads; 8 terminals; body 1.6 x 1.6 x 0.5 mm

Fig. 14. Package outline SOT902-2 (XQFN8)

Product data sheet

Dual 2-input NAND gate

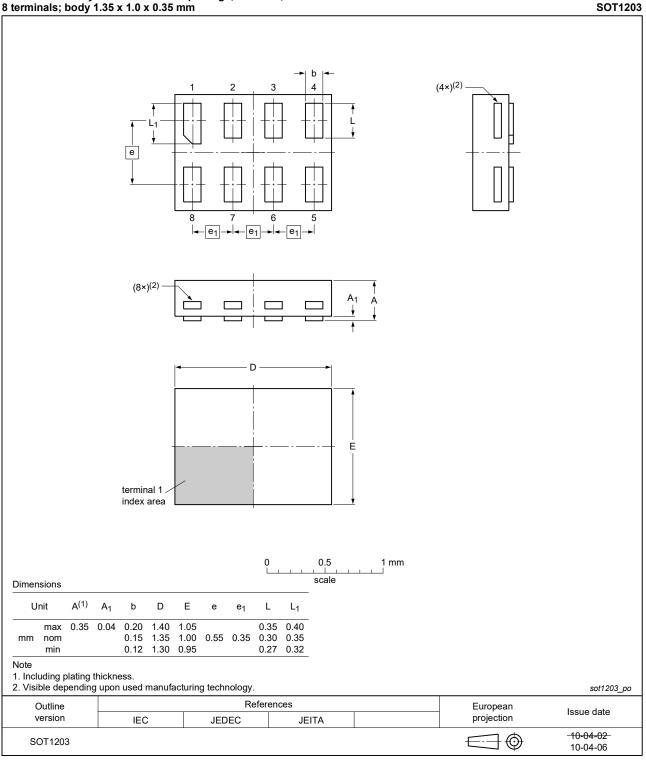
XSON8: extremely thin small outline package; no leads; 8 terminals; body 1.2 x 1.0 x 0.35 mm





Dual 2-input NAND gate

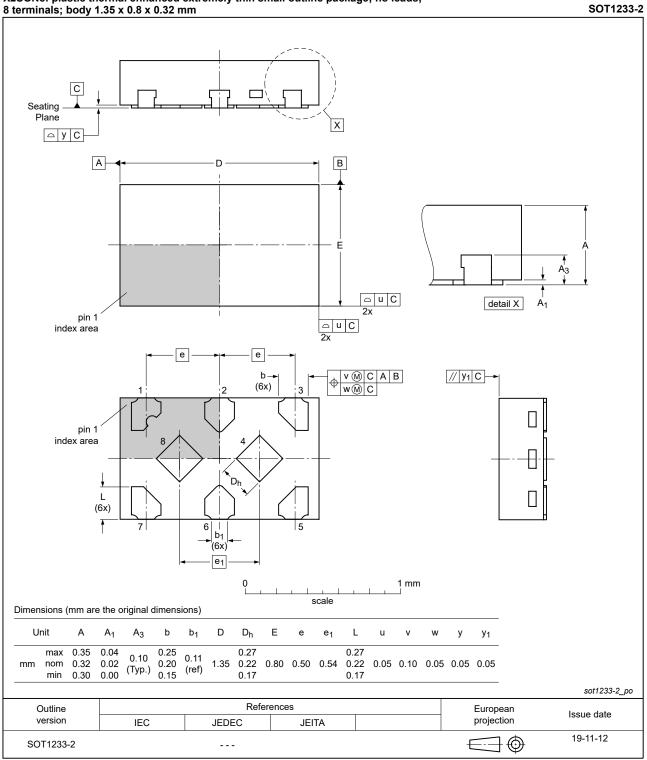
XSON8: extremely thin small outline package; no leads; 8 terminals; body 1.35 x 1.0 x 0.35 mm





Product data sheet

Dual 2-input NAND gate



X2SON8: plastic thermal enhanced extremely thin small outline package; no leads; 8 terminals; body 1.35 x 0.8 x 0.32 mm

Fig. 17. Package outline SOT1233-2 (X2SON8)

Product data sheet

13. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes	
74LVC2G00 v.16	20220620	Product data sheet	-	74LVC2G00 v.15	
Modifications:	 SOT1233 (X2SON8) package changed to SOT1233-2 (X2SON8) package. <u>Table 5</u>: P_{tot} total power dissipation and derating values have been updated. <u>Section 1</u> and <u>Section 2</u> updated. 				
74LVC2G00 v.15	20170703	Product data sheet	-	74LVC2G00 v.14	
Modifications:	 The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Fig. 17: Package outline drawing for SOT1233 has changed. Type number 74LVC2G00GD removed. 				
74LVC2G00 v.14	20161212	Product data sheet	-	74LVC2G00 v.13	
Modifications:	• <u>Table 7</u> : The maximum limits for leakage current and supply current have changed.				
74LVC2G00 v.13	20161028	Product data sheet	-	74LVC2G00 v.12	
Modifications:	Added type number 74LVC2G00GX (SOT1233/X2SON8)				
74LVC2G00 v.12	20130408	Product data sheet	-	74LVC2G00 v.11	
Modifications:	For type number 74LVC2G00GD XSON8U has changed to XSON8.				
74LVC2G00 v.11	20120622	Product data sheet	-	74LVC2G00 v.10	
Modifications:	• For type number 74LVC2G00GM the SOT code has changed to SOT902-2.				
74LVC2G00 v.10	20111130	Product data sheet	-	74LVC2G00 v.9	
Modifications:	Legal pages updated.				
74LVC2G00 v.9	20100608	Product data sheet	-	74LVC2G00 v.8	
74LVC2G00 v.8	20091026	Product data sheet	-	74LVC2G00 v.7	
74LVC2G00 v.7	20080610	Product data sheet	-	74LVC2G00 v.6	
74LVC2G00 v.6	20080220	Product data sheet	-	74LVC2G00 v.5	
74LVC2G00 v.5	20070904	Product data sheet	-	74LVC2G00 v.4	
74LVC2G00 v.4	20060515	Product data sheet	-	74LVC2G00 v.3	
74LVC2G00 v.3	20050201	Product specification	-	74LVC2G00 v.2	
74LVC2G00 v.2	20040923	Product specification	-	74LVC2G00 v.1	
74LVC2G00 v.1	20031117	Product specification	-	-	

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

 Please consult the most recently issued document before initiating or completing a design.

- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <u>https://www.nexperia.com</u>.

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