CSD16411Q3 25-V N-Channel NexFET™ Power MOSFET

1 Features

- Ultra-Low Q_g and Q_{gd}
- Low-Thermal Resistance
- Avalanche Rated
- Lead-Free Terminal Plating
- RoHS Compliant
- Halogen Free
- SON 3.3-mm × 3.3-mm Plastic Package

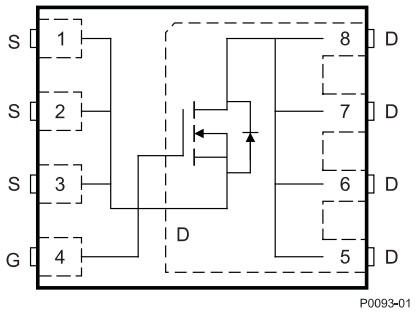
2 Applications

- Point-of-Load Synchronous Buck Converter for Applications in Networking, Telecom and Computing Systems
- Optimized for Control FET Applications

3 Description

This 25-V, 8-mΩ, 3.3-mm × 3.3-mm SON NexFET™ power MOSFET has been designed to minimize losses in power conversion applications.

Top View



Product Summary

T_A = 25°C		TYPICAL VALUE		UNIT
V_{DS}	Drain-to-Source Voltage	25		V
Q_g	Gate Charge Total (4.5 V)	2.9		nC
Q_{gd}	Gate Charge Gate-to-Drain	0.7		nC
$R_{DS(on)}$	Drain-to-Source On Resistance	V_{GS} = 4.5 V	12	mΩ
		V_{GS} = 10 V	8	
$V_{GS(th)}$	Threshold Voltage	2		V

Device Information(1)

DEVICE	QTY	MEDIA	PACKAGE	SHIP
CSD16411Q3	2500	13-Inch Reel	SON 3.30-mm × 3.30-mm Plastic Package	Tape and Reel
CSD16411Q3T	250			

(1) For all available packages, see the orderable addendum at the end of the data sheet.

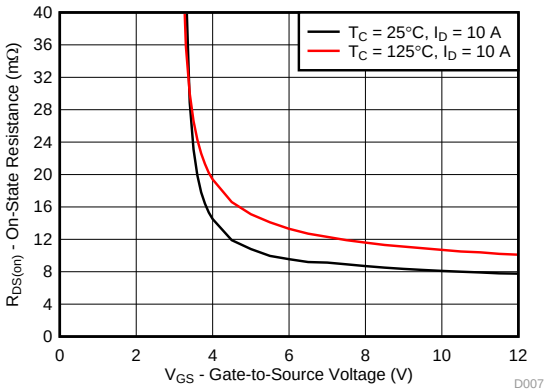
Absolute Maximum Ratings

T_A = 25°C		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	25	V
V_{GS}	Gate-to-Source Voltage	+16 / –12	V
I_D	Continuous Drain Current (Package Limited)	60	A
	Continuous Drain Current (Silicon Limited), T_C = 25°C	50	
	Continuous Drain Current(1)	14	
I_{DM}	Pulsed Drain Current, T_A = 25°C(2)	130	A
P_D	Power Dissipation(1)	2.87	W
	Power Dissipation, T_C = 25°C	35	
T_J, T_{STG}	Operating Junction Storage Temperature	–55 to 150	°C
E_{AS}	Avalanche Energy, Single Pulse I_D = 18 A, L = 0.1 mH, R_G = 25 Ω	16	mJ

(1) $R_{\theta JA}$ = 45°C/W on 1-in^2 Cu (2-oz) on 0.06-in thick FR4 PCB.

(2) Max $R_{\theta JC}$ = 3.5°C/W, pulse duration ≤ 100 μs, duty cycle ≤ 1%.

$R_{DS(ON)}$ vs V_{GS}



Gate Charge

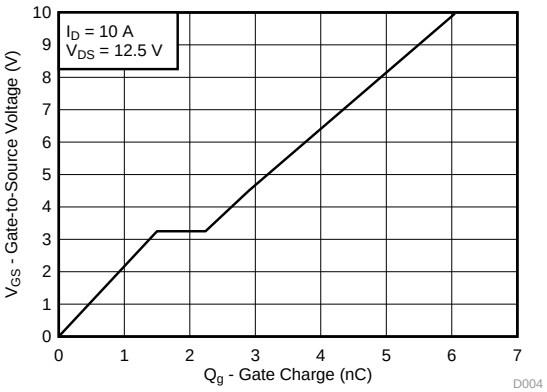


Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (September 2010) to Revision B **Page**

- Changed *Description* text ... 1
- Added silicon limited continuous drain current to *Absolute Maximum Ratings* table ... 1
- Added max power dissipation at T_C = 25°C to *Absolute Maximum Ratings* table ... 1
- Changed Note 2 in *Absolute Maximum Ratings* table ... 1
- Changed $R_{\theta JA}$ max from 59°C/W : to 55°C/W ... 3
- Changed the SOA in Figure 10 to reflect measured data ... 6
- Added *Device and Documentation Support* section ... 7
- Changed *MECHANICAL DATA* section to *Mechanical, Packaging, and Orderable Information* section ... 8

Changes from Original (August 2009) to Revision A **Page**

- Changed Figure 1 text From: $R_{\theta JA}$ = 92°C/W To: Typical $R_{\theta JA}$ = 93°C/W ... 4
- Changed Figure 10 text From: $R_{\theta JA}$ = 92°C/W To: Typical $R_{\theta JA}$ = 93°C/W ... 5
- Changed Figure 11 X-axis values ... 5

5 Specifications

5.1 Electrical Characteristics

T_A = 25°C (unless otherwise stated)

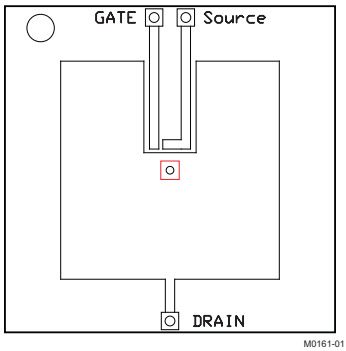
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-source voltage	V_{GS} = 0 V, I_D = 250 µA	25			V
I_{DSS}	Drain-to-source leakage current	V_{GS} = 0 V, V_{DS} = 20 V			1	µA
I_{GSS}	Gate-to-source leakage current	V_{DS} = 0 V, V_{GS} = +16 / –12 V			100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	1.7	2	2.3	V
$R_{DS(on)}$	Drain-to-source on resistance	V_{GS} = 4.5 V, I_D = 10 A		12	15	mΩ
		V_{GS} = 10 V, I_D = 10 A		8	10	
g_{fs}	Transconductance	V_{DS} = 15 V, I_D = 10 A		30		S
DYNAMIC CHARACTERISTICS						
C_{ISS}	Input capacitance	V_{GS} = 0 V, V_{DS} = 12.5 V, f = 1 MHz		440	570	pF
C_{OSS}	Output capacitance			330	430	pF
C_{RSS}	Reverse transfer capacitance			33	43	pF
R_g	Series gate resistance			0.8	1.6	Ω
Q_g	Gate charge total (4.5 V)	V_{DS} = 12.5 V, I_D = 10 A		2.9	3.8	nC
Q_{gd}	Gate charge gate-to-drain			0.7		nC
Q_{gs}	Gate charge gate-to-source			1.5		nC
Qg(th)	Gate charge at V_{th}			0.9		nC
Q_{OSS}	Output charge	V_{DS} = 12.5 V, V_{GS} = 0 V		6.5		nC
$t_{d(on)}$	Turnon delay time	V_{DS} = 12.5 V, V_{GS} = 4.5 V, I_D = 10 A R_G = 2 Ω		5.3		ns
t_r	Rise time			7.8		ns
$t_{d(off)}$	Turnoff delay time			6		ns
t_f	Fall time			3.1		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	I_S = 10 A, V_{GS} = 0 V		0.85	1	V
Q_{rr}	Reverse recovery charge	V_{DD} = 12.5 V, I_F = 10 A, di/dt = 300 A/µs		11.7		nC
t_{rr}	Reverse recovery time	V_{DD} = 12.5 V, I_F = 10 A, di/dt = 300 A/µs		15.5		ns

5.2 Thermal Information

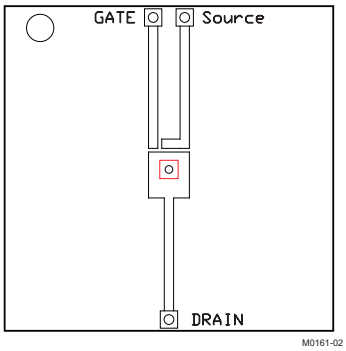
T_A = 25°C (unless otherwise stated)

PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-case thermal resistance(1)			3.5	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance(1) (2)			55	°C/W

(1) $R_{\theta JC}$ is determined with the device mounted on a 1-in^2 2-oz Cu pad on a 1.5-in × 1.5-in 0.06-in thick FR4 board. $R_{\theta JC}$ is specified by design while $R_{\theta JA}$ is determined by the user's board design.
(2) Device mounted on FR4 Material with 1-in^2 of 2-oz Cu.



Max $R_{\theta JA}$ = 55°C/W when mounted on 1-in^2 of 2-oz Cu.



Max $R_{\theta JA}$ = 160°C/W when mounted on minimum pad area of 2-oz Cu.

5.3 Typical MOSFET Characteristics

T_A = 25°C (unless otherwise stated)

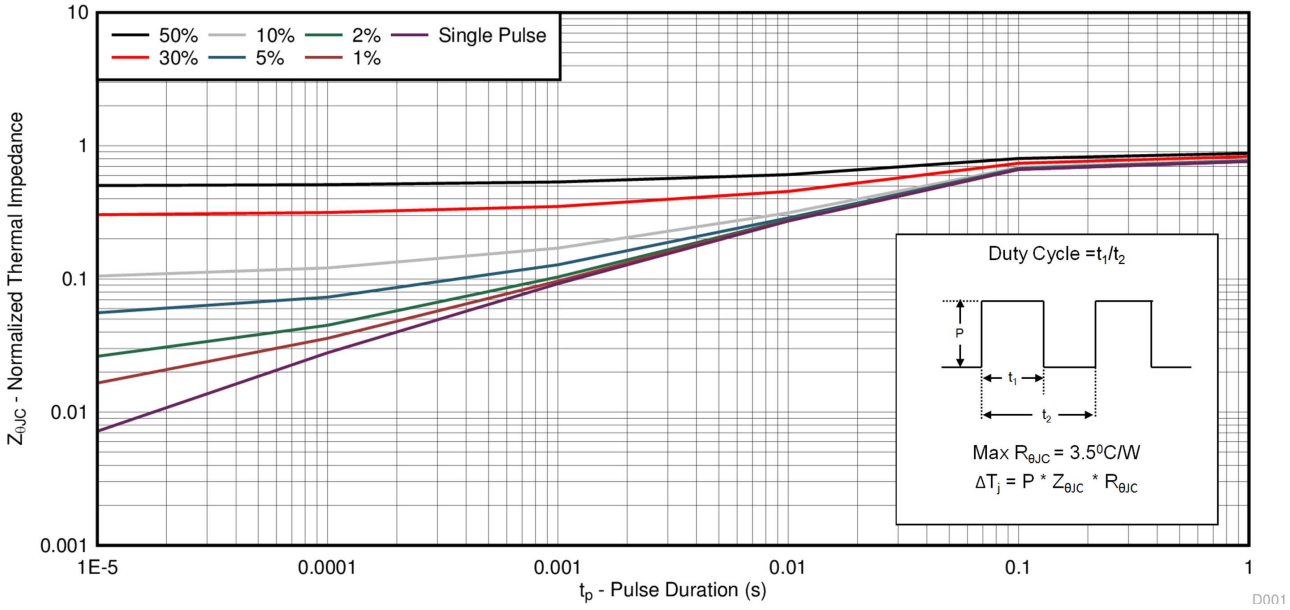


Figure 1. Transient Thermal Impedance

Typical MOSFET Characteristics (continued)

T_A = 25°C (unless otherwise stated)

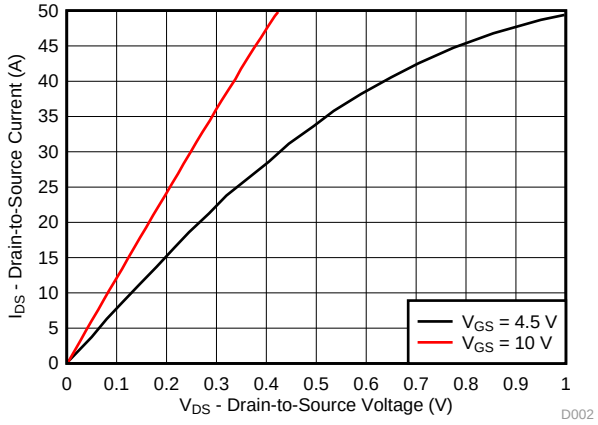
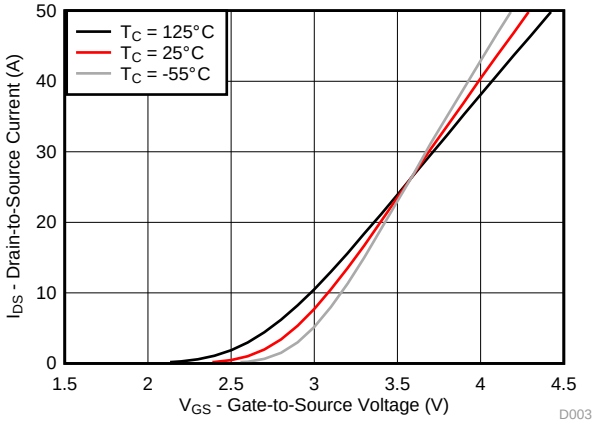
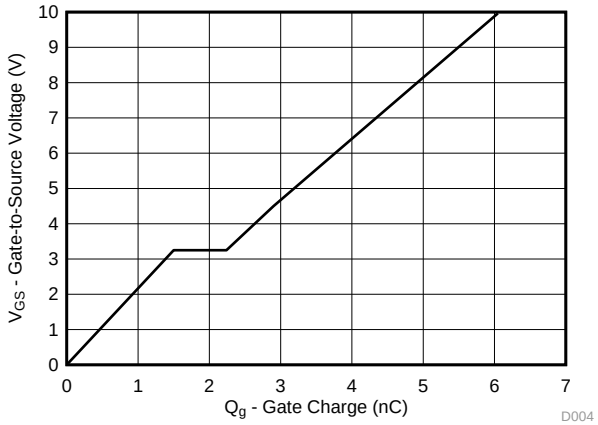


Figure 2. Saturation Characteristics



V_{DS} = 5 V

Figure 3. Transfer Characteristics



V_{DS} = 12.5 V, I_D = 10 A

Figure 4. Gate Charge

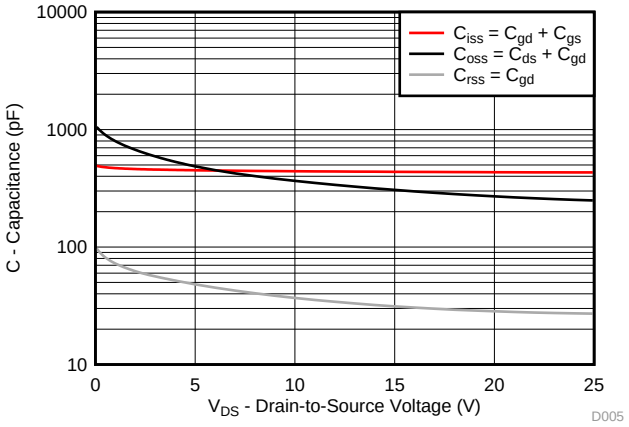
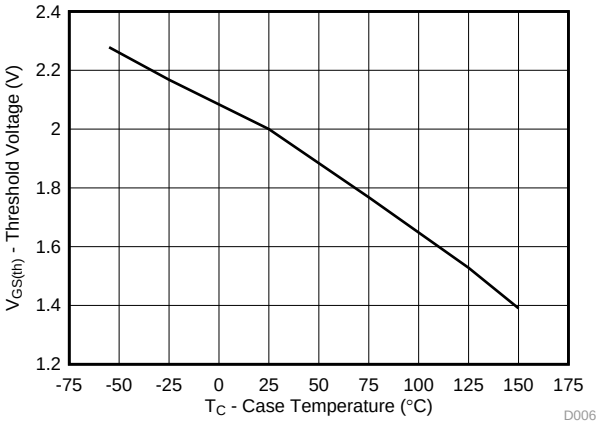


Figure 5. Capacitance



I_D = 250 µA

Figure 6. Threshold Voltage vs Temperature

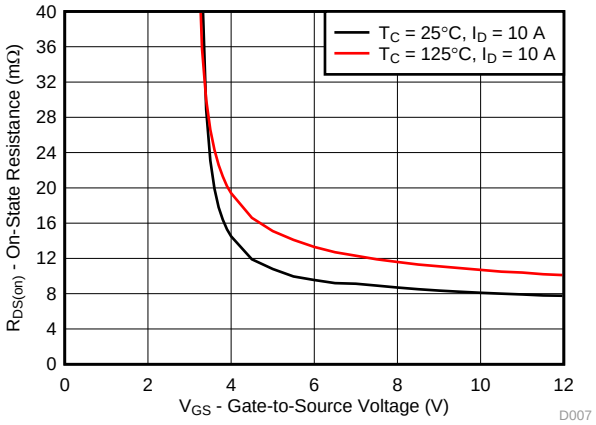
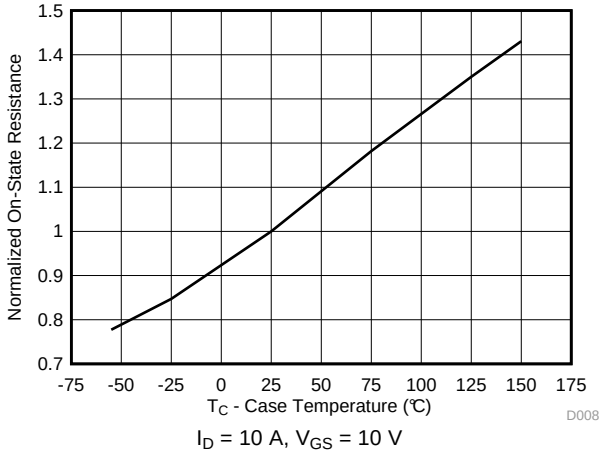


Figure 7. On Resistance vs Gate Voltage

Typical MOSFET Characteristics (continued)

T_A = 25°C (unless otherwise stated)



I_D = 10 A, V_{GS} = 10 V

Figure 8. On Resistance vs Temperature

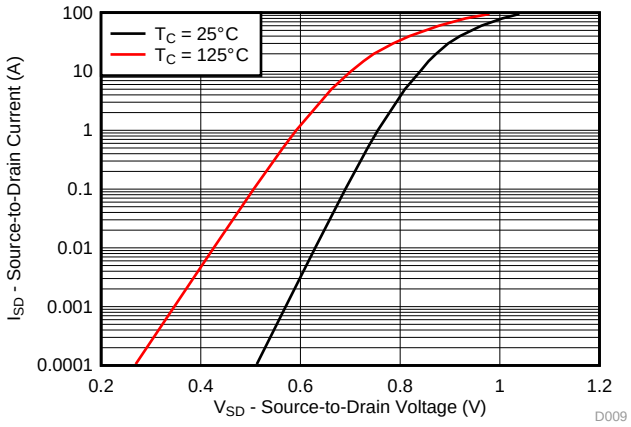
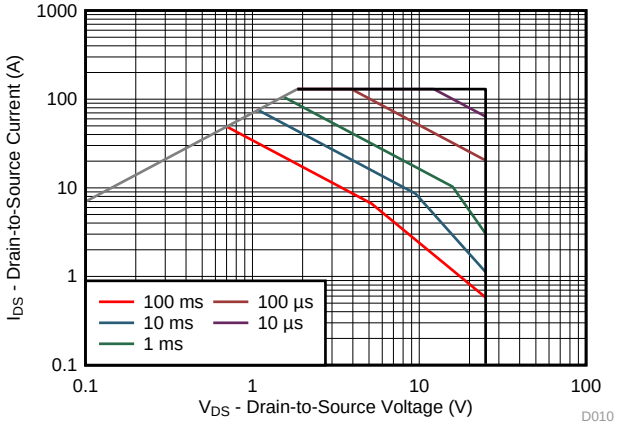


Figure 9. Typical Diode Forward Voltage



Single pulse, max $R_{\theta JC}$ = 3.5°C/W

Figure 10. Maximum Safe Operating Area

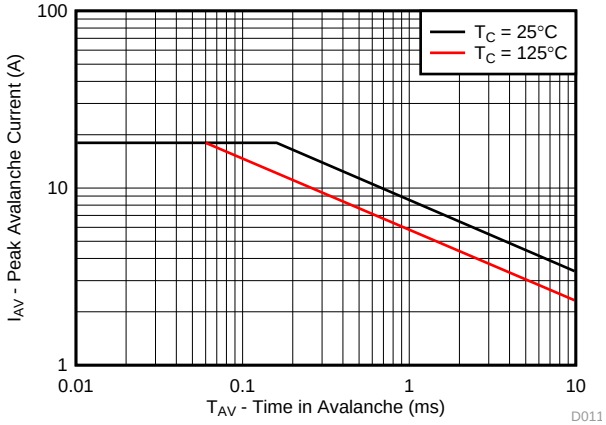


Figure 11. Single Pulse Unclamped Inductive Switching

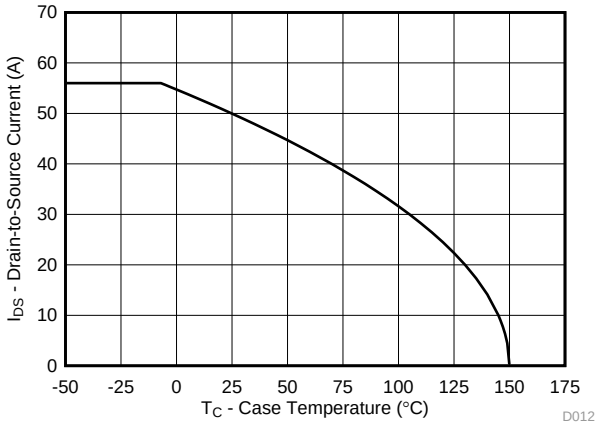


Figure 12. Maximum Drain Current vs Temperature

6 Device and Documentation Support

6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

6.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

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6.3 Trademarks

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6.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.5 Glossary

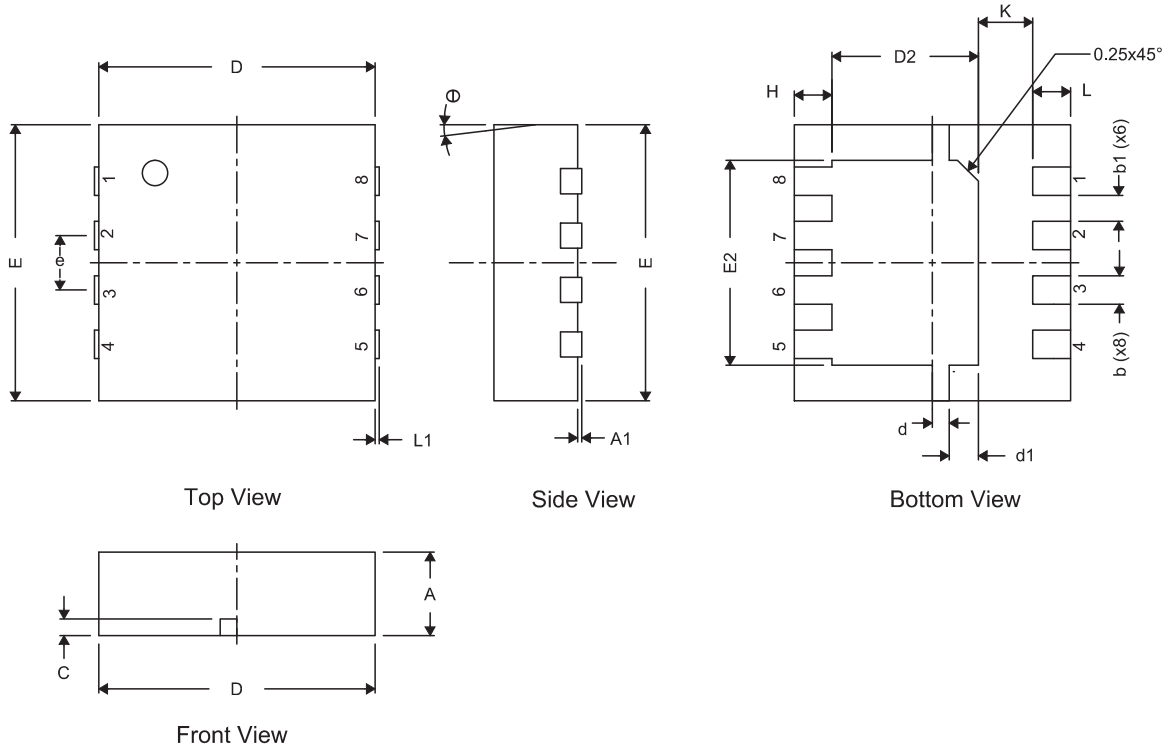
SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 Mechanical, Packaging, and Orderable Information

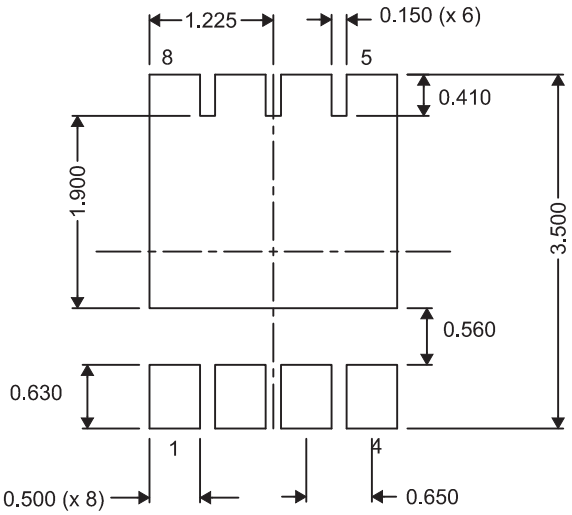
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 Q3 Package Dimensions



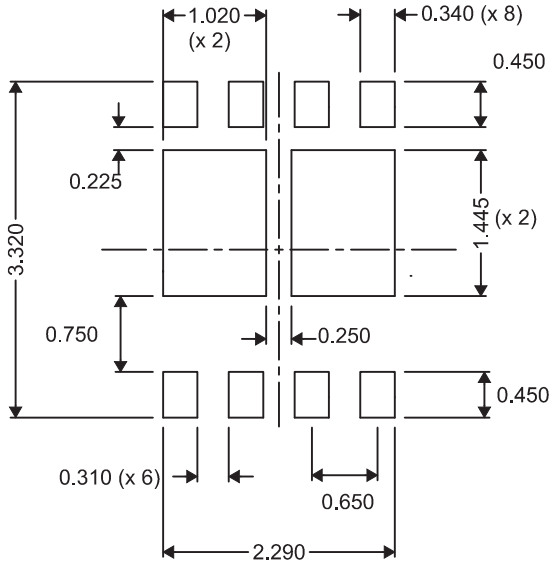
DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.950	1.000	1.100	0.037	0.039	0.043
A1	0.000	0.000	0.050	0.000	0.000	0.002
b	0.280	0.340	0.400	0.011	0.013	0.016
b1		0.310 NOM			0.012 NOM	
c	0.150	0.200	0.250	0.006	0.008	0.010
D	3.200	3.300	3.400	0.126	0.130	0.134
D2	1.650	1.750	1.800	0.065	0.069	0.071
d	0.150	0.200	0.250	0.006	0.008	0.010
d1	0.300	0.350	0.400	0.012	0.014	0.016
E	3.200	3.300	3.400	0.126	0.130	0.134
E2	2.350	2.450	2.550	0.093	0.096	0.100
e		0.650 TYP			0.026 TYP	
H	0.35	0.450	0.550	0.014	0.018	0.022
K		0.650 TYP			0.026 TYP	
L	0.35	0.450	0.550	0.014	0.018	0.022
L1	0	—	0	0	—	0
θ	0	—	0	0	—	0

7.2 Recommended PCB Pattern



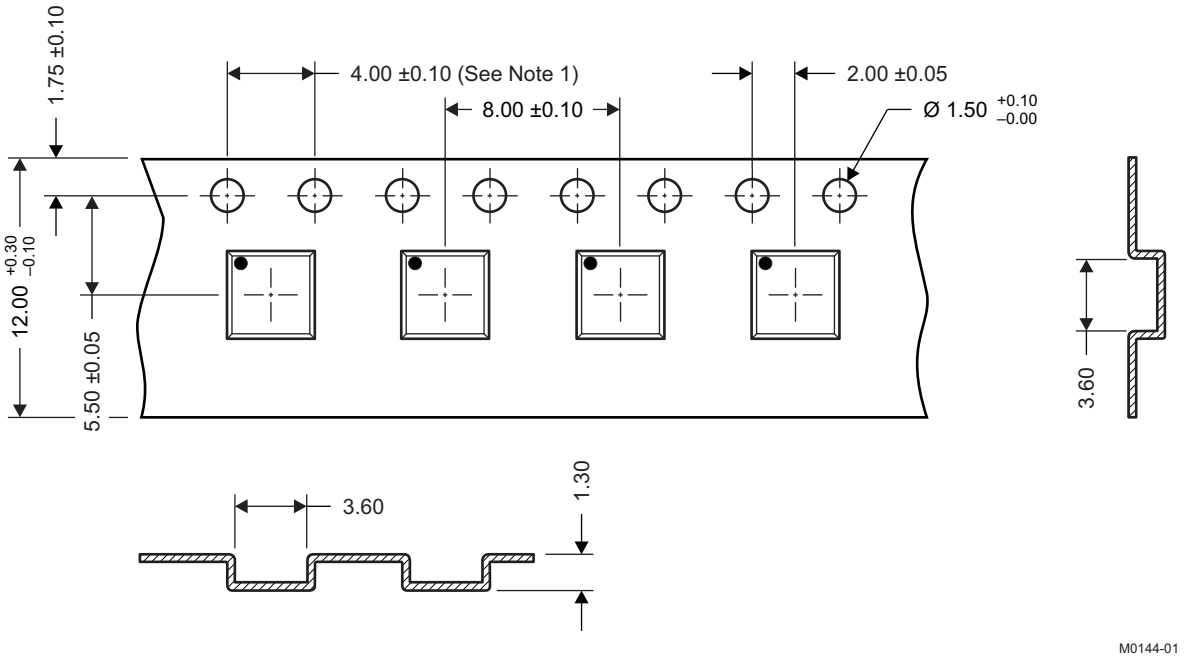
For recommended circuit layout for PCB designs, see *Reducing Ringing Through PCB Layout Techniques* (SLPA005).

7.3 Recommended Stencil Opening



All dimensions are in mm, unless otherwise specified.

7.4 Q3 Tape and Reel Information



Notes:

1. 10-sprocket hole pitch cumulative tolerance ±0.2.
2. Camber not to exceed 1 mm in 100 mm, noncumulative over 250 mm.
3. Material: black static dissipative polystyrene.
4. All dimensions are in mm (unless otherwise specified).
5. Thickness: 0.30 ±0.05 mm.
6. MSL1 260°C (IR and Convection) PbF-Reflow Compatible.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD16411Q3	ACTIVE	VSON-CLIP	DQG	8	2500	Pb-Free (RoHS Exempt)	CU SN	Level-1-260C-UNLIM	-55 to 150	CSD16411	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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