Zero-Drift, Rail-to-Rail I/O CMOS Operational Amplifiers

FEATURES

- **Low Offset Voltage: ±40uV (Max)**
- **Input Offset Drift: ±0.05uV/°C**
- **High Gain Bandwidth Product: 350KHz**
- **Rail-to-Rail Input and Output**
- **High Gain, CMRR, PSRR: 130dB**
- **High Slew Rate: 0.17V/us**
- **Low Noise: 1.6uVp-p (0.01~10Hz)**
- **Low Power Consumption: 60uA /op amp**
- **Overload Recovery Time:6us**
- **Low Supply Voltage: +2.3 V to +5.5 V**
- **No External Capacitors Required**
- **Extended Temperature: -40°C to +125°C**

APPLICATIONS

- **Temperature Sensors**
- **Medical/Industrial Instrumentation**
- **Pressure Sensors**
- **Battery-Powered Instrumentation**
- **Active Filtering**
- **Weight Scale Sensor**
- **Strain Gage Amplifiers**
- **Power Converter/Inverter**

DESCRIPTION

The RS8511, RS8512, RS8514, RS8513 (dual version &shutdown) series of CMOS operational amplifiers use auto-zero techniques to simultaneously provide very low offset voltage (40uV max) and near-zero drift over time and temperature. This family of amplifiers has ultralow noise, offset and power.

This miniature, high-precision operational amplifiers offset high input impedance and rail-to-rail input and rail-to-rail output swing. With high gain-bandwidth product of 350KHz and slew rate of 0.17V/us.

Single or dual supplies as low as +2.3V (±1.15V) and up to +5.5V (±2.75V) may be used.

The RS8511/ RS8512/ RS8514/ RS8513 (dual version with shutdown) are specified for the extended industrial and automotive temperature range (-40°C to 125°C). The RS8511 single amplifier is available in 5-lead SOT23, 8-lead MSOP8 and 8-lead SOIC packages, The RS8512 dual amplifier is available in 8-lead SOIC, 8-lead DFN2x2 and 8-lead TSSOP narrow surface mount packages, The RS8513(dual version with shutdown) comes in Micro-SIZE MSOP-10. The RS8514 quad is available in 14-lead SOIC and 14-lead narrow TSSOP packages.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE(NOM)
RS8511	SOT23-5	2.90mm×1.60mm
	SOIC-8(SOP8)	4.90mm×3.90mm
	MSOP-8	3.00mm×3.00mm
	SOT353(SC70-5)	2.10mm×1.25mm
RS8512	SOIC-8(SOP8)	4.90mm×3.90mm
	MSOP-8	3.00mm×3.00mm
	DFN2×2-8L	2.00mm×2.00mm
RS8513	MSOP-10	3.00mm×3.00mm
RS8514	SOIC-14(SOP14)	8.65mm×3.90mm
	TSSOP-14	5.00mm×4.40mm

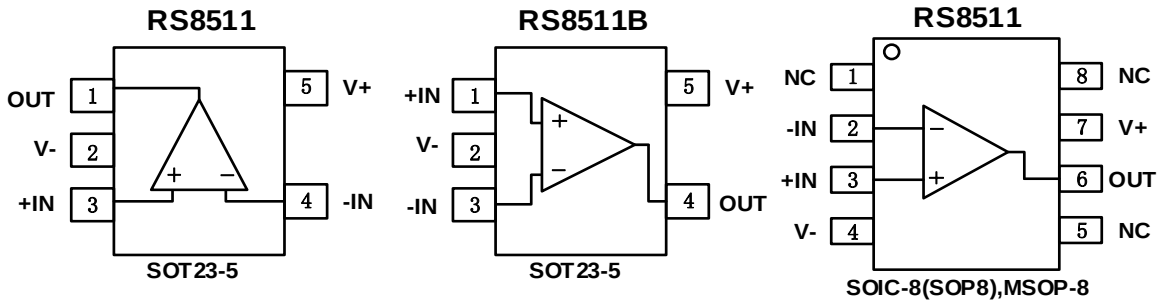
(1) For all available packages, see the orderable addendum at the end of the data sheet.

Revision History

Note: Page numbers for previous revisions may different from page numbers in the current version.

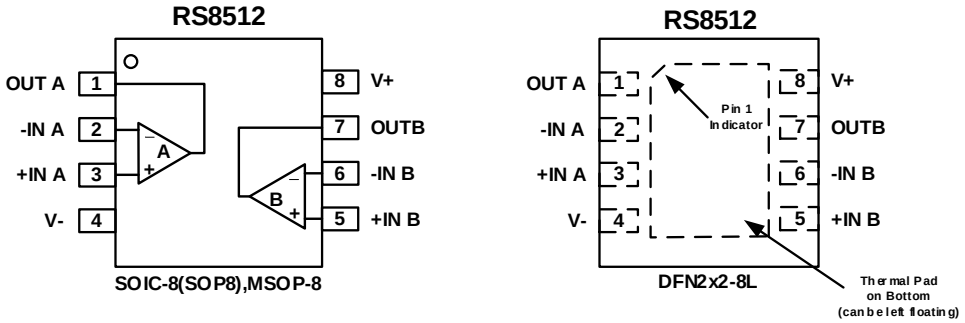
Version	Change Date	Change Item
C.1	2022/06/02	1. Update Package Qty on Page 3@RevB.7 2. Added TAPE AND REEL INFORMATION 3. Change Input Bias Current vs Temperature charts on Page 5@RevB.7

Pin Configuration and Functions (Top View)



Pin Description

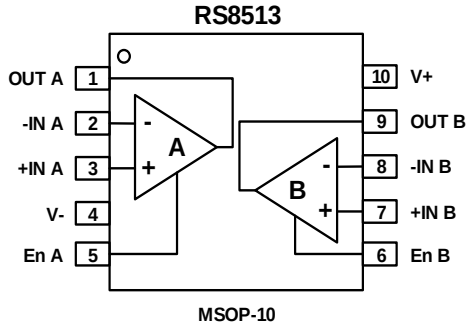
NAME	PIN			I/O	DESCRIPTION
	RS8511	RS8511B	RS8511		
	SOT23-5	SOT23-5	SOIC-8 (SOP8)/ MSOP8		
-IN	4	3	2	I	Negative (inverting) input
+IN	3	1	3	I	Positive (noninverting) input
NC	-	-	1,5,8	-	No internal connection (can be left floating)
OUT	1	4	6	O	Output
V-	2	2	4	-	Negative (lowest) power supply
V+	5	5	7	-	Positive (highest) power supply



Pin Description

NAME	PIN	I/O	DESCRIPTION
	SOIC-8 (SOP8)/ MSOP8/DFN2×2-8L		
-INA	2	I	Inverting input, channel A
+INA	3	I	Noninverting input, channel A
-INB	6	I	Inverting input, channel B
+INB	5	I	Noninverting input, channel B
OUTA	1	O	Output, channel A
OUTB	7	O	Output, channel B
V-	4	-	Negative (lowest) power supply
V+	8	-	Positive (highest) power supply

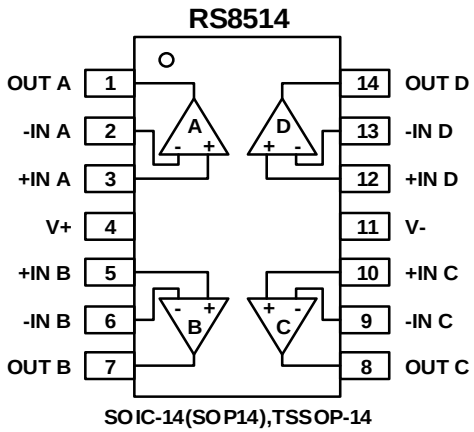
Pin Configuration and Functions (Top View)



Pin Description

NAME	PIN	I/O	DESCRIPTION
	MSOP-10		
-INA	2	I	Inverting input, channel A
+INA	3	I	Noninverting input, channel A
-INB	8	I	Inverting input, channel B
+INB	7	I	Noninverting input, channel B
EnA	5	I	Enable Input. A logic low reduces the supply current to 10nA. Connect to IN for normal operation，channel A
EnB	6	I	Enable Input. A logic low reduces the supply current to 10nA. Connect to IN for normal operation，channel B
OUTA	1	O	Output, channel A
OUTB	9	O	Output, channel B
V-	4	-	Negative (lowest) power supply
V+	10	-	Positive (highest) power supply

Pin Configuration and Functions (Top View)



Pin Description

NAME	PIN	I/O	DESCRIPTION
	SOIC-14 (SOP14)/ TSSOP-14		
-INA	2	I	Inverting input, channel A
+INA	3	I	Noninverting input, channel A
-INB	6	I	Inverting input, channel B
+INB	5	I	Noninverting input, channel B
-INC	9	I	Inverting input, channel C
+INC	10	I	Noninverting input, channel C
-IND	13	I	Inverting input, channel D
+IND	12	I	Noninverting input, channel D
OUTA	1	O	Output, channel A
OUTB	7	O	Output, channel B
OUTC	8	O	Output, channel C
OUTD	14	O	Output, channel D
V-	11	-	Negative (lowest) power supply
V+	4	-	Positive (highest) power supply

SPECIFICATIONS

Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Voltage	Supply, Vs=(V+) - (V-)		7	V
	Signal input pin (2)	(V-) -0.5	(V+) +0.5	
	Signal output pin (3)	(V-) -0.5	(V+) +0.5	
Current	Signal input pin (2)	-10	10	mA
	Signal output pin (3)	-55	55	mA
	Output short-circuit (4)	Continuous		
Temperature	Operating range, T_A	-40	125	°C
	Junction, T_J	-40	150	
	Storage, T_{stg}	-65	150	

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current-limited to 10mA or less.
(3) Output terminals are diode-clamped to the power-supply rails. Output signals that can swing more than 0.5V beyond the supply rails should be current-limited to ±55mA or less.
(4) Short-circuit to ground, one amplifier per package.

ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM)	±5000	V
		Machine Model (MM)	±400	

Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage，Vs= (V+) - (V-)	Single-supply	2.3		5.5	V
	Dual-supply	±1.15		±2.75	

Thermal Information: RS8511

THERMAL METRIC		RS8511			UNIT
		5PINS	8PINS		
		SOT23-5	SOIC-8	MSOP-8	
$R_{\Theta JA}$	Junction-to-ambient thermal resistance	273.8	116	165	°C/W
$R_{\Theta JC\ (top)}$	Junction-to-case (top) thermal resistance	126.8	60	53	°C/W
$R_{\Theta JB}$	Junction-to-board thermal resistance	85.9	56	87	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	10.9	12.8	4.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	84.9	98.3	85	°C/W
$R_{\Theta JC\ (bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

Thermal Information: RS8512

THERMAL METRIC		RS8512			UNIT
		8PINS			
		SOIC-8	MSOP-8	DFN2×2-8L	
$R_{\Theta JA}$	Junction-to-ambient thermal resistance	116	165	80.1	°C/W
$R_{\Theta JC\ (top)}$	Junction-to-case (top) thermal resistance	60	53	100	°C/W
$R_{\Theta JB}$	Junction-to-board thermal resistance	56	87	45	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	12.8	4.9	6.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	98.3	85	45.2	°C/W
$R_{\Theta JC\ (bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	22.7	°C/W

Thermal Information: RS8513

THERMAL METRIC		RS8513	UNIT
		10PINS	
		MSOP-10	
$R_{\Theta JA}$	Junction-to-ambient thermal resistance	169.5	°C/W
$R_{\Theta JC\ (top)}$	Junction-to-case (top) thermal resistance	84.1	°C/W
$R_{\Theta JB}$	Junction-to-board thermal resistance	113	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	15.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	111.6	°C/W
$R_{\Theta JC\ (bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

Thermal Information: RS8514

THERMAL METRIC		RS8514		UNIT
		14PINS		
		SOIC-14	TSSOP-14	
$R_{\Theta JA}$	Junction-to-ambient thermal resistance	83.8	120.8	°C/W
$R_{\Theta JC\ (top)}$	Junction-to-case (top) thermal resistance	70.7	34.3	°C/W
$R_{\Theta JB}$	Junction-to-board thermal resistance	59.5	62.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	11.6	1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	37.7	56.5	°C/W
$R_{\Theta JC\ (bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

PACKAGE/ORDERING INFORMATION

Orderable Device	Package Type	Pin	Channel	Op Temp(°C)	Device Marking(1)	Package Qty
RS8511XF	SOT23-5	5	1	-40°C ~125°C	8511	Tape and Reel,3000
RS8511BXF	SOT23-5	5	1	-40°C ~125°C	8511B	Tape and Reel,3000
RS8511XK	SOIC-8 (SOP8)	8	1	-40°C ~125°C	RS8511	Tape and Reel,4000
RS8511XM	MSOP-8	8	1	-40°C ~125°C	RS8511	Tape and Reel,4000
RS8512XK	SOIC-8 (SOP8)	8	2	-40°C ~125°C	RS8512	Tape and Reel,4000
RS8512XM	MSOP-8	8	2	-40°C ~125°C	RS8512	Tape and Reel,4000
RS8512XTDE8	DFN2x2-8L	8	2	-40°C ~125°C	8512	Tape and Reel,3000
RS8513XN	MSOP-10	10	2	-40°C ~125°C	RS8513	Tape and Reel,4000
RS8514XP	SOIC-14 (SOP14)	14	4	-40°C ~125°C	RS8514	Tape and Reel,4000
RS8514XQ	TSSOP-14	14	4	-40°C ~125°C	RS8514	Tape and Reel,4000

NOTE:

(1) There may be additional marking, which relates to the lot trace code information (data code and vendor code), the logo or the environmental category on the device.

ELECTRICAL CHARACTERISTICS

Boldface limits apply over the specified temperature range, T_A = -40°C to +125°C.
(At T_A = +25°C, Vs=5V, R_L = 10kΩ connected to V_S/2, and V_{OUT} = V_S/2, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITION	RS8511, RS8512, RS8513, RS8514			
			MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
Input Offset Voltage	V_{OS}	V_{CM}= V_S/2	-40	±7	40	uV
Input Offset Voltage Average Drift	Vos Tc			±0.05	±0.2	uV/°C
Power-Supply Rejection Ratio	PSRR	V_S= +2.3V to +5.5V, V_{CM}= 0	110	130		dB
Channel Separation, dc				0.1		uV/V
INPUT BIAS CURRENT						
Input Bias Current	IB	V_{CM} = V_S/2		±50		pA
Input Offset Current	I_{OS}			±10		pA
NOISE PERFORMANCE						
Input Voltage Noise	e_np-p	f= 0.01Hz to 10Hz		1.6		uVpp
Input Voltage Noise	e_np-p	f= 0.01Hz to 1Hz		0.48		uVpp
Input Voltage Noise Density	e_n	f= 1KHz		70		nV/$\sqrt{\text{Hz}}$
Input Current Noise Density	i_n	f= 10Hz		8		fA/$\sqrt{\text{Hz}}$
INPUT VOLTAGE RANGE						
Common-Mode Voltage Range	V_{CM}		(V-) -0.1		(V+) +0.1	V
Common-Mode Rejection Ratio	CMRR	(V-) -0.1V < V_{CM} < (V+)+ 0.1V	110	130		dB
INPUT CAPACITANCE						
Differential				1		pF
Common-Mode				5		pF
Open-Loop Gain						
Open-Loop Voltage Gain	A_{OL}	R_L= 10KΩ, V_O= 0.3V to 4.7V, T_A= -40°C to 125°C	110	130		dB
DYNAMIC PERFORMANCE						
Slew Rate	SR	G= +1		0.17		V/us
Gain-Bandwidth Product	GBW			350		KHz
Overload Recovery Time	t_{OR}			6		us
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L=100 KΩ to GND	4.99	4.998		V
		R_L=10 KΩ to GND	4.95	4.98		
Output Voltage Low	V_{OL}	R_L=100 KΩ to V+		1	10	mV
		R_L=10 KΩ to V+		10	30	
Short-Circuit Current	I_{SC}			25		mA
POWER SUPPLY						
Operating Voltage Range	V_S		2.3		5.5	V
Quiescent Current/ Amplifier	IQ			60	87	uA
SHUTDOWN						
t_{OFF}				2		us
t_{ON}				1		ms

V_L (shutdown)			0		+0.8	V
V_H (amplifier is active)			0.75 (V+)		V+	V
Input Bias Current of Enable Pin				50		pA
I_{QSD}				1	5	uA

TYPICAL CHARACTERISTICS

At T_A = +25°C, Vs=5V, R_L = 10kΩ connected to $V_S/2$, V_{OUT} = $V_S/2$, unless otherwise noted.

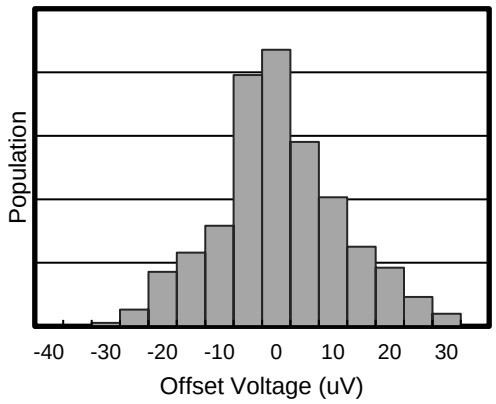


Figure 1. Offset Voltage Production Distribution

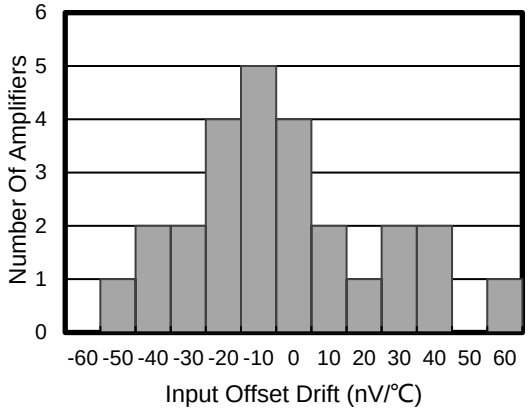


Figure 2. Offset Voltage Drift Production Distribution

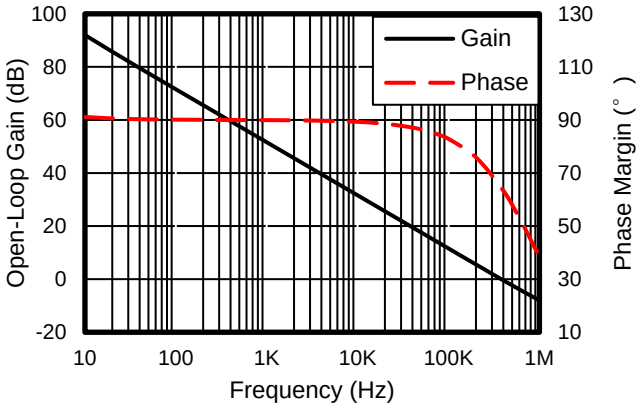


Figure 3. Open-Loop Gain and Phase vs Frequency

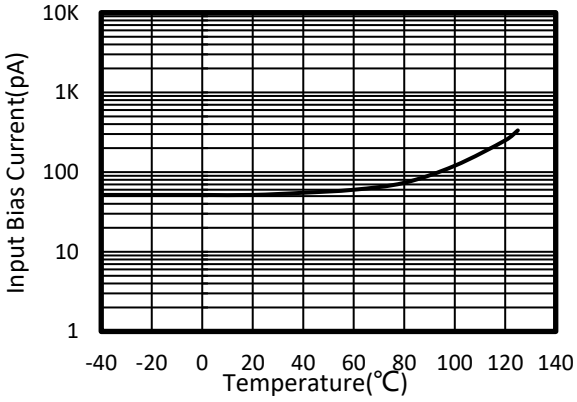


Figure 4. Input Bias Current vs Temperature

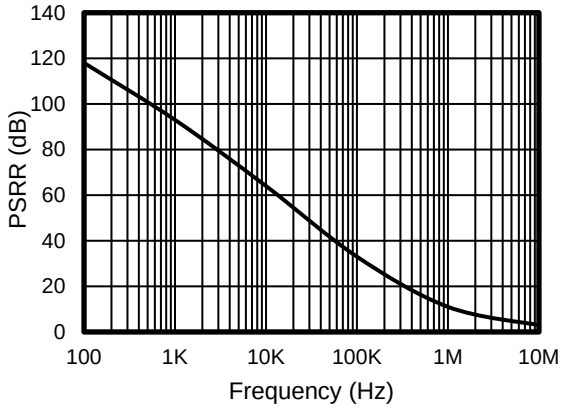


Figure 5. Power-Supply Rejection Ratio vs Frequency

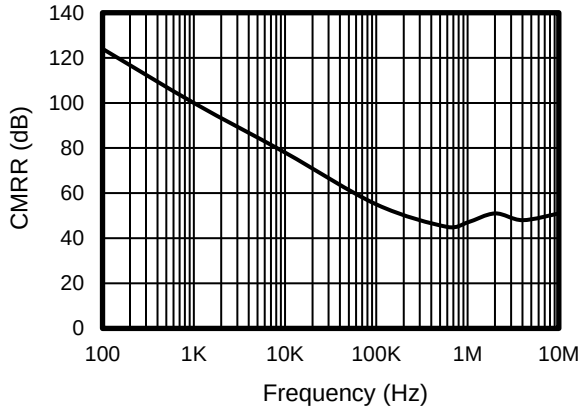


Figure 6. Common-Mode Rejection Ratio vs Frequency

TYPICAL CHARACTERISTICS

At T_A = +25°C, Vs=5V, R_L = 10kΩ connected to V_S/2, V_{OUT} = V_S/2, unless otherwise noted.

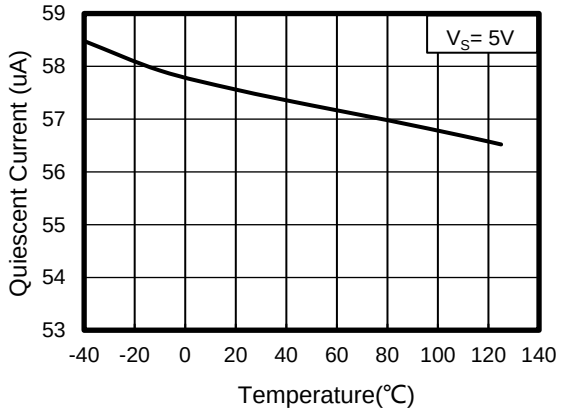


Figure 7. Quiescent Current vs Temperature

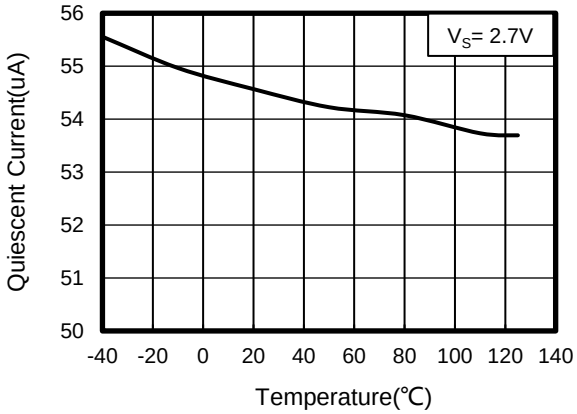


Figure 8. Quiescent Current vs Temperature

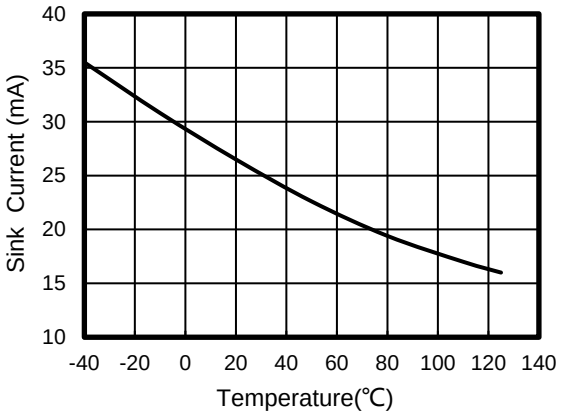


Figure 9. Sink Current vs Temperature

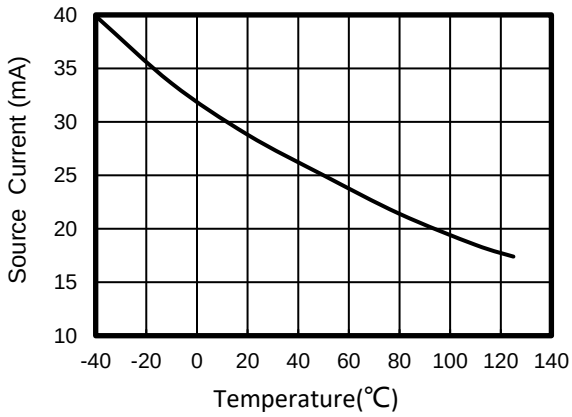


Figure 10. Source Current vs Temperature

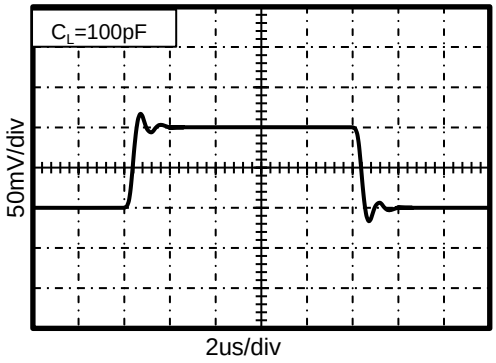


Figure 11. Small-Signal Step Response

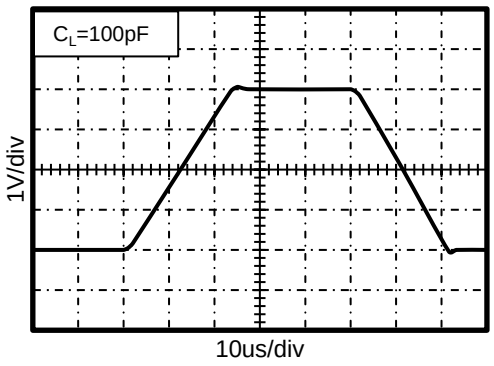


Figure 12. Large-Signal Step Response

TYPICAL CHARACTERISTICS

At T_A = +25°C, Vs=5V, R_L = 10kΩ connected to $V_S/2$, V_{OUT} = $V_S/2$, unless otherwise noted.

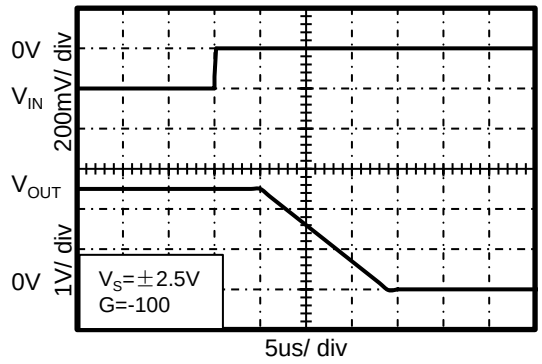


Figure 13. Positive Overvoltage Recovery

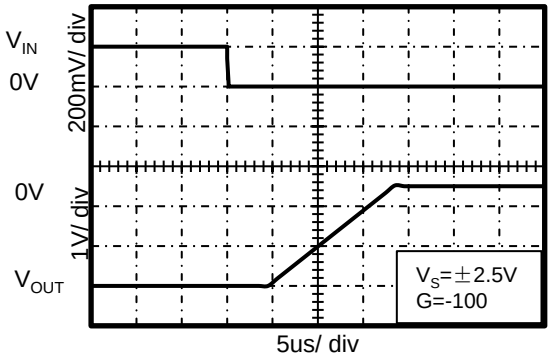


Figure 14. Negative Overvoltage Recovery

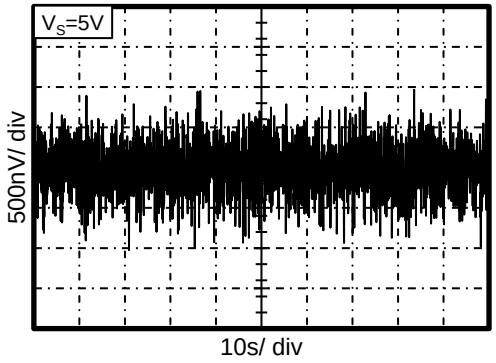


Figure 15. 0.01Hz to 10Hz Noise

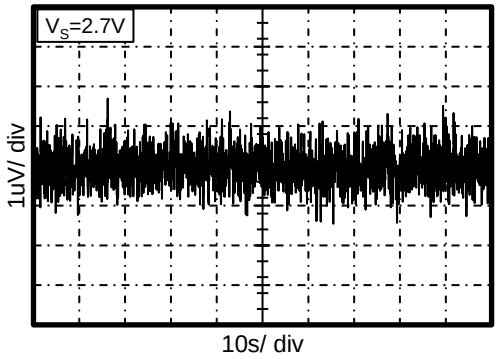


Figure 16. 0.01Hz to 10Hz Noise

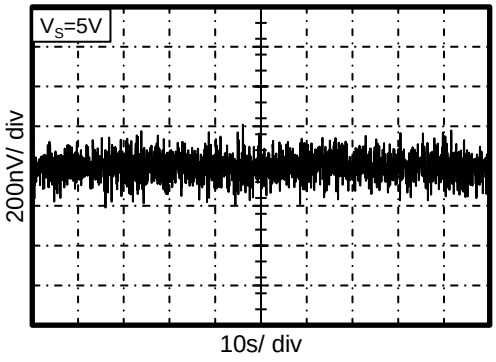


Figure 17. 0.01Hz to 1Hz Noise

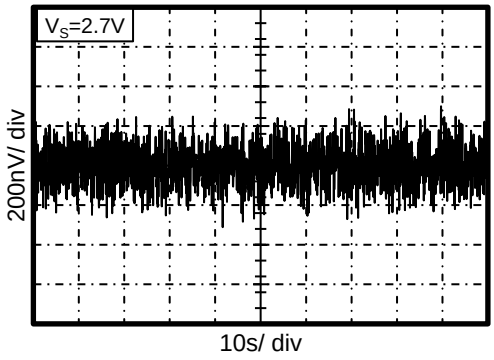


Figure 18. 0.01Hz to 1Hz Noise

Detailed Description

Overview

The RS8511, RS8512, RS8513, RS8514 series op amps are unity-gain stable and free from unexpected output phase reversal. They use auto-zeroing techniques to provide low offset voltage and very low drift over time and temperature.

Good layout practice mandates use of a 0.1uF capacitor placed closely across the supply pins. For lowest offset voltage and precision performance, circuit layout and mechanical conditions should be optimized. Avoid temperature gradients that create thermoelectric (Seebeck) effects in thermocouple junctions formed from connecting dissimilar conductors. These thermally-generated potentials can be made to cancel by assuring that they are equal on both input terminals.

- Use low thermoelectric-coefficient connections (avoid dissimilar metals).
- Thermally isolate components from power supplies or other heat-sources.
- Shield op amp and input circuitry from air currents, such as cooling fans.

Following these guidelines will reduce the likelihood of junctions being at different temperatures, which can cause thermoelectric voltages of 0.1uV/°C or higher, depending on materials used.

OPERATING VOLTAGE

The RS8511, RS8512, RS8513, RS8514 series op amps operate over a power-supply range of +2.3V to +5.5V (±1.15V to ±2.75V). Supply voltages higher than 7V (absolute maximum) can permanently damage the amplifier. Parameters that vary over supply voltage or temperature are shown in the Typical Characteristics section of this data sheet.

RS8513 ENABLE FUNCTION

The enable/shutdown digital input is referenced to the V- supply voltage of the amp. A logic high enables the op amp. A valid logic high is defined as > 75% of the total supply voltage. The valid logic high signal can be up to 5.5V above the negative supply, independent of the positive supply voltage. A valid logic low is defined as < 0.8V above the V– supply pin. If dual or split power supplies are used, be sure that logic input signals are properly referred to the negative supply voltage. The enable pin must be connected to a valid high or low voltage, or driven, not left open circuit.

The logic input is a high-impedance CMOS input, with separate logic inputs provided on the dual version. For battery operated applications, this feature can be used to greatly reduce the average current and extend battery life.

The enable time includes one full autozero cycle required by the amplifier to return to V_{OS} accuracy. Prior to this time, the amplifier functions properly, but with unspecified offset voltage.

Disable time is 1us. When disabled, the output assumes a high-impedance state. This allows the RS8513 to be operated as a gated amplifier, or to have the output multiplexed onto a common analog output bus.

LAYOUT

Layout Guidelines

Attention to good layout practices is always recommended. Keep traces short. When possible, use a PCB ground plane with surface-mount components placed as close to the device pins as possible. Place a 0.1uF capacitor closely across the supply pins.

These guidelines should be applied throughout the analog circuit to improve and provide benefits such as reducing the EMI susceptibility.

Layout Example

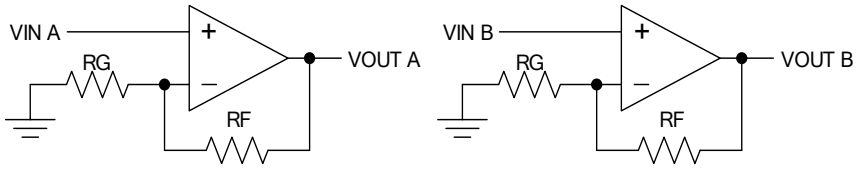


Figure 19. Schematic Representation

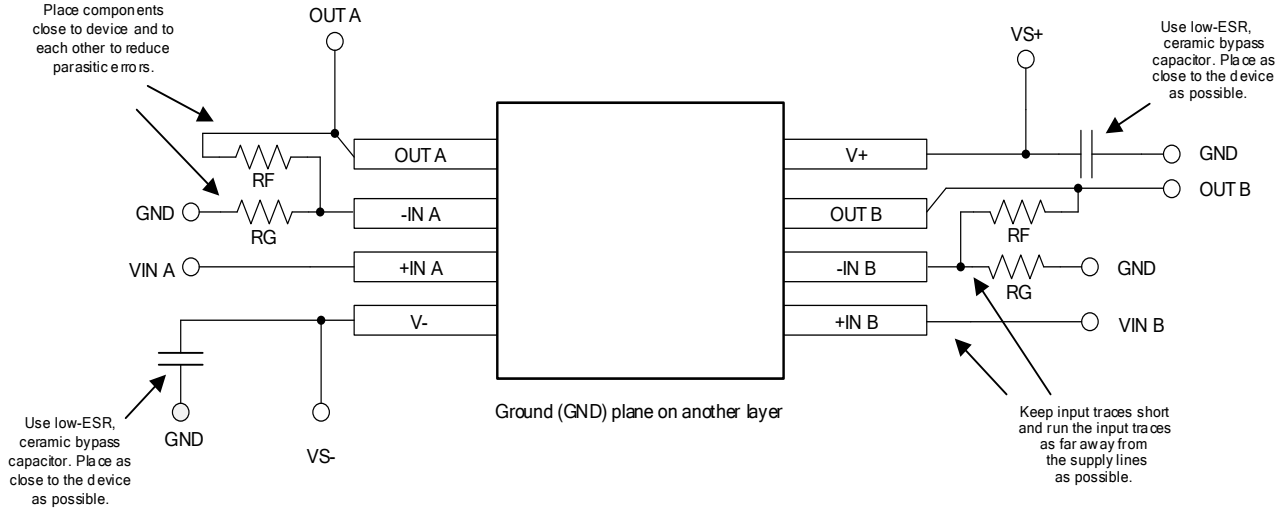
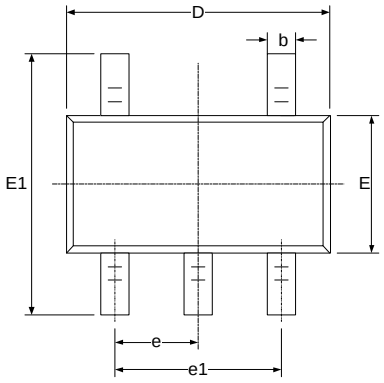
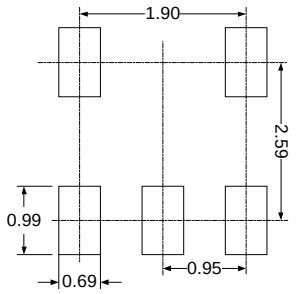


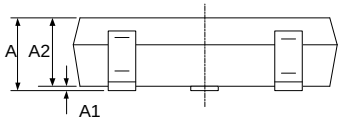
Figure 20. Layout Example

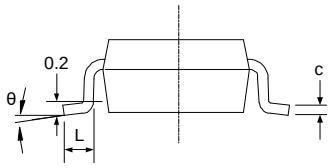
PACKAGE OUTLINE DIMENSIONS
SOT23-5





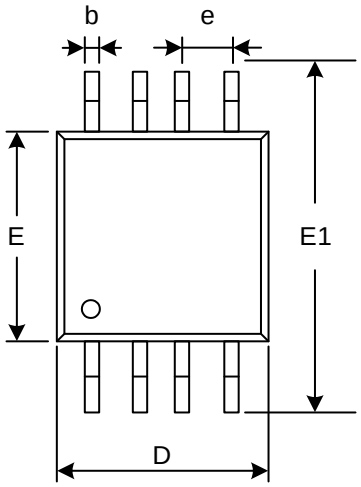
RECOMMENDED LAND PATTERN (Unit: mm)

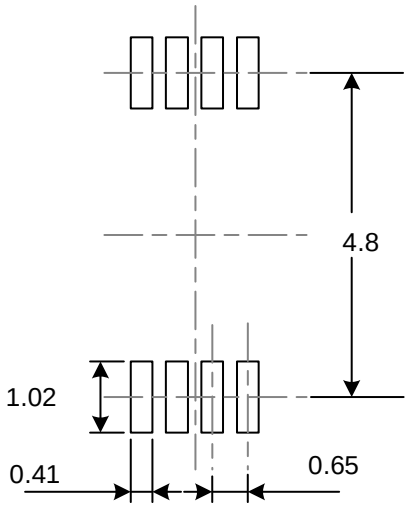




Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

MSOP-8





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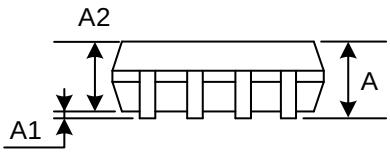
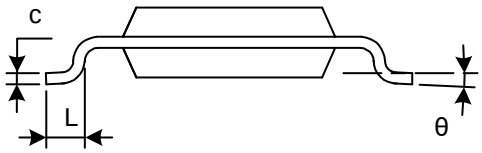
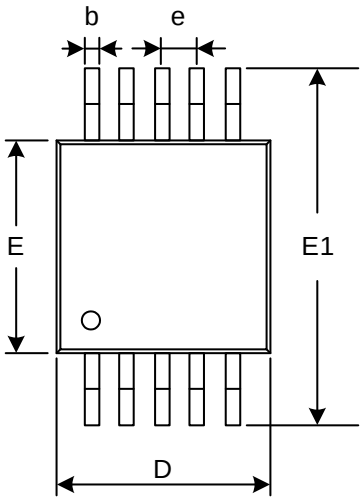
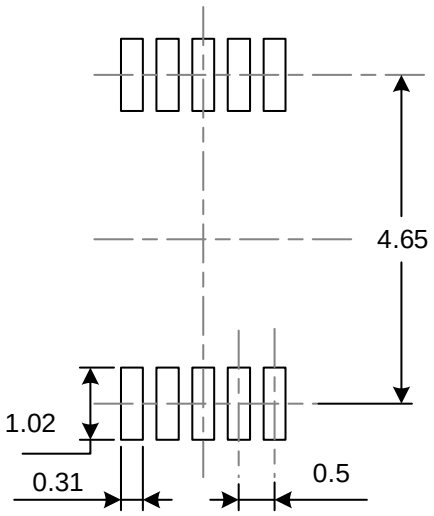




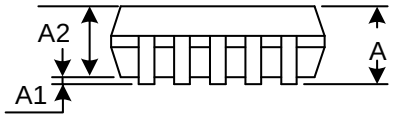
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.820	1.100	0.032	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.250	0.380	0.010	0.015
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
e	0.650(BSC)		0.026(BSC)	
E	2.900	3.100	0.114	0.122
E1	4.750	5.050	0.187	0.199
L	0.400	0.800	0.016	0.031
θ	0°	6°	0°	6°

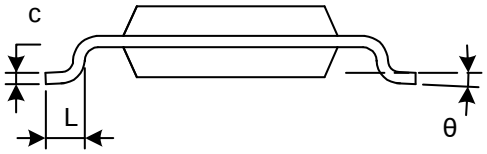
MSOP-10





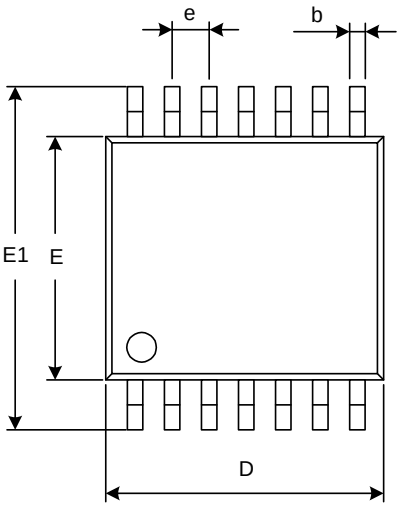
RECOMMENDED LAND PATTERN (Unit: mm)

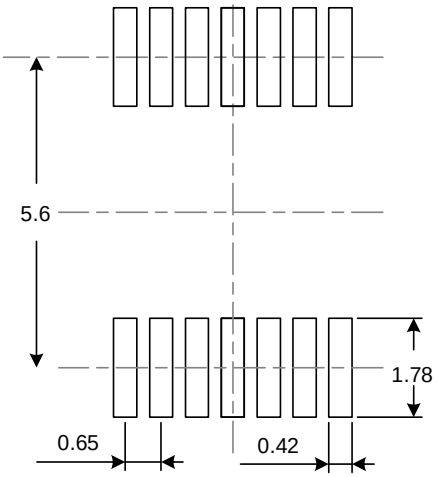




Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.820	1.100	0.032	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.180	0.280	0.007	0.011
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
e	0.50(BSC)		0.020(BSC)	
E	2.900	3.100	0.114	0.122
E1	4.750	5.050	0.187	0.199
L	0.400	0.800	0.016	0.031
θ	0°	6°	0°	6°

TSSOP-14





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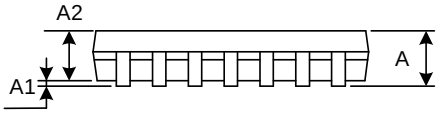
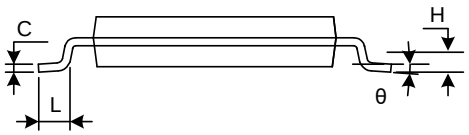
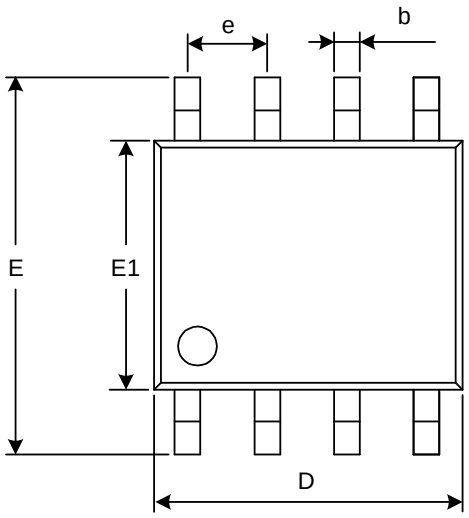
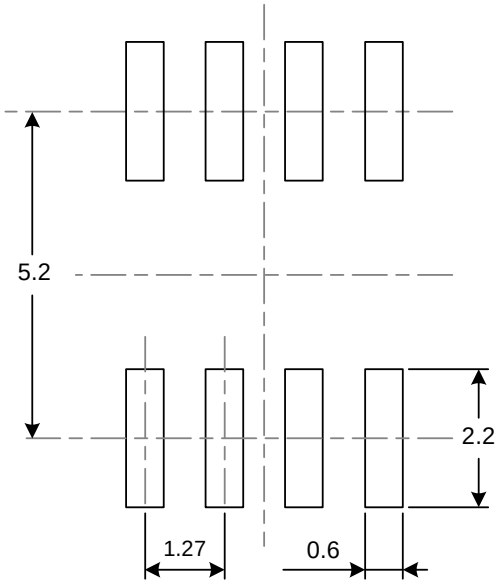




Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A		1.200		0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.050	0.031	0.041
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	4.860	5.100	0.191	0.201
E	4.300	4.500	0.169	0.177
E1	6.250	6.550	0.246	0.258
e	0.650(BSC)		0.026(BSC)	
L	0.500	0.700	0.020	0.028
H	0.25(TYP)		0.01(TYP)	
θ	1°	7°	1°	7°

SOIC-8 (SOP8)





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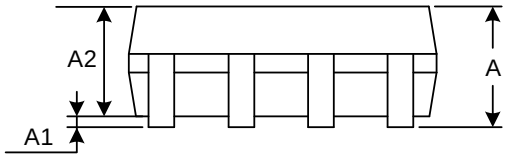
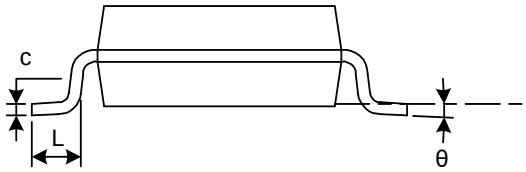
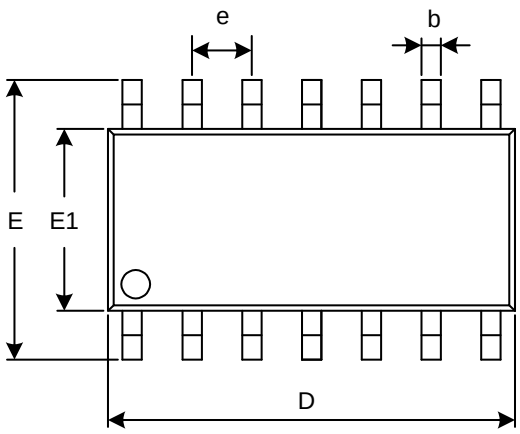
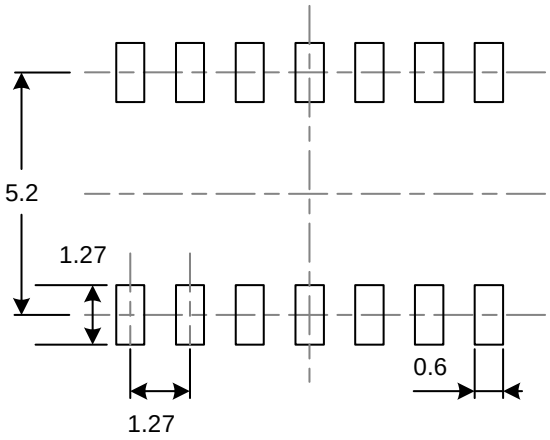




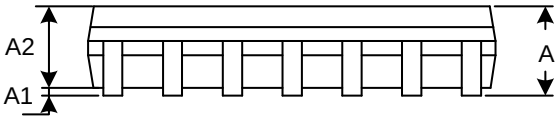
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.800	5.000	0.189	0.197
e	1.270(BSC)		0.050(BSC)	
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

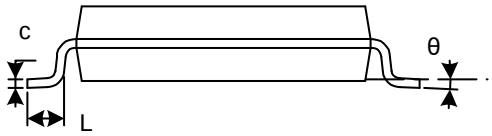
SOIC-14 (SOP14)





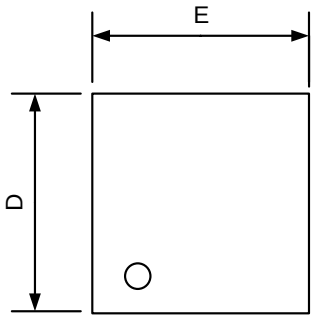
RECOMMENDED LAND PATTERN (Unit: mm)



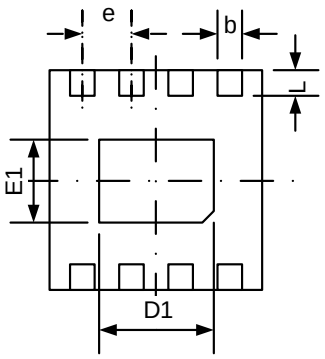


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.310	0.510	0.012	0.020
c	0.100	0.250	0.004	0.010
D	8.450	8.850	0.333	0.348
e	1.270(BSC)		0.050(BSC)	
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

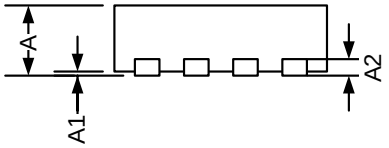
DFN2x2-8L



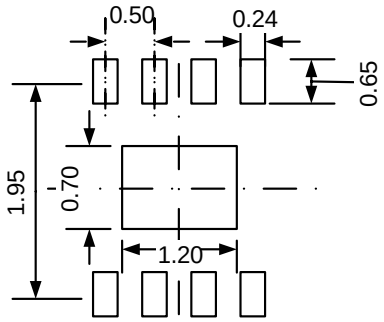
TOP VIEW



BOTTOM VIEW



SIDE VIEW



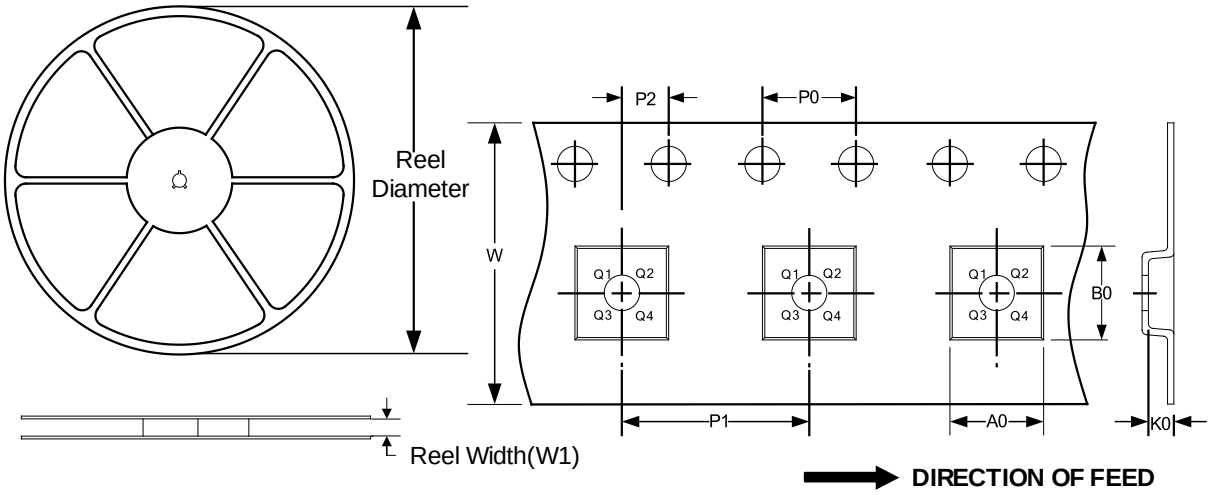
RECOMMENDED LAND PATTERN
(Unit: mm)

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.203(TYP)		0.008(TYP)	
b	0.180	0.300	0.007	0.012
D	1.900	2.100	0.075	0.083
D1	1.100	1.300	0.043	0.051
E	1.900	2.100	0.075	0.083
E1	0.600	0.800	0.024	0.031
e	0.500(TYP)		0.020(TYP)	
L	0.250	0.450	0.010	0.018

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSION



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOT23-5	7''	9.5	3.20	3.20	1.40	4.0	4.0	2.0	8.0	Q3
MSOP8	13''	12.4	5.20	3.30	1.50	4.0	8.0	2.0	12.0	Q1
TSSOP14	13''	12.4	6.95	5.60	1.20	4.0	8.0	2.0	12.0	Q1
SOIC-8 (SOP8)	13''	12.4	6.40	5.40	2.10	4.0	8.0	2.0	12.0	Q1
SOIC-14 (SOP14)	13''	16.4	6.60	9.30	2.10	4.0	8.0	2.0	16.0	Q1
MSOP-10	13''	12.4	5.20	3.30	1.20	4.0	8.0	2.0	12.0	Q1
DFN2x2-8L	7''	9.5	2.30	2.30	1.10	4.0	4.0	2.0	8.0	Q2