Power Supply IC Series for TFT-LCD Panels

Multi-channel System Power Supply IC + Gamma Buffer

BD8162AEKV

General Description

The BD8162AEKV is a system power supply IC that provides control 6 power supply channels and 4 gamma output channels + VCOM required for TFT-LCD panels on a single chip. All channels have built-in control input and Power-Good output functions, enabling free sequence control setting just by changing channels. In addition, the BD8162AEKV is a user-friendly IC incorporating input switch, short-circuit protection, and protection detection output circuits.

Features

- Step-up DC/DC Converter with Built-in 3A FET
- Step-down DC/DC Converter with Built-in 2A FET
- Synchronous Rectification Step-down DC/DC Converter with Built-in 2A FET
- 3ch LDO Regulator (500mA, 200mA, 20mA)
- Positive/Negative Charge Pumps
- 4ch Gamma Buffer Amplifier + VCOM
- Protection Circuits:
  - Under-Voltage Lockout Protection Circuit
  - Thermal Shutdown Circuit
  - Timer Latch Type Short-Circuit Protection Circuit
- Controllable Startup Sequence

Applications

LCD TV power supplies

Key Specifications

- Power Supply Voltage 1 Range: 4.2V to 14V
- Oscillating Frequency: 200kHz to 800kHz(Variable)
- Operating Temperature Range: -40°C to +105°C

Package W(Typ) x D(Typ) x H(Max)

HTQFP64V
12.00mm x 12.00mm x 1.00mm

Typical Application Circuit (1)

1. Application used to input V_{CC}12V:

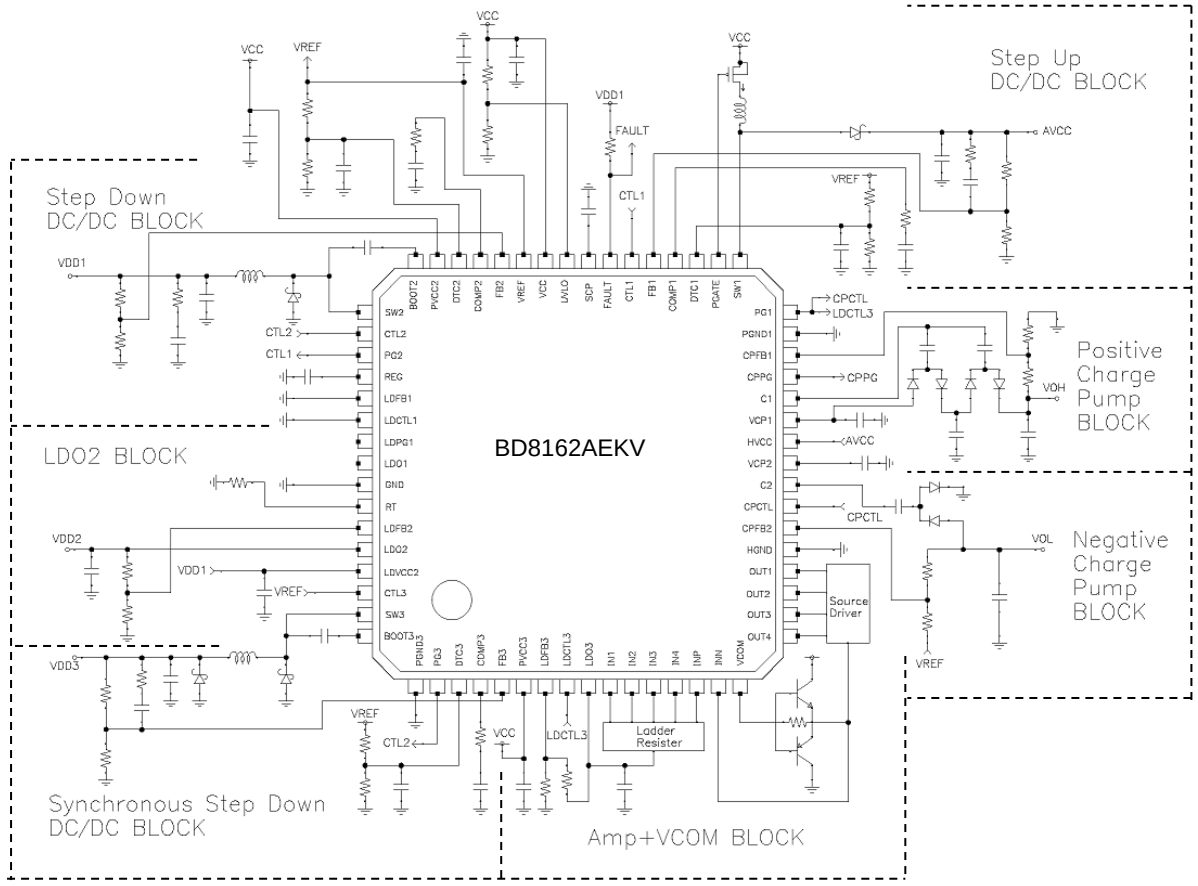
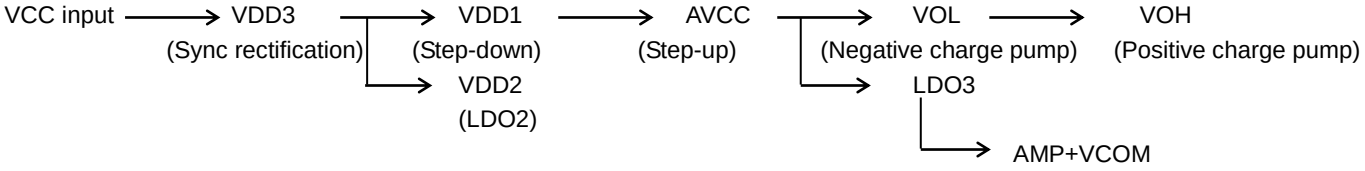


Figure 1. Typical 12V Input Application Diagram

2. Startup Sequence



3. Sequence Image Chart

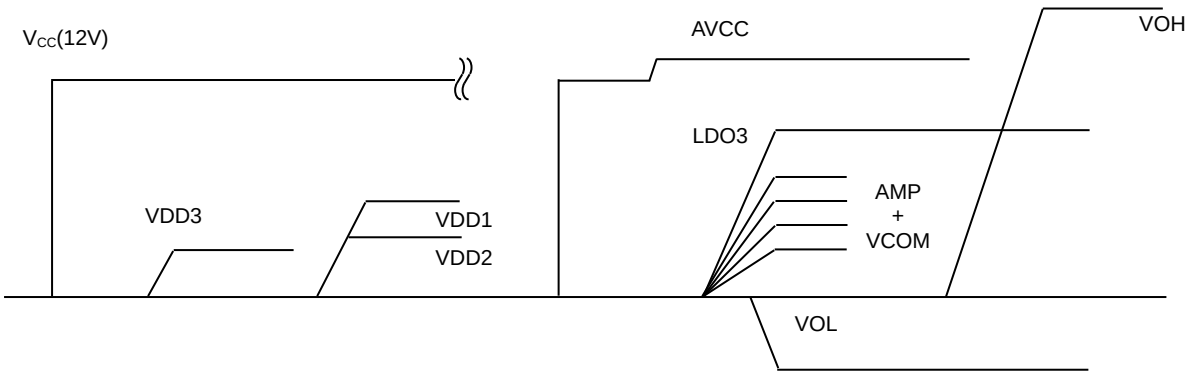


Figure 2. Sequence Chart

Typical Application Circuit (2)

1. Application used to input 5V:

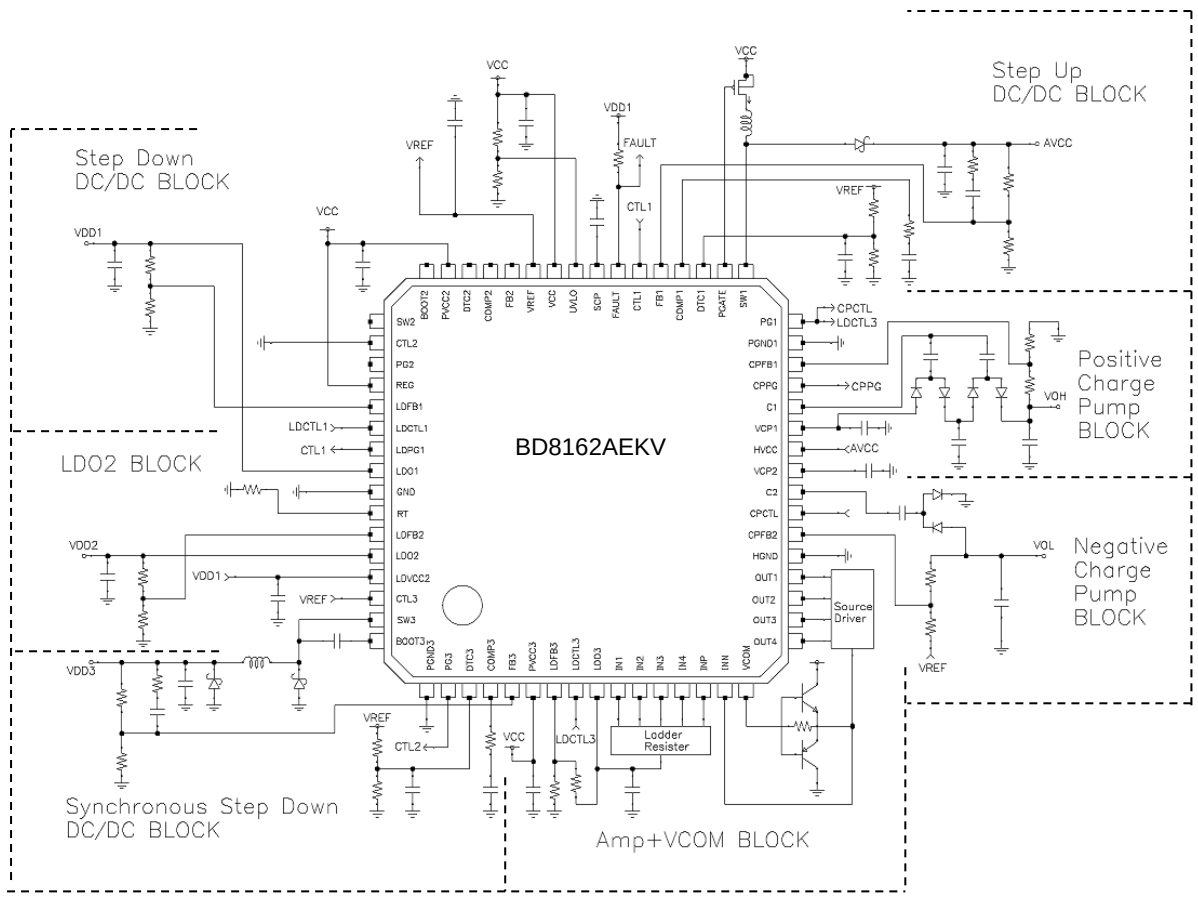
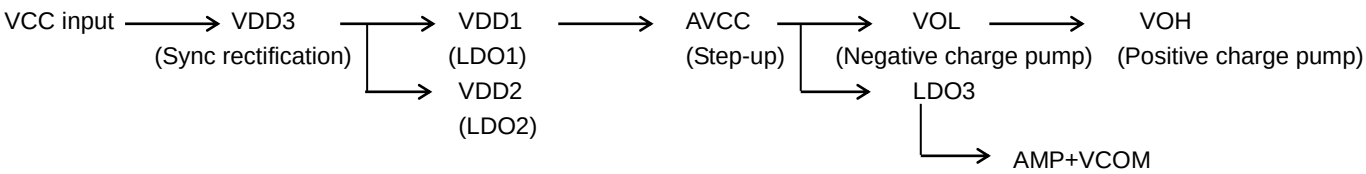


Figure 3. Typical 5V Input Application Circuit Diagram

2. Startup Sequence



3. Sequence Image Chart

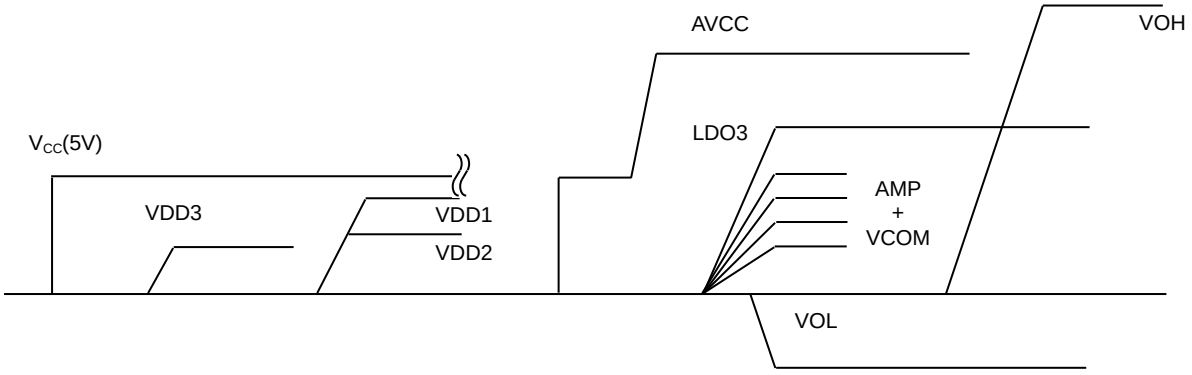
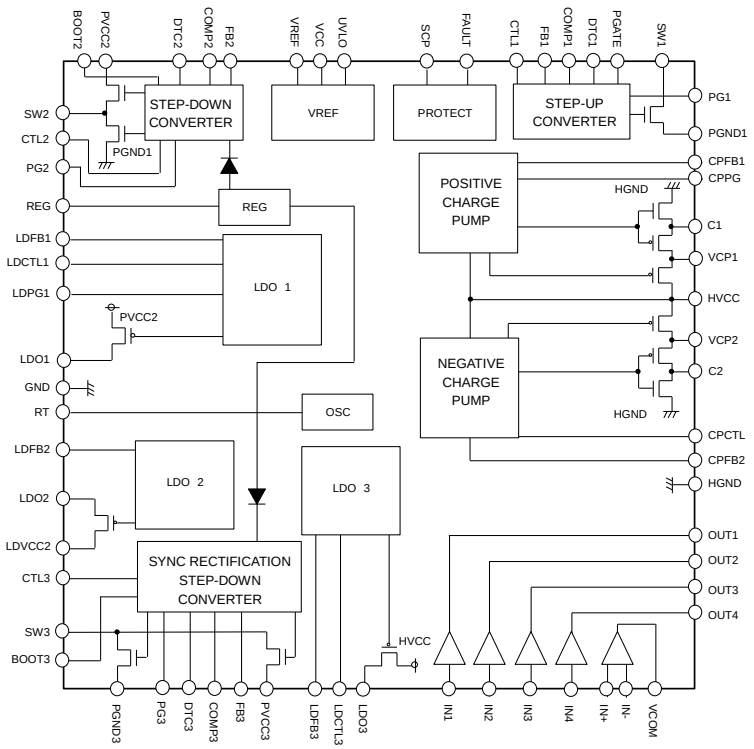


Figure 4. Sequence Chart

Block Diagram



Pin Description

PIN NO.	Pin name	Function	PIN NO.	Pin name	Function	PIN NO.	Pin name	Function
1	PGND3	Ground pin	23	CPCTL	CP control input pin	45	COMP2	Error amp output 2 pin
2	PG3	Power Good output 3 pin	24	C2	Charge pump output 2 pin	46	DTC2	Duty limit pin 2 pin
3	DTC3	Duty limit pin 3 pin	25	VCP2	Charge pump LDO output 2 pin	47	PVCC2	Power supply input pin
4	COMP3	Error amp output 3 pin	26	HVCC	Power supply input pin	48	BOOT2	Switch boot pin 2 pin
5	FB3	Feedback input 3 pin	27	VCP1	Charge pump LDO output 1 pin	49	SW2	Switching output 2 pin
6	PVCC3	Power supply input pin	28	C1	Charge pump output 1 pin	50	CTL2	Control input 2 pin
7	LDFB3	LDO feedback input 3 pin	29	CPPG	CP Power Good output pin	51	PG2	Power Good output 2 pin
8	LDCTL3	LDO3 control input pin	30	CPFB1	Charge pump feedback 1 pin	52	REG	Boot LDO output pin
9	LDO3	LDO output 3 pin	31	PGND1	Ground pin	53	LDFB1	LDO feedback 1 pin
10	IN1	AMP input 1 pin	32	PG1	Power Good output 1 pin	54	LDCTL1	LDO1 control input pin
11	IN2	AMP input 2 pin	33	SW1	Switching output 1 pin	55	LDPG1	LDO1 Power Good output pin
12	IN3	AMP input 3 pin	34	PGATE	Pch gate drive output pin	56	LDO1	LDO output 1 pin
13	IN4	AMP input 4 pin	35	DTC1	Duty limit pin 1 pin	57	GND	Ground pin
14	IN+	COM input + pin	36	COMP1	Error amp output 1 pin	58	RT	Frequency setting pin
15	IN-	COM input – pin	37	FB1	Feedback input 1 pin	59	LDFB2	LDO feedback 2 pin
16	VCOM	COM output pin	38	CTL1	Control input 1 pin	60	LDO2	LDO output 2 pin
17	OUT4	AMP output 4 pin	39	FAULT	Protection detection output pin	61	LDVCC2	Power supply input pin
18	OUT3	AMP output 3 pin	40	SCP	Short-circuit protection delay pin	62	CTL3	Control input 3 pin
19	OUT2	AMP output 2 pin	41	UVLO	Under-voltage lockout protection setting pin	63	SW3	Switching output 3 pin
20	OUT1	AMP output 1 pin	42	VCC	Power supply input pin	64	BOOT3	Switch boot pin 3 pin
21	HGND	Ground pin	43	VREF	Reference voltage output pin			
22	CPFB2	Charge pump feedback 2 pin	44	FB2	Feedback input 2 pin			

Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Rating	Unit
Power Supply Voltage 1	V_{CC}, $V_{PVCC2, 3}$	15	V
Power Supply Voltage 2	V_{LDVCC2}	7	V
Power Supply Voltage 3	V_{HVCC}	20	V
SW1 Pin Voltage	V_{SW1}	20	V
Maximum Junction Temperature	Tjmax	150	°C
Power Dissipation	Pd	5.20 (Note 1)	W
Operating Temperature Range	Topr	-40 to +105	°C
Storage Temperature Range	Tstg	-55 to +150	°C

(Note 1) To use the IC at temperatures over Ta=25°C, derate power rating by 41.6mW/°C.
When mounted on a four-layer glass epoxy board measuring 70 mm x 70 mm x 1.6 mm (with reverse side of copper foil measuring 70mm x 70 mm).

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions (Ta=-40°C to +105°C)

Parameter	Symbol	Min	Max	Unit
Power Supply Voltage 1	V_{CC}, $V_{PVCC2, 3}$	4.2	14	V
Power Supply Voltage 2	V_{LDVCC2}	-	5.5	V
Power Supply Voltage 3	V_{HVCC}	6	18	V
SW1 Pin Voltage	V_{SW1}	-	18	V
SW1 Pin Current	I_{SW1}	-	3	A
SW2, 3 Pin Current	$I_{SW2,3}$	-	2	A
Fault Detection Pull-up Voltage	V_{FAULT}	-	5.5	V
Power Good Pull-up Voltage	V_{PG}	-	5.5	V
Switching Frequency	f_{SW}	200	800	kHz

Electrical Characteristics (Unless otherwise noted, Ta=25°C, V_{CC}=12V, V_{HVCC}=15V)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
[DC/DC Converter Controller Block]						
Step-up Feedback Voltage	V_{FB1}	1.230	1.250	1.270	V	
Step-down Feedback Voltage	V_{FB2}	1.225	1.250	1.275	V	
Sync Rectification Feedback Voltage	V_{FB3}	0.882	0.900	0.918	V	
Input Bias Current	I_{FB}	-1.2	-0.1	+1.2	µA	V_{FB}=1.5V
COMP Source Current	I_{CSO}	15	40	65	µA	
COMP Sink Current	I_{CSI}	-65	-40	-15	µA	
SW1, 2, 3 Max Duty Ratio	MDT	85	92	99	%	
DTC at 0% Duty	V_{DTCMIN}	-	0.1	-	V	V_{FB}=0V
DTC at Max Duty	V_{DTCMAX}	-	0.9	-	V	V_{FB}=0V
DTC Bias Current	I_{DTC}	-1.2	-0.1	+1.2	µA	V_{DTC}=0V
DTC Sink Current	I_{DTC}	1	2	4	mA	
SW1 On Resistance	R_{ON1}	-	0.2	-	Ω	I_{SW}=1A
SW1 Current Limit	I_{SW1OCP}	3	-	-	A	
SW2 High Level On Resistance	R_{ON2H}	-	0.2	-	Ω	I_{SW}=1A
SW2 Low Level On Resistance	R_{ON2L}	-	2	-	Ω	I_{SW}=20mA
SW3 High Level On Resistance	R_{ON3H}	-	0.2	-	Ω	I_{SW}=1A
SW3 Low Level On Resistance	R_{ON3L}	-	0.2	-	Ω	I_{SW}=1A
SW1, 2, 3 Leak Current	I_{SWLEAK}	-5	0	+5	µA	
PGATE Sink Current	I_{PGTSI}	4	9	14	µA	V_{PG}=5V
PGATE Source Current	I_{PGTSO}	4	8	15	mA	V_{PG}=5V
PG On Resistance	R_{ONPG}	0.5	1.0	1.5	kΩ	
PG Leak Current	I_{PGLEAK}	-5	0	+5	µA	
PG1, 2, 3 On Voltage	PGH	-	90	-	%	
PG1, 2, 3 Off Voltage	PGL	-	60	-	%	
[LDO1, 2, 3 Block]						
Feedback Voltage 1, 2 ,3	$V_{LDFB123}$	1.231	1.250	1.269	V	
Input Bias Current	$I_{LDFB123}$	-1.2	-0.1	+1.2	µA	
LDO1 Output Voltage Range 1	V_{LDO1}	0	-	V_{PVCC2}	V	
LDO1 Output Voltage Range 2	V_{LDO2}	0	-	V_{LDVCC2}	V	
LDO1 Output Voltage Range 3	V_{LDO3}	0	-	V_{HVCC}	V	
I/O Voltage Difference 1	V_{DPLD1}	0.3	0.75	1.6	V	V_{LDFB1}=0V, I_O=500mA
I/O Voltage Difference 2	V_{DPLD2}	0.1	0.33	0.75	V	V_{LDFB2}=0V, I_O=200mA
I/O Voltage Difference 3	V_{DPLD3}	0.14	0.3	0.65	V	V_{LDFB3}=0V, I_O=20mA
LDPG1 ON Voltage	LDPG1H	-	90	-	%	
LDPG1 OFF Voltage	LDPG1L	-	60	-	%	

Electrical Characteristics – continued (Unless otherwise noted, Ta=25°C, V_{CC}=12V, V_{HVCC}=15V)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
[Charge Pump Block]						
Positive/Negative Feedback Voltage	V_{CPFB12}	1.225	1.250	1.275	V	
Input Bias Current	I_{CPFB12}	-1.2	-0.1	+1.2	µA	
VCP I/O Voltage Difference	V_{DPCP12}	0.28	0.7	1.55	V	I_O=100mA
C1, 2 High Level On Resistance	R_{ONCH}	-	3	-	Ω	
C1, 2 Low Level On Resistance	R_{ONCL}	-	3	-	Ω	
CPPG1 On Voltage	CPPGH	-	80	-	%	
CPPG1 Off Voltage	CPPGL	-	60	-	%	
[Operation Amplifier Block]						
Input Offset Voltage	V_{OFF}	-15	0	+15	mV	
Input Bias Current	I_{BAMP}	-1.2	0	+1.2	µA	
AMP Output Current Capability	I_{AMP}	30	50	200	mA	
VCOMP Output Current Capability	I_{COM}	60	150	400	mA	
AMP Slew Rate	SRAMP	-	4	-	V/µs	
VCOM Slew Rate	SRCOM	-	4	-	V/µs	
Load Stability	ΔVo	-15	0	+15	mV	I_O=+1mA to -1mA
Max Output Voltage	V_{OH}	V_{HVCC}-1.0	V_{HVCC}-0.8	-	V	I_O=-1mA, V_{IN}=V_{HVCC}-0.8V
Min Output Voltage	V_{OL}	-	0.1	0.16	V	I_O=1mA, V_{IN}=0V
[Overall]						
Reference Output Voltage	V_{VREF}	2.44	2.50	2.66	V	
REG Output Voltage	V_{REG}	4.7	5.0	5.3	V	
Oscillating Frequency	f_{SW}	450	550	650	kHz	R_{RT}=51kΩ
UVLO Pin ON Voltage	V_{UVLOON}	0.88	1.00	1.12	V	
UVLO Pin OFF Voltage	$V_{UVLOOFF}$	0.93	1.05	1.17	V	
VCC Under-Voltage Lockout Protection ON/OFF Voltage	V_{CCUV}	3.5	-	4.2	V	
HVCC Under-Voltage Lockout Protection ON/OFF Voltage	V_{HVUV}	4.3	-	5.3	V	
CTL ON Voltage	V_{CTLON}	2	-	-	V	
CTL OFF Voltage	V_{CTLOF}	-	-	0.2	V	
CTL Bias Current	I_{CTL}	-20	-12.5	-5	µA	V_{CTLX}=0V
SCP Source Current	I_{SCPSO}	2	5	8	µA	
SCP Sink Current	I_{SCPSI}	2	5	10	mA	
SCP Threshold Voltage	V_{SCP}	-	1.25	-	V	
Fault Detection ON Resistance	R_{ONFLT}	0.5	1	1.5	kΩ	
Average Consumption Current 1 (VCC, PVCC2, 3)	I_{CC}	-	5	11	mA	No Switching
Average Consumption Current 2 (HVCC)	I_{HICC}	-	2.8	6	mA	No Switching

Description of Operation of Each Block and Procedure for Selecting Application Components

(1) Step-up DC/DC Converter Block

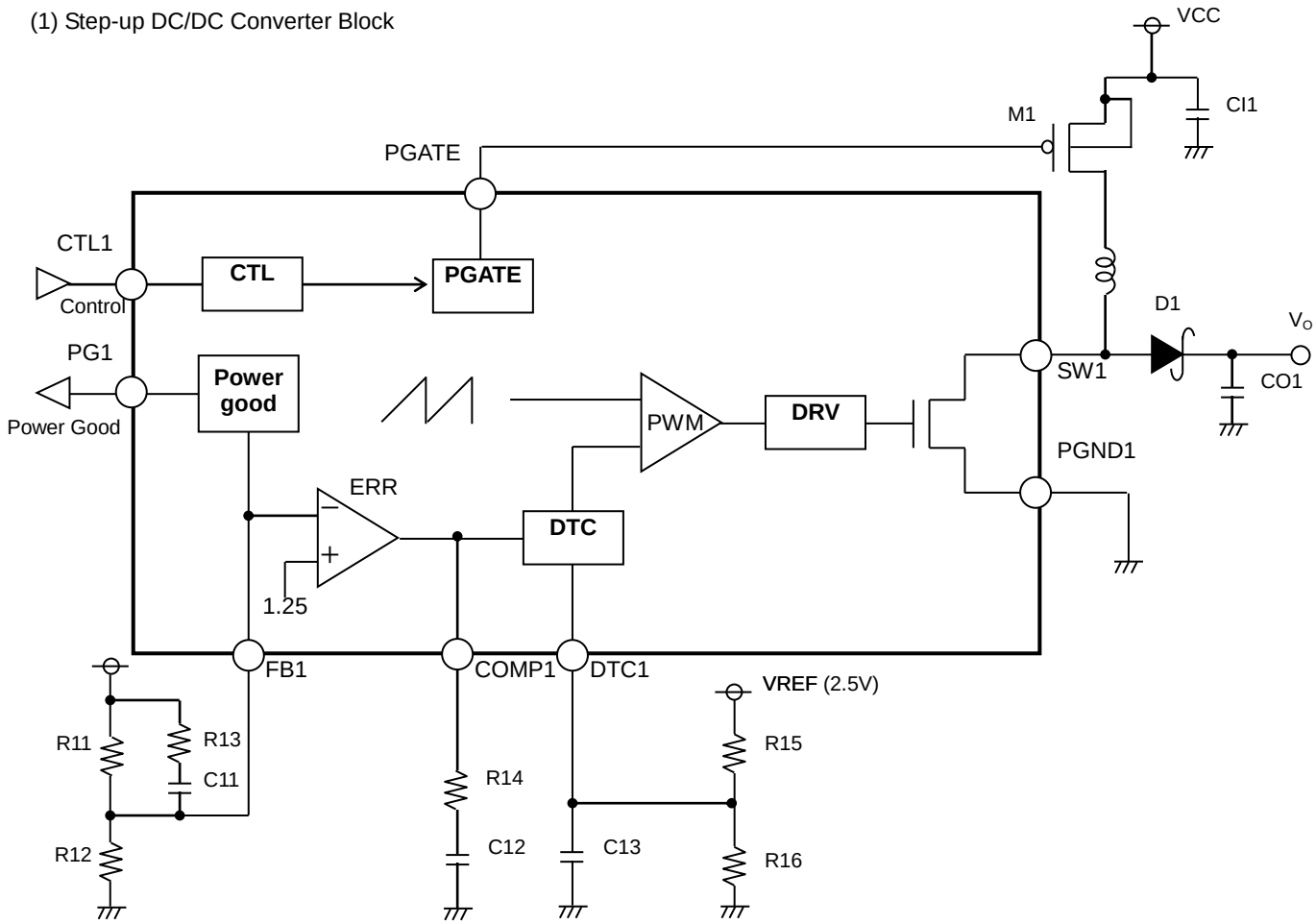


Figure 5. Step-up DC/DC Converter Block

This is a step-up DC/DC converter block that outputs a step-up voltage upon receipt of a signal from CTL1.
When the high-level signal is input to CTL1, a current will be pulled up from PGATE to turn ON input switch M1. At the time of startup, since the switching duty is limited by the DTC1 pin voltage, a soft start is operated. When output reaches 90% of the set voltage, the Power Good signal will be output from PG1.

(1.1) Selecting input switch M1

Input switch M1 will serve as a switch to block the path from VCC to output when a low-level control signal is input to CTL1. Select the input switch with careful attention paid to the following conditions.

Recommended ICs: RSQ and RTQ Series

Maximum inductor current:	$I_{INMAX} + \frac{\Delta I_L}{2}$	<	Rated current of FET
Power supply voltage:	VCC	<	Rated voltage of FET
Power supply voltage:	VCC	<	ON voltage of FET gate

When the CTL1 control input is switched to the high level, a 9μA (Typ) sink current will be pulled from the PGATE pin to turn ON the input switch.

(1.2) Selecting the output L constant

The coil L to be used for output is determined by the rated current I_{LR} and the maximum input current value I_{INMAX} of the coil.

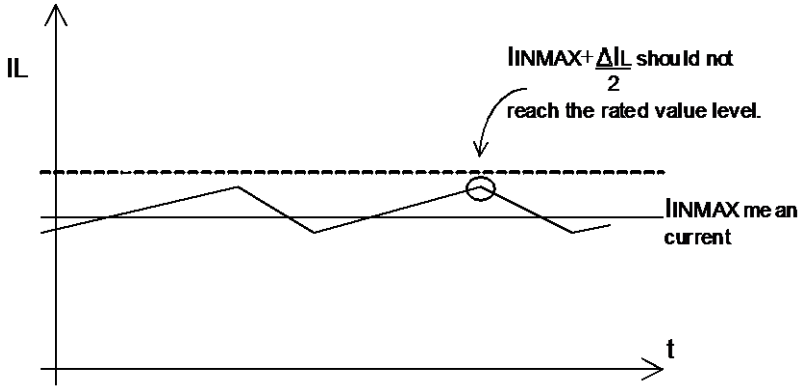


Figure 6. Coil Current Waveform (Step-up DC/DC Converter)

Make adjustments so that $I_{INMAX} + \Delta I_L / 2$ will not reach the rated current I_{LR}. At this time, ΔI_L is obtained by the following equation.

$$\Delta I_L = \frac{1}{L} \quad V_{CC} \times \frac{V_O - V_{CC}}{V_O} \times \frac{1}{f} \quad [A]$$

Where:

f = Switching frequency

In addition, since the coil L value may have variations in the range of approximately ±30%, set this value with sufficient margin.

If the coil current exceeds the rated current I_{LR}, the internal IC element may be damaged.

(1.3) Output capacitor setting

For capacitor C to be used for output, set it to the permissible value of the ripple voltage VPP or that of the drop voltage at the time of a sudden load change, whichever is larger.

The output ripple voltage is obtained by the following equation.

$$\Delta VPP = I_{LMAX} \times R_{ESR} + \frac{1}{fC_O} \quad \times \frac{V_{CC}}{V_O} \times (I_{LMAX} - \frac{\Delta I_L}{2})$$

Make this setting so that the voltage will fall within the permissible ripple voltage range.
For the drop voltage VDR during a sudden load change, estimate the VDR with the following equation.

$$VDR = \frac{\Delta I}{C_O} \quad \times 10\mu\text{sec} \quad [V]$$

Wherein, 10 µsec is the estimate of DC/DC response speed.
Set C_O so that these two values will fall within the limit values.

Since the DC/DC converter causes a peak current to flow between input and output, capacitors must also be mounted on the input side. For this reason, it is recommended to use low-ESR capacitors above 10µF and below 100mΩ as the input capacitors. Using input capacitors outside of this range may superimpose excess ripple voltage upon the input voltage, causing the IC to malfunction.

However, since the aforementioned conditions vary with load current, input voltage, output voltage, inductor value, and switching frequency, be sure to verify the margin using the actual product.

(1.4) Output rectifier diode setting

For the rectifier diodes to be used as the output stage of the DC/DC converter, it is recommended to use Schottky diodes. Select diodes with careful attention paid to the maximum inductance current, maximum output voltage, and power supply voltage.

Maximum inductance current: $I_{INMAX} + \frac{\Delta I_L}{2}$ < Rated current of diode

Maximum output voltage: V_{OMAX} < Rated voltage of diode

In addition, since each parameter has variations in current and voltage of 30% to 40%, design systems with sufficient margin.

(1.5) Output voltage setting

Set output voltage using the following equation with feedback resistance composed of R11 and R12.

$$V_O = \frac{R11 + R12}{R12} \times 1.25 \quad [V]$$

Set the maximum output voltage to not more than 18V so that it will not exceed the rating of the SW1 pin.
It is recommended to apply a setting range of 10kΩ to 330kΩ. Setting the feedback resistance to not more than 10kΩ will result in degraded voltage efficiency, while setting it to not less than 330kΩ will result in higher offset voltage due to an input bias current of 0.1μA (Typ) of the internal error amplifier.

(1.6) Phase compensation setting

Phase setting procedure:
The following conditions are required to ensure the stability of the negative feedback system.

- When the gain is set to “1” (0 dB), the phase lag should not be more than 150° (i.e., phase margin should not be less than 30°).

In addition, since DC/DC converter applications are sampled according to the switching frequency, the overall system GBW should be set to not more than 1/10 of the switching frequency. The targeted characteristics of the applications can be summarized as follows.

- When the gain is set to “1” (0 dB), the phase lag should not be more than 150° (i.e., phase margin should not be less than 30°).
- The GBW at that time (i.e., frequency when the gain is set to “0 dB”) should not be more than 1/10 of the switching frequency.

The responsiveness is determined by the GBW limitation. Consequently, to raise the responsiveness, higher switching frequencies are required.

To ensure the stability through the phase compensation, it is necessary to cancel the secondary phase delay (-180°) caused by LC resonance with the secondary phase lead (in other words, by adding two phase leads).
The GBW (i.e., frequency when the gain is set to “0 dB”) is determined by phase compensation capacitance connected to the error amplifier. If GBW needs to be reduced, increase the capacitance of the capacitor.

(i) Ordinary integrator (Low-pass filter)

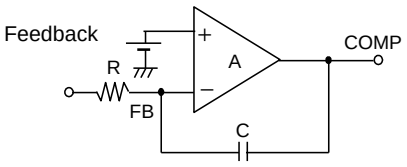


Figure 7

$$Point(a)\quad fa = \frac{1}{2\pi RCA} \quad [Hz]$$

(ii) Open loop characteristics of integrator

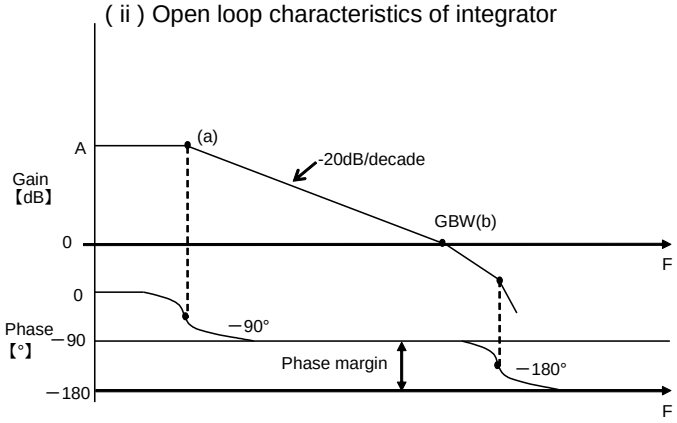
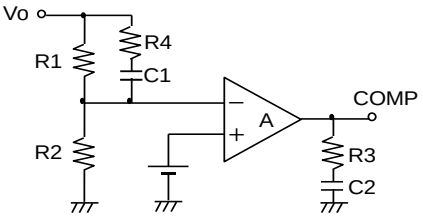


Figure 8

$$Point(b)\quad fb = GBW = \frac{1}{2\pi RC} \quad [Hz]$$

Since the phase compensation like that shown in (a) and (b) applies to the error amplifier, it will act as a low-pass filter.
For DC/DC converter applications, R represents feedback resistors connected in parallel.

According to the LC resonance of the output, two phase leads should be added.



$$LC\ resonant\ frequency \quad fp = \frac{1}{2\pi\sqrt{LC}} \quad [Hz]$$

$$Phase\ lead \quad fz1 = \frac{1}{2\pi C1R1} \quad [Hz]$$

$$Phase\ lead \quad fz2 = \frac{1}{2\pi C2R3} \quad [Hz]$$

Figure 9

Set the lead frequency of one of the phases close to the LC resonant frequency for the purpose of canceling the LC resonance.

Note: If high-frequency noise occurs in output, it will pass through capacitor C1 and affect the feedback. To avoid this problem, add resistor R4 of approximately 1kΩ in series with capacitor C1.

(1.7) Duty cycle limit setting

Applying a voltage to the DTC pin makes it possible to fix the maximum duty cycle. Furthermore, since the upper limit value of the maximum duty cycle is fixed within the IC, it will not increase beyond the upper limit value. Figure 10 shows the relationship between the DTC voltage and the maximum duty cycle. Refer to this figure to make the DTC voltage setting. Subsequently, set R15 and R16 so that the DTC voltage will reach the level shown in the figure.

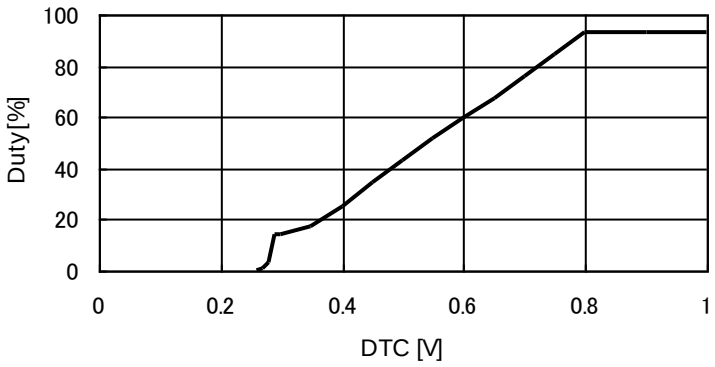


Figure 10. Characteristics of DTC Voltage vs Duty Cycle

Set the maximum duty cycle with sufficient margin so that it will not reach the maximum duty cycle for normal use. For step-up converters, the range normally used is as follows.

$$\text{Max On duty cycle} = \frac{V_{OMAX} - V_{CCMIN}}{V_{OMAX}} < \text{Max set duty cycle}$$

(1.8) Soft-start time setting

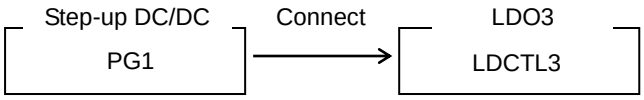
Adding capacitor C13 to DTC resistive dividers R15 and R16 makes it possible to use the soft-start function. The soft-start function is needed to prevent an excessive increase in coil current and output voltage overshoot at startup. The capacitance and soft-start time are obtained by the following equation.

$$tss = -C13 \times \frac{R15 \times R16}{R15 + R16} \times \ln\left(1 - \frac{\frac{V_O - V_{CC}}{V_O} \times 0.62 + 0.28}{2.5 \times \frac{R16}{R15 + R16}}\right) \quad [\text{sec}]$$

(1.9) Control and Power Good functions

When the control pin (CTL) is set to low-level input, the relevant block will stop operation. The control pin voltage is internally pulled up to the reference voltage VREF, whereby operating the relevant block in the open state.
The Power Good terminal (PG) is designed in an open-drain pattern to use as the control pin of a different block or an external power-good signal. The PG pin outputs a low-level signal while in the rising mode and, when the output voltage reaches 90% of the set voltage, will enter a high impedance state. At this time, the CTL pin at the destination will be switched to high-level input by the use of a pull-up resistor. In contrast, when the output voltage falls below 60% of the set voltage, the CTL pin will switch to low-level output.
To use the PG pin output as an external signal, connect a pull-up resistor.
A pull-up resistance ranging from 51kΩ to 200kΩ is recommended.

Typical application:



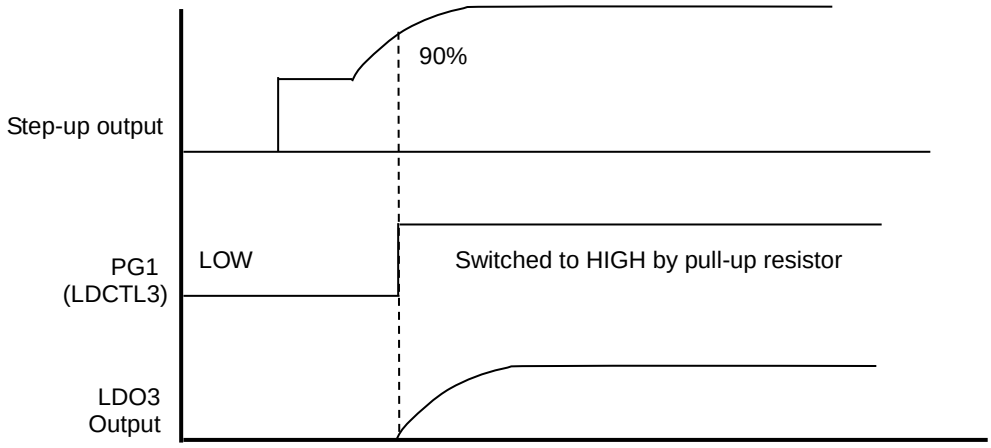


Figure 11. Typical Application of Control / Power Good Functions

(2) Step-down DC/DC Converter Block and
Sync Rectification Step-down DC/DC Converter Block

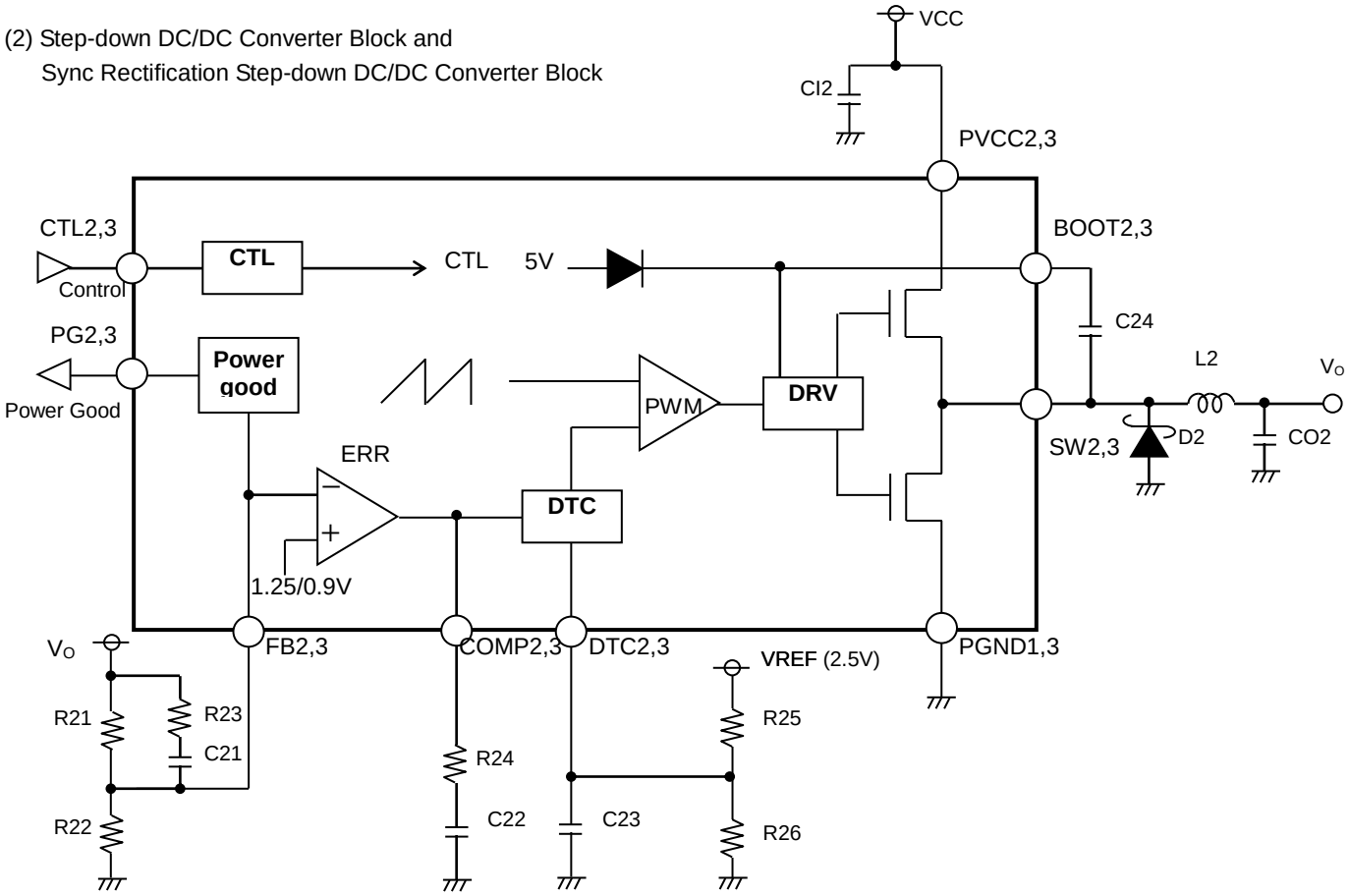


Figure 12. Step-down DC/DC Converter Block and Sync Rectification Step-down DC/DC Converter Block

The step-down DC/DC converter block and the sync rectification step-down DC/DC converter block differ in the feedback voltage and SW low-level On resistance, but have about the same configuration.
While the control signal remains at low level, the low-level SW turns ON to output a low voltage. When the control signal is switched to a high level, output voltage will start rising with the soft start function in operation.
When the output voltage reaches 90% of the set voltage, the Power Good signal will be output.

(2.1) Selecting the output L constant

The inductance L to be used for output is determined by the rated current I_{LR} and the maximum output current value I_{OMAX} of the inductor.

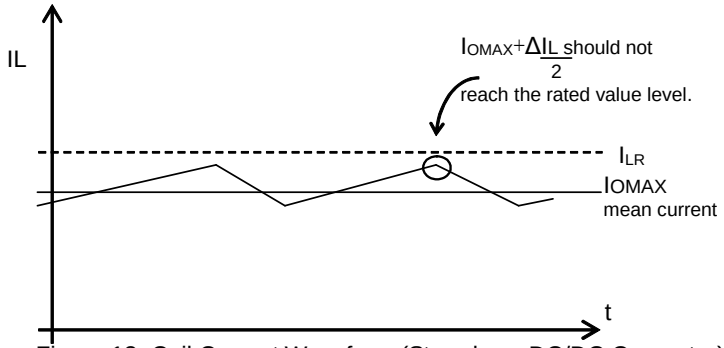


Figure 13. Coil Current Waveform (Step-down DC/DC Converter)

Make adjustments so that $I_{OMAX} + \Delta I_L / 2$ will not reach the rated current I_{LR}. At this time, ΔI_L is obtained by the following equation.

$$\Delta I_L = \frac{1}{L} \times (V_{CC} - V_O) \times \frac{V_O}{V_{CC}} \times \frac{1}{f} \quad [A]$$

In addition, since the inductance L value may have variations in the range of approximately ±30%, set this value with sufficient margin.
If the coil current exceeds the rated current I_{LR}, the internal IC element may be damaged.

(2.2) Selecting I/O capacitors

To select I/O capacitors, refer to information in Section (1.3).
However, the output ripple voltage of the step-down DC/DC converter is obtained by the following equation.

$$\Delta V_{PP} = \Delta I_L \times R_{ESR} + \frac{\Delta I_L}{2C_O} \times \frac{V_O}{V_{CC}} \times \frac{1}{f} \quad [V]$$

(2.3) Output rectifier diode setting

For the rectifier diodes to be used as the output stage of the DC/DC converter, it is recommended to use Schottky diodes. Select diodes with careful attention paid to the maximum inductance current, maximum output voltage, and power supply voltage.

Maximum inductance current:	$I_{OMAX} + \frac{\Delta I_L}{2}$	<	Rated current of diode
Power supply voltage:	VCC	<	Rated voltage of diode

In addition, since each parameter has variations in current and voltage of 30% to 40%, design systems with sufficient margin.

(2.4) Output voltage setting

Set output voltage using the following equation with feedback resistance composed of R21 and R22.

$$V_O = \frac{R21 + R22}{R22} \times V_{FB} \quad [V]$$

Where:

V_{FB}: Set to 1.25 for the step-down DC/DC converter (FB2) and 0.9 for the sync rectification step-down DC/DC converter (FB3).

It is recommended to apply a setting range of 10kΩ to 330kΩ. Setting the feedback resistance to not more than 10kΩ will result in degraded voltage efficiency, while setting it to not less than 330kΩ will result in higher offset voltage due to an input bias current of 0.1μA (Typ) of the internal error amplifier.

(2.5) Phase compensation setting

For details of phase compensation setting, refer to information in Section (1.6).

(2.6) Duty cycle limit setting

For details of duty cycle limit setting, refer to information in Section (1.7).
For step-down converters, however, the range normally used comes to the following:

$$\text{Max On duty cycle} = \frac{V_{OMAX}}{V_{CCMIN}} < \text{Max set duty cycle}$$

(2.7) Soft start time setting

Adding the capacitor C23 to the DTC resistive dividers R25 and R26 makes it possible to use the soft start function. The soft start function is needed to prevent an excessive increase in coil current at startup and output voltage overshoot at startup. The capacitance and soft start time are obtained by the following equation:

$$tss = -C23 \times \frac{R25 \times R26}{R25 + R26} \times \ln\left(1 - \frac{\frac{V_O}{V_{CC}} \times 0.62 + 0.28}{2.5 \times \frac{R26}{R25 + R26}}\right) \quad [\ s\ e$$

(2.8) Control and Power Good functions

For details of the control and Power Good functions, refer to information in Section (1.9).

(3) LDO1 to LDO3 blocks

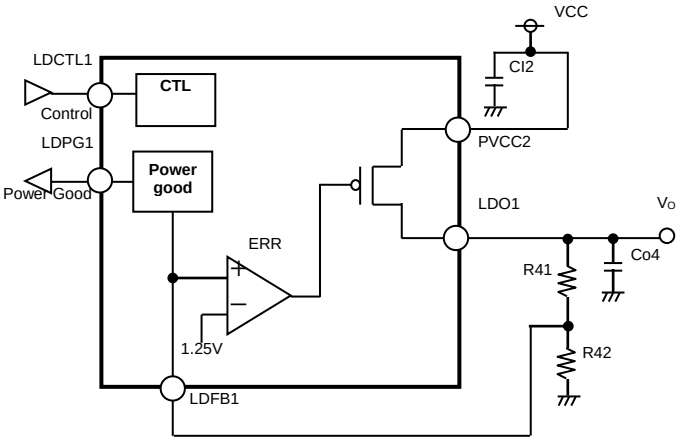


Figure 14. LDO1 Block

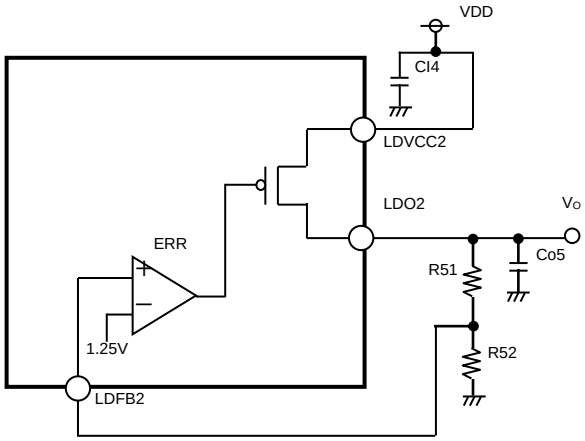


Figure 15. LDO2 Block

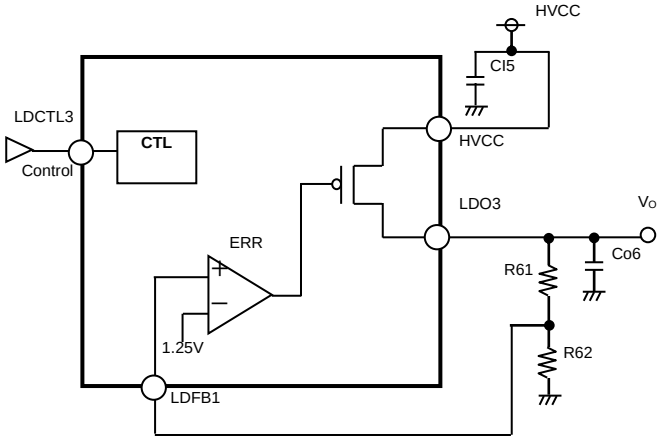


Figure 16. LDO3 Block

(3.1) Selecting I/O capacitors

The LDO1 to LDO3 blocks are ceramic capacitor compatible.
Capacitance in the range of 1µF to 100µF is recommended.

(3.2) Output voltage setting

Set output voltage using the following equation with feedback resistance composed of R∗1 and R∗2.

$$V_O = \frac{R*1 + R*2}{R*2} \times 1.25 \quad [V]$$

∗:4 to 6

It is recommended to apply a setting range of 10kΩ to 330kΩ. Setting the feedback resistance to not more than 10kΩ will result in degraded voltage efficiency, while setting it to not less than 330kΩ will result in higher offset voltage due to an input bias current of 0.1μA (Typ) of the internal error amplifier.

The following table shows the output voltage setting ranges and current capabilities.

	Minimum setting	Maximum setting (with maximum output current)	Output current capability
LDO1	1.5V	VCC (Max 14V) -1.6V	Up to 500mA
LDO2	1.5V	LDVCC2 (Max 5.5V) -0.75V	Up to 200mA
LDO3	1.5V	HVCC (Max 18V) -0.65V	Up to 20mA

(3.3) Control and Power Good functions

For details of the control and Power Good functions, refer to information in Section (1.9).
For the LDO3 block, however, set output voltage so that the signal will be input into the control pin after HVCC, which serves as a power source, starts up.

(4) Charge Pump Block

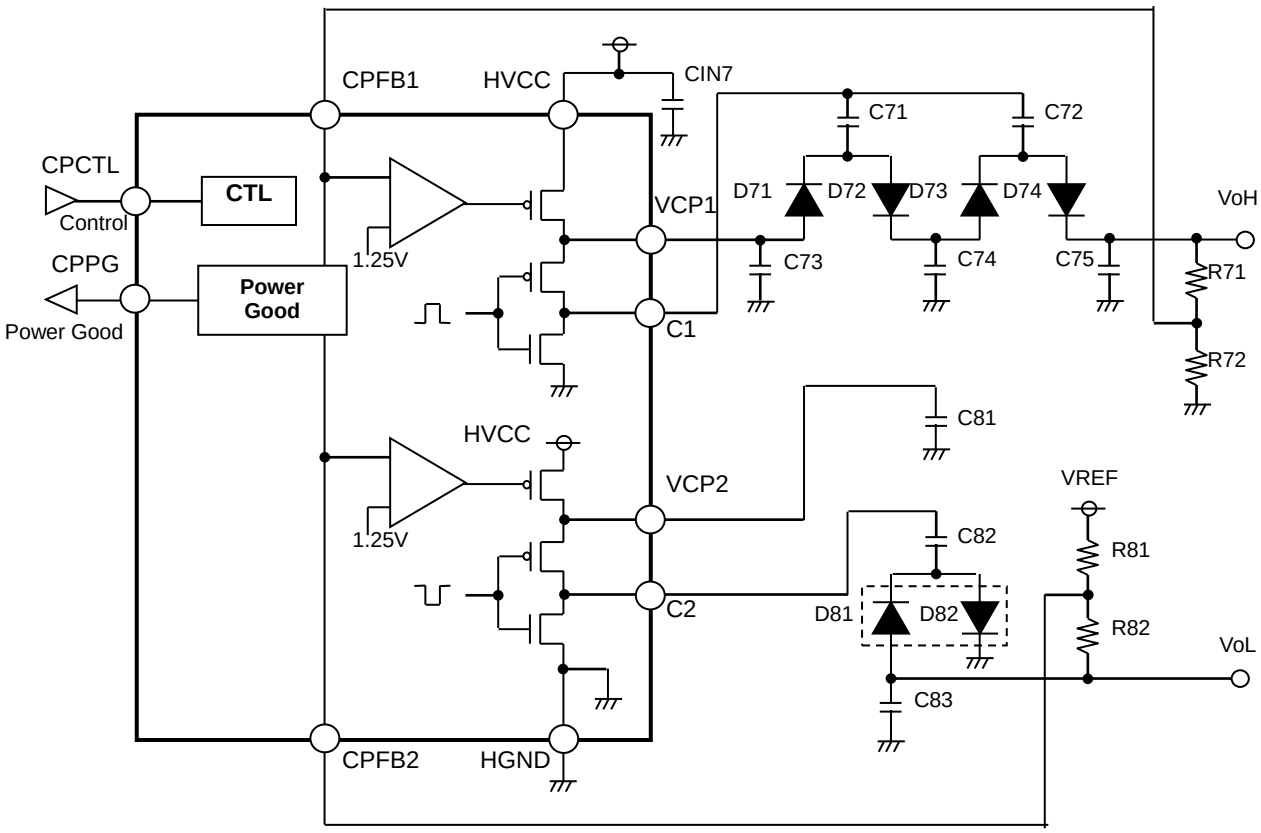


Figure 17. Charge Pump Block

When the charge pimp block receives the control input signal, the negative-side charge pump will start operation. The startup sequences are internally fixed. Consequently, when the negative-side charge pump reaches 80% of the set voltage, the positive-side charge pump will start operation. When both negative- and positive-side charge pumps reach 80% of the set voltage, the power-good signal will be output from the CPPG pin.

(4.1) Selecting output diodes

For diodes D71 to D74, and D81 and D82, select Schottky diodes having a current capability three times (positive side) or two times (negative side) as high as the maximum output current and a withstand voltage higher than the output voltage.
Due to the aforementioned requirements, it is recommended to use the RB550EA dual Schottky barrier diode.

(4.2) Selecting output capacitors

Capacitors C73 and C81 serve as output capacitors for the charge pump regulators; a capacitance in the range of 1μF to 10μF is recommended. Capacitors C71, C72, and C82 serve as flying capacitors; a capacitance in the range of 0.1μF to 1μF is recommended. Capacitors C74, C75, and C83 serve as charge pump output capacitors; a capacitance in the range of 0.1μF to 10μF is recommended.

(4.3) Output voltage setting

Set output voltage using the following equation with feedback resistance.

$$V_OH = \frac{R71 + R72}{R72} \times 1.25\,[V]$$

$$V_OL = VREF - \frac{R81 + R82}{R81} \quad (VREF - 1.25)$$

$$= 2.5 - \frac{R81 + R82}{R81} \times 1.25\,[V]$$

It is recommended to apply a setting range of 10kΩ to 330kΩ. Setting the feedback resistance to not more than 10kΩ will result in degraded voltage efficiency, while setting it to not less than 330kΩ will result in higher offset voltage due to an input bias current of 0.1μA (Typ) of the internal error amplifier.

(4.4) Control and Power Good functions

Make the sequence setting by inputting the power-good signal output from a different block. However, make this setting so that the signal will be input into the CPCTL control pin after HVCC, which serves as a power source, starts up. For example, to generate HVCC in the step-up DC/DC converter block, do not set the sequence so that the same Power Good pin is connected to CTL1 and CPCTL. Since the sequences of the negative- and positive-side charge pumps are internally fixed, the sequence of the negative-side pump starts up first and is followed by that of the positive-side pump. When both negative- and positive-side charge pumps reach 80% of the set voltage, the power-good signal will be output from the CPPG pin. The power-good signal output pattern is the same as that of different blocks. For details, refer to information in Section (1.9).

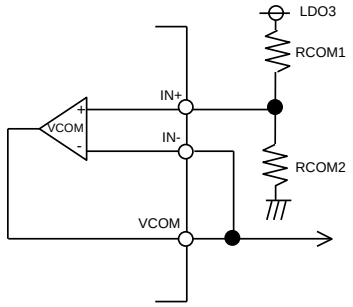
(5) Common Amplifier + 4ch Buffer Amplifier

The AMP and VCOM amplifiers operate in the range of 0.1V to HVCC−0.8V (Typ). Normally, use the VCOM amplifier as a buffer type amplifier as shown in (a). Use the output voltage of the LDO3 block for power supply on the reference side.

To increase the current drive capability, use the PNP and NPN transistors as shown in (b).

When the VCOM amplifier is not used, set the block to the buffer type as shown in (a) and ground the V+ pin. In this case, it is recommended to set the R3 and R4 resistors in the range of 10kΩ to 100kΩ. Setting them to not more than 10kΩ may increase current consumption, thus resulting in degraded power efficiency. Setting them to not less than 100kΩ may result in higher offset voltage due to the input bias current of 0.1μA (Typ).

(a)



(b)

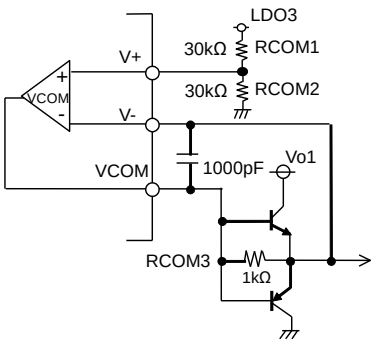


Figure 18 VCOM Block

$$VCOM = \frac{RCOM2}{RCOM1 + RCOM2} \times LDO3 \quad [V]$$

Resistance of approximately 1kΩ is recommended for RCOM3.

(6) Common Block

(6.1) UVLO function

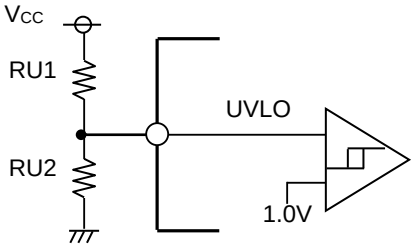


Figure 19. UVLO Block

Set the UVLO voltage with RU1 and RU2. The UVLO protection function will be implemented when the UVLO pin voltage falls below 1.0V (Typ) and canceled when it exceeds 1.05V (Typ). The VCC voltage at which the UVLO function is activated is expressed by the following equation.

$$VUVLO = \frac{RU1 + RU2}{RU2} \quad [V]$$

It is recommended to set resistance in the range of 10kΩ to 200kΩ.

In addition, the VCC pin incorporates a fixed UVLO function. Consequently, when the UVLO pin voltage falls below 3.8V (Typ), the UVLO protection function will be operated even if the external UVLO voltage is set below 3.8V (Typ).

(6.2) SCP function

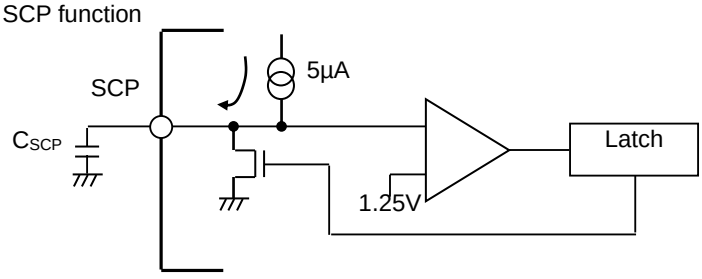


Figure 20. SCP Block

The SCP function protects against short-circuits in the outputs of the step-up DC/DC converter, step-down DC/DC converter, sync rectification step-down DC/DC converter, LDO1, and charge pump blocks. When any one of these outputs falls below 60% of the set voltage, it will be regarded as a short-circuit in output, thus activating the short-circuit protection function.
If a short-circuit is detected, source current of 5μA (Typ) will be output from the SCP pin. Then, delay time will be set with external capacitance. When the SCP pin voltage exceeds 1.25V (Typ), the state will be latched to shut down all outputs. Once the state has been latched, it will not be canceled unless VCC restarts. The delay time setting is obtained by using the following equation.

$$TL\,[s] = (C_{SCP} \times 1.25)/(5 \times 10^{-6})$$

Even if none of the output startup sequences is complete at startup of the IC, short-circuits will be detected and the SCP function activated. For this reason, set the delay time substantially longer than the startup time.

(6.3) Fault detection function

This IC has the built-in fault detection function that alerts the operating status of protection circuits.
If any of the protection circuits turns ON, the FAULT pin will be pulled up to output low voltage.
In stable operating status, the pin outputs high voltage. In this case, resistance ranging from 10kΩ to 220kΩ is recommended. Setting resistance to not more than 10kΩ may generate offset voltage due to the internal On resistance, thus disabling proper output of low voltage. In contrast, setting it to not less than 220kΩ may not output proper high-level voltage due to leak current.

The FAULT pin is switched to low voltage output under any of the following conditions.

- When the UVLO (under-voltage protection) function is activated;
- When the TSD (thermal shutdown circuit) function is activated;
- When the OCP (overcurrent protection circuit) function is activated, or;
- When the SCP (short-circuit protection) function is activated.

(6.4) Variable oscillator

Changing the timing resistance RT enables switching frequency adjustment. Set resistance referring to Figure 21. Set frequency in the range of 200kHz to 800kHz.

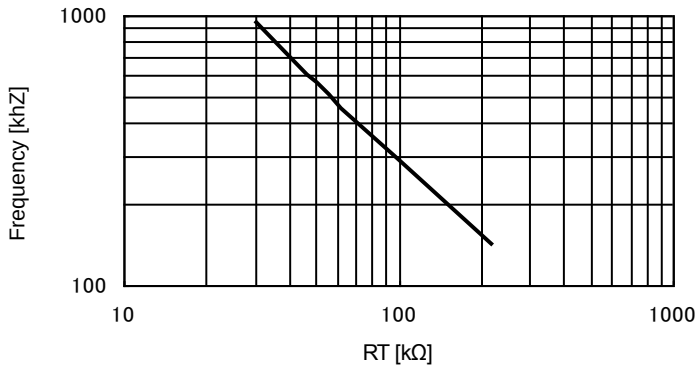


Figure 21. RT vs Switching Frequency

I/O Equivalent Circuits

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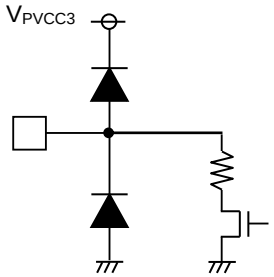	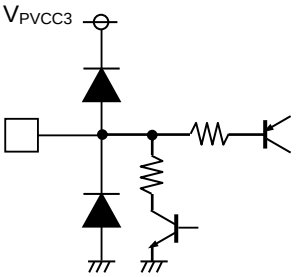	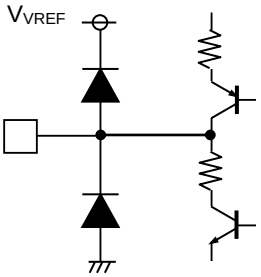
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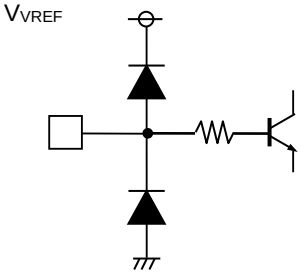
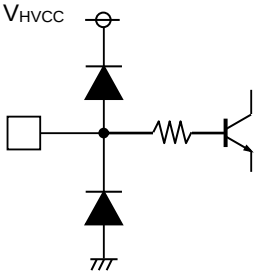
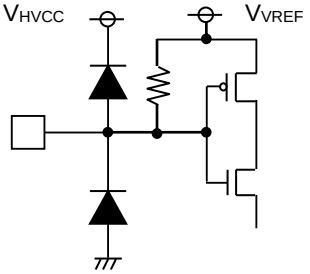
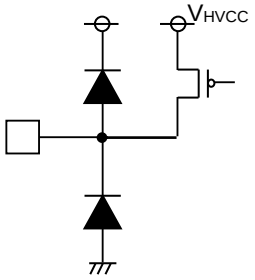
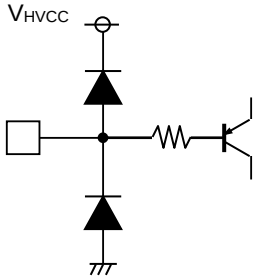
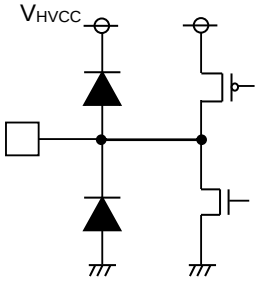
		
9.LDO3	10.IN1 11.IN2 12.IN3 13.IN4 14.IN+ 15.IN-	16.VCOM 17.OUT4 18.OUT3 19.OUT2 20.OUT1 24.C2 28.C1
		
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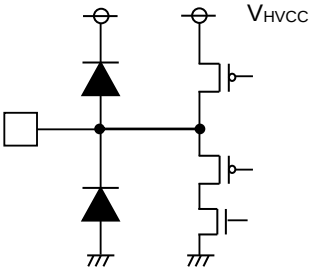	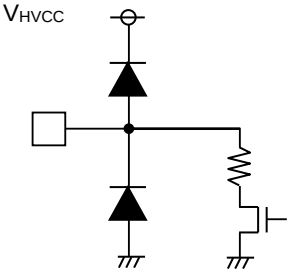	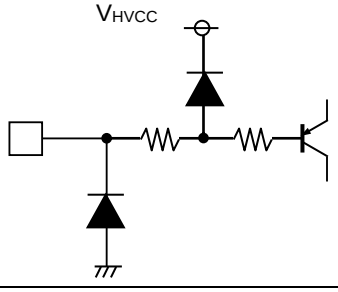
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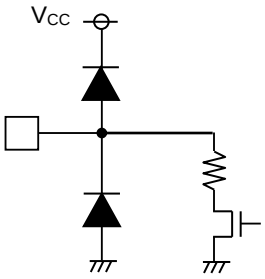	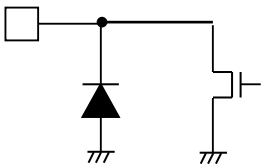	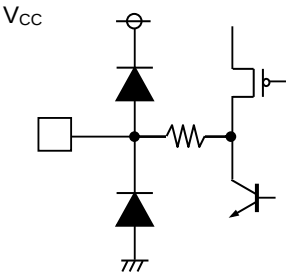

I/O Equivalent Circuits - Continued

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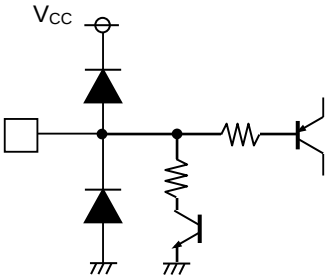	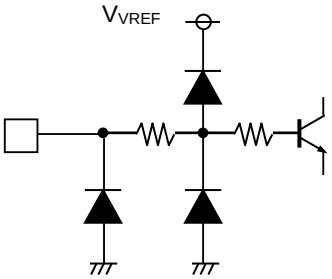	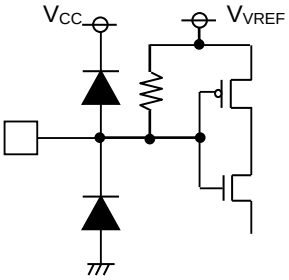
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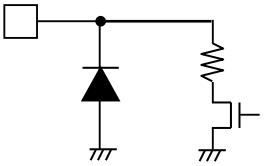	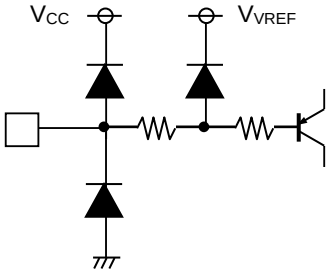	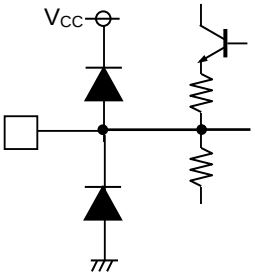
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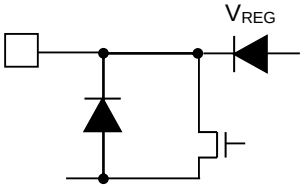	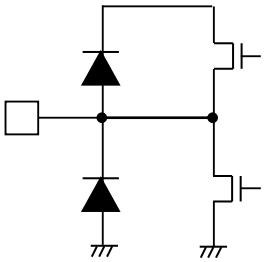	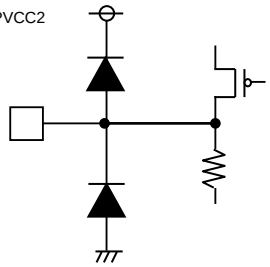
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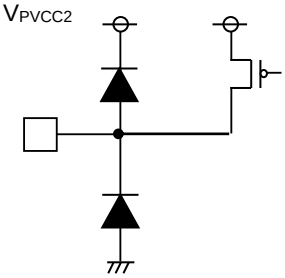	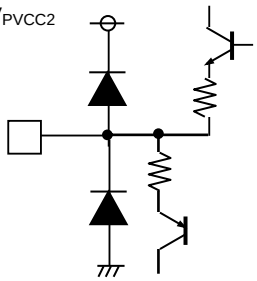	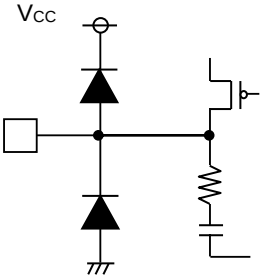
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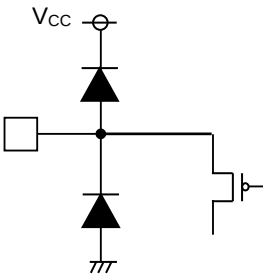
		

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the maximum junction temperature rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. **Unused Input Pins**
    Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

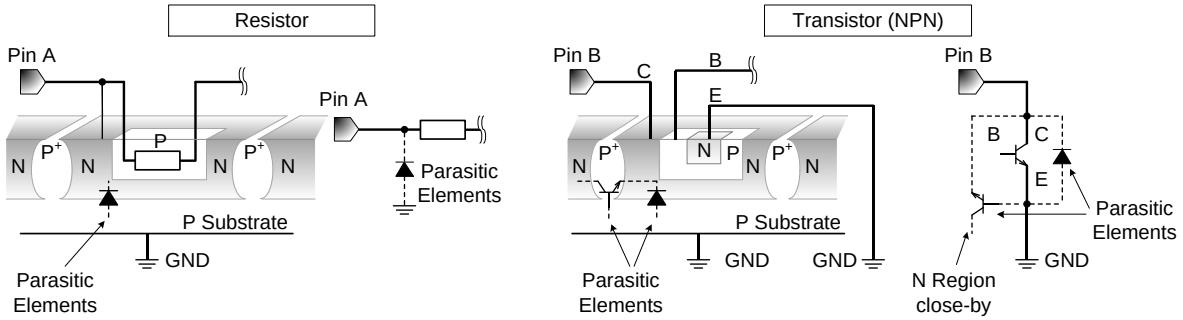


Figure 22. Example of monolithic IC structure

13. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

14. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

15. Discontinuous mode

The step-up and step-down DC/DC converters used in this IC have been designed on the assumption that the converters are used in continuous mode. Using the IC constantly while in discontinuous mode may result in malfunctions. To avoid this problem, make coil adjustments or insert a resistor between output and GND to prevent the IC from entering discontinuous mode while in use.

16. PCB layout for open-drain pin (SW1) of step-up DC/DC converter

Connect the open-drain pin of the FET built in the step-up DC/DC converter to the coil / diode with as thick and short of a line as possible. Particularly, making the line distance between the open-drain pin and the external diode longer or routing it with the use of a through-hole may form parasitic impedance due to patterns and cause the open-drain pin to generate a high surge voltage, thus leading to IC destruction. For this reason, ensure that the open-drain pin voltage (direct mounting to IC pin) will never exceed the absolute maximum ratings in practical applications of this IC.

Ordering Information

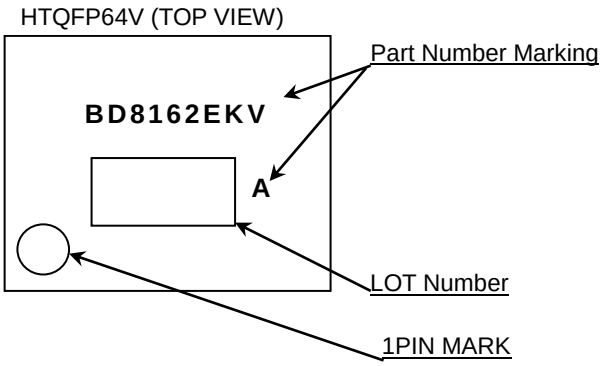
B	D	8	1	6	2	A	E	K	V	-	

Part number

Package
EKV：HTQFP64V

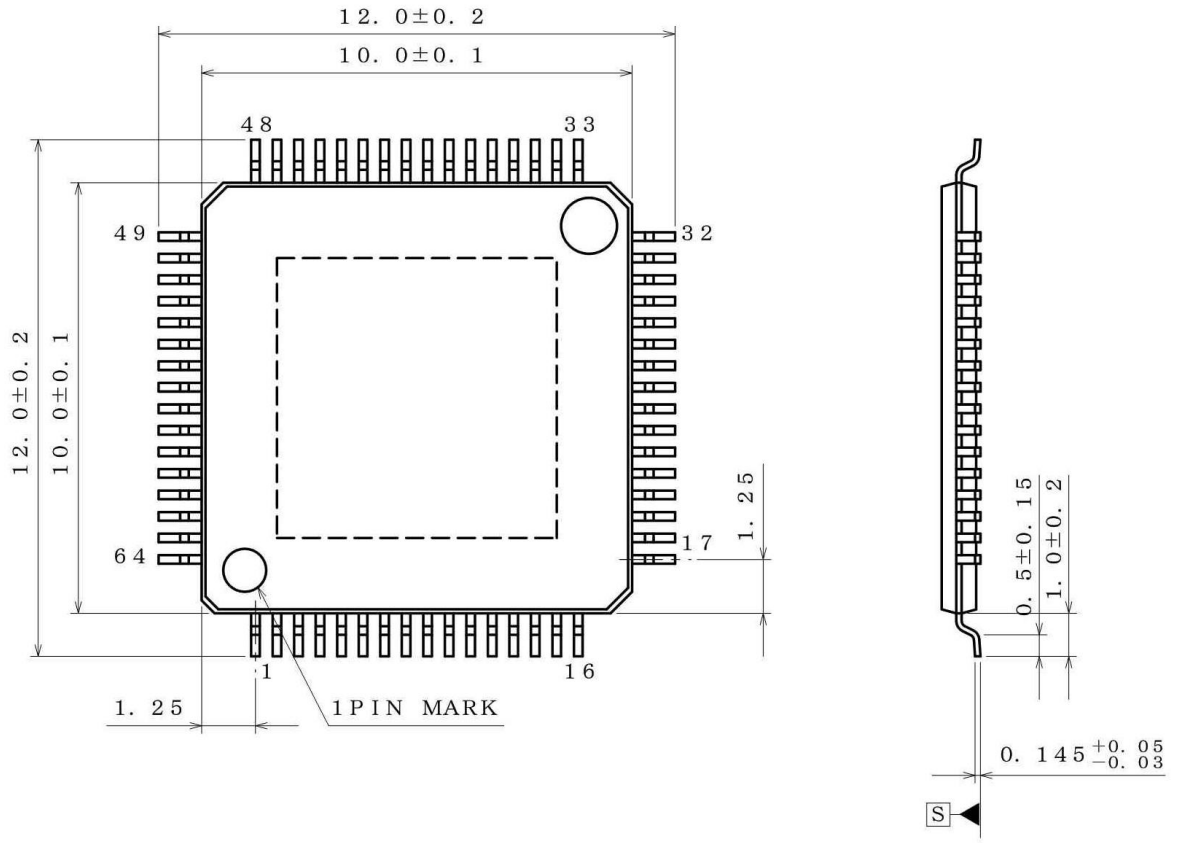
Packaging and forming specification
None: Tray

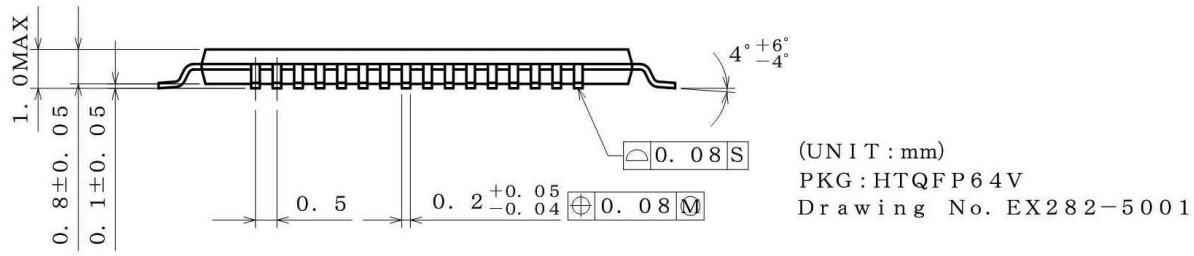
Marking Diagram



Physical Dimension, Tape and Reel Information

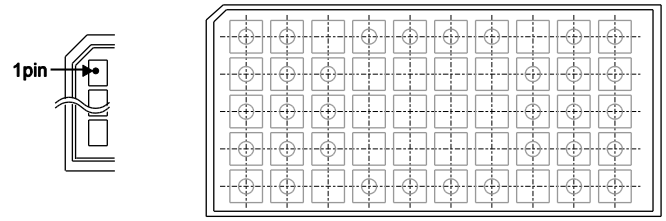
Package Name	HTQFP64V





<Tape and Reel information>

Container	Tray (with dry pack)
Quantity	1000pcs
Direction of feed	Direction of product is fixed in a tray



*Order quantity needs to be multiple of the minimum quantity.

Revision History

Date	Revision	Changes
15.Feb.2016	001	New Release

Notice

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1. Our Products are designed and manufactured for application in ordinary electronic equipments (such as AV equipment, OA equipment, telecommunication equipment, home electronic appliances, amusement equipment, etc.). If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), transport equipment, traffic equipment, aircraft/spacecraft, nuclear power controllers, fuel controllers, car equipment including car accessories, safety devices, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are designed and manufactured for use under standard conditions and not under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

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