CSD16327Q3 25-V N-Channel NexFET™ Power MOSFET

1 Features

- Optimized for 5-V Gate Drive
- Ultra-Low Q_g and Q_{gd}
- Low Thermal Resistance
- Avalanche Rated
- Lead-Free Terminal Plating
- RoHS Compliant
- Halogen Free
- SON 3.3-mm × 3.3-mm Plastic Package

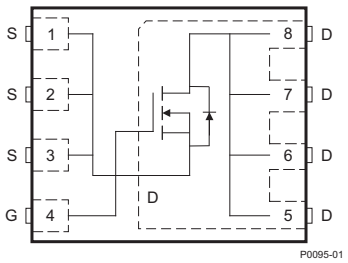
2 Applications

- Point-of-Load Synchronous Buck Converter for Applications in Networking, Telecom and Computing Systems
- Optimized for Control or Synchronous FET Applications

3 Description

This 25-V, 3.4-mΩ, SON 3.3-mm × 3.3-mm NexFET™ power MOSFET has been designed to minimize losses in power conversion and optimized for 5-V gate drive applications.

Top View



Product Summary

T_A = 25°C		TYPICAL VALUE		UNIT
V_{DS}	Drain-to-Source Voltage	25		V
Q_g	Gate Charge Total (4.5 V)	6.2		nC
Q_{gd}	Gate Charge Gate-to-Drain	1.1		nC
$R_{DS(on)}$	Drain-to-Source On-Resistance	V_{GS} = 3 V	5	mΩ
		V_{GS} = 4.5 V	4	
		V_{GS} = 8 V	3.4	
$V_{GS(th)}$	Threshold Voltage	1.2		V

Device Information(1)

DEVICE	MEDIA	QTY	PACKAGE	SHIP
CSD16327Q3	13-Inch Reel	2500	SON 3.30-mm × 3.30-mm Plastic Package	Tape and Reel
CSD16327Q3T	7-Inch Reel	250		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

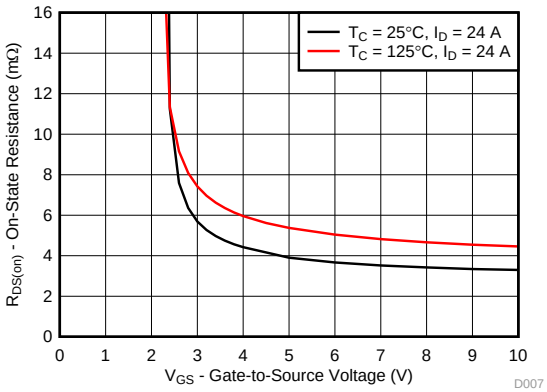
Absolute Maximum Ratings

T_A = 25°C		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	25	V
V_{GS}	Gate-to-Source Voltage	+10 / –8	V
I_D	Continuous Drain Current (Package Limited)	60	A
	Continuous Drain Current (Silicon Limited), T_C = 25°C	112	
	Continuous Drain Current(1)	22	
I_{DM}	Pulsed Drain Current(2)	240	A
P_D	Power Dissipation(1)	2.8	W
	Power Dissipation, T_C = 25°C	74	
T_J, T_{stg}	Operating Junction Temperature, Storage Temperature	–55 to 150	°C
E_{AS}	Avalanche Energy, Single Pulse I_D = 50 A, L = 0.1 mH, R_G = 25 Ω	125	mJ

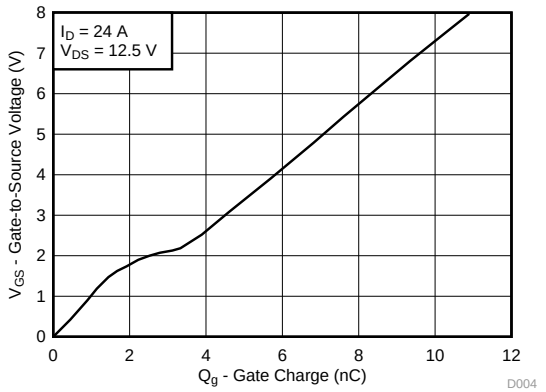
(1) Typical $R_{\theta JA}$ = 45°C/W on 1-in^2 Cu (2 oz) on 0.06-in thick FR4 PCB.

(2) Max $R_{\theta JC}$ = 1.7°C/W pulse width ≤100 µs, duty cycle ≤1%.

$R_{DS(on)}$ vs V_{GS}



Gate Charge



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4 Revision History

Changes from Original (December 2011) to Revision A **Page**

- Added *Device and Documentation Support* section ... 1
- Changed *Description* text ... 1
- Changed I_D Continuos Drain Current from 21 A : to 22 A ... 1
- Changed I_{DM} from 112 A : to 240 A ... 1
- Changed P_D Power Dissipation from 3 W : to 2.8 W ... 1
- Changed Note 2 in *Absolute Maximum Ratings* table ... 1
- Changed $R_{\theta JA}$ from 56°C/W : to 55°C/W ... 3
- Changed Figure 10 to reflect measured data ... 5
- Changed MECHANICAL DATA section to *Mechanical, Packaging, and Orderable Information* section ... 8

5 Specifications

5.1 Electrical Characteristics

T_A = 25°C (unless otherwise stated)

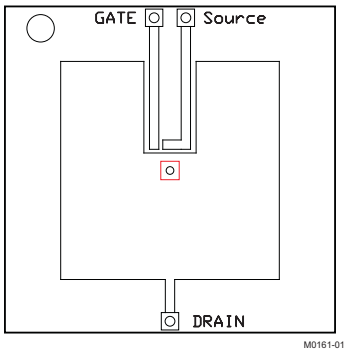
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-source voltage	V_{GS} = 0 V, I_D = 250 μA	25			V
I_{DSS}	Drain-to-source leakage current	V_{GS} = 0 V, V_{DS} = 20 V			1	μA
I_{GSS}	Gate-to-source leakage current	V_{DS} = 0 V, V_{GS} = +10 / –8 V			100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_D = 250 μA	0.9	1.2	1.4	V
$R_{DS(on)}$	Drain-to-source on-resistance	V_{GS} = 3 V, I_D = 24 A		5	6.5	mΩ
		V_{GS} = 4.5 V, I_D = 24 A		4	4.8	
		V_{GS} = 8 V, I_D = 24 A		3.4	4.0	
g_{fs}	Transconductance	V_{DS} = 12.5 V, I_D = 24 A		96		S
DYNAMIC CHARACTERISTICS						
C_{ISS}	Input capacitance	V_{GS} = 0 V, V_{DS} = 12.5 V, f = 1 MHz		1020	1300	pF
C_{OSS}	Output capacitance			740	960	pF
C_{RSS}	Reverse transfer capacitance			50	65	pF
R_g	Series gate resistance			1.4	2.8	Ω
Q_g	Gate charge total (4.5 V)	V_{DS} = 12.5 V, I_D = 24 A		6.2	8.4	nC
Q_{gd}	Gate charge gate-to-drain			1.1		nC
Q_{gs}	Gate charge gate-to-source			1.8		nC
Qg(th)	Gate charge at V_{th}			1		nC
Q_{OSS}	Output charge	V_{DS} = 12.5 V, V_{GS} = 0 V		14		nC
$t_{d(on)}$	Turnon delay time	V_{DS} = 12.5 V, V_{GS} = 4.5 V I_D = 24 A R_G = 2 Ω		5.3		ns
t_r	Rise time			15		ns
$t_{d(off)}$	Turnoff delay time			13		ns
t_f	Fall time			6.3		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	I_S = 24 A, V_{GS} = 0 V		0.85	1	V
Q_{rr}	Reverse recovery charge	V_{DD} = 12.5 V, I_F = 24 A, di/dt = 300 A/μs		21		nC
t_{rr}	Reverse recovery time	V_{DD} = 12.5 V, I_F = 24 A, di/dt = 300 A/μs		16		ns

5.2 Thermal Information

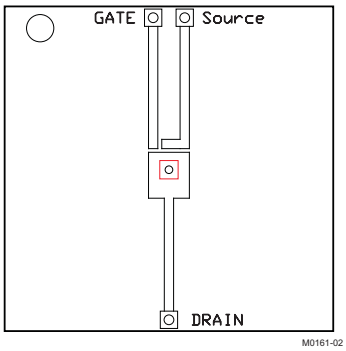
T_A = 25°C (unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-case thermal resistance(1)			1.7	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance(1)(2)			55	°C/W

(1) $R_{\theta JC}$ is determined with the device mounted on a 1-in^2 (6.45-cm^2), 2-oz (0.071-mm) thick Cu pad on a 1.5-in × 1.5-in (3.81-cm × 3.81-cm), 0.06-in (1.52-mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
(2) Device mounted on FR4 material with 1-in^2 (6.45-cm^2), 2-oz (0.071-mm) thick Cu.



Max $R_{\theta JA}$ = 55°C/W when mounted on 1-in^2 (6.45-cm^2) of 2-oz (0.071-mm) thick Cu.



Max $R_{\theta JA}$ = 160°C/W when mounted on a minimum pad area of 2-oz (0.071-mm) thick Cu.

5.3 Typical MOSFET Characteristics

T_A = 25°C (unless otherwise stated)

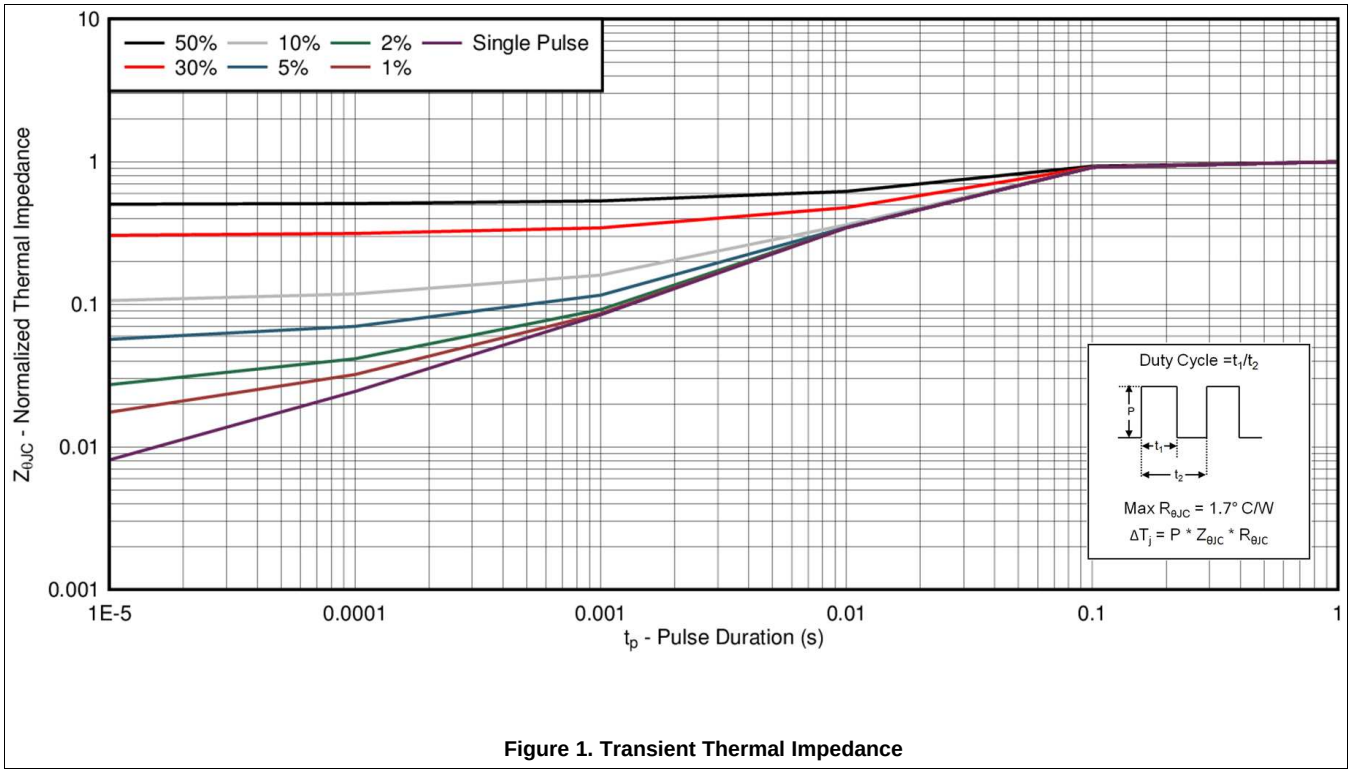


Figure 1. Transient Thermal Impedance

Typical MOSFET Characteristics (continued)

T_A = 25°C (unless otherwise stated)

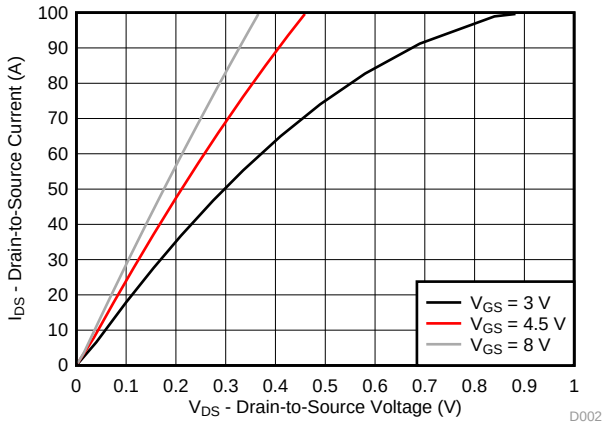
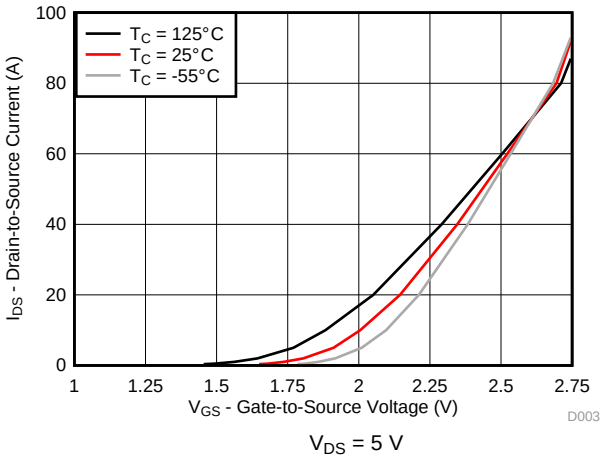
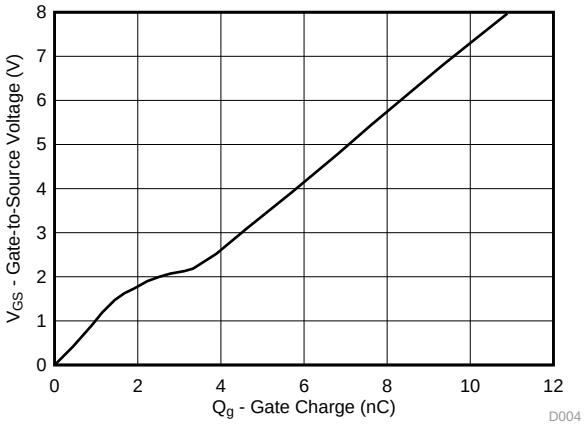


Figure 2. Saturation Characteristics



VDS = 5 V

Figure 3. Transfer Characteristics



ID = 24 A VDS = 12.5 V

Figure 4. Gate Charge

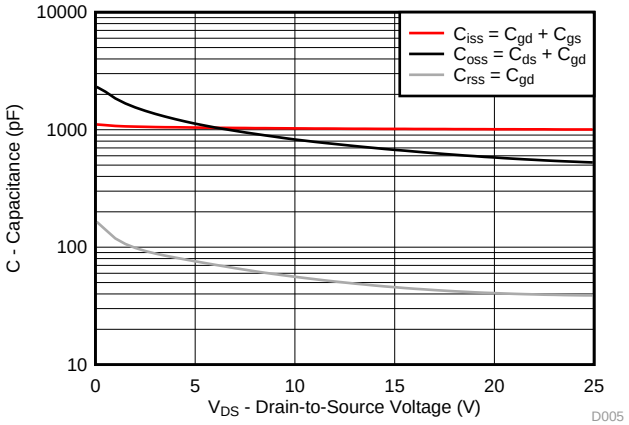
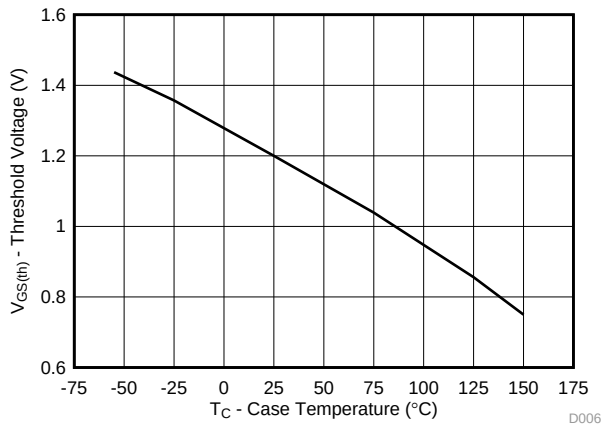


Figure 5. Capacitance



ID = 250 µA

Figure 6. Threshold Voltage vs Temperature

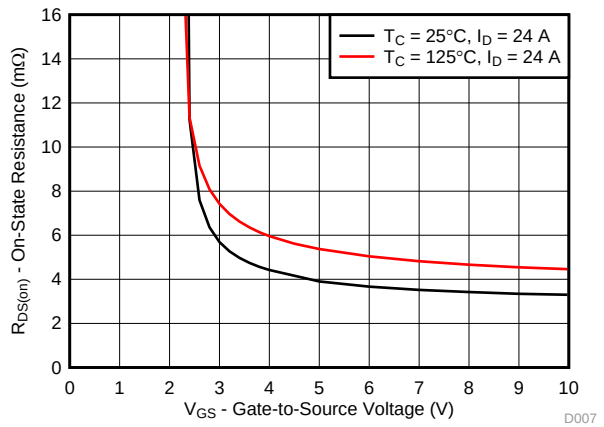


Figure 7. On-State Resistance vs Gate-to-Source Voltage

Typical MOSFET Characteristics (continued)

T_A = 25°C (unless otherwise stated)

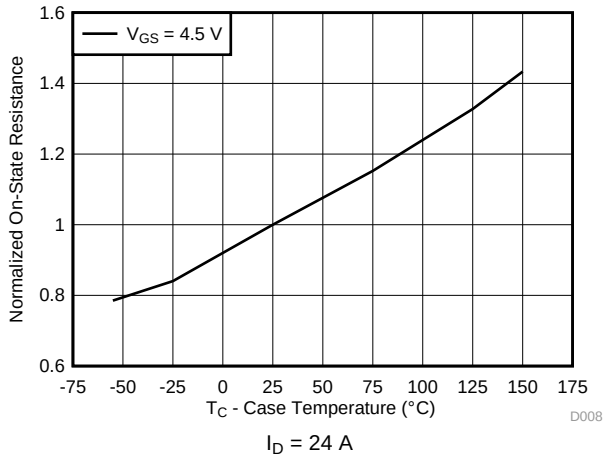


Figure 8. Normalized On-State Resistance vs Temperature

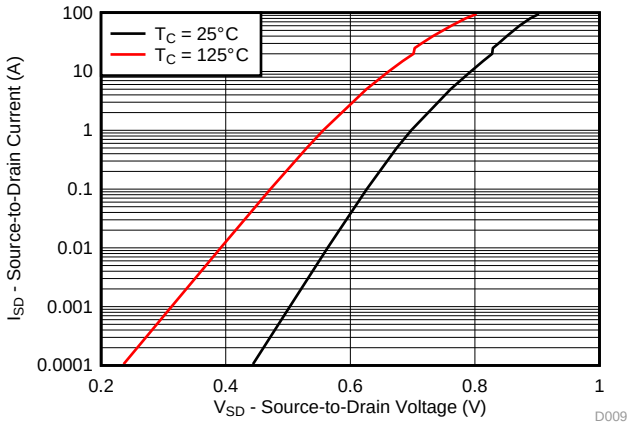


Figure 9. Typical Diode Forward Voltage

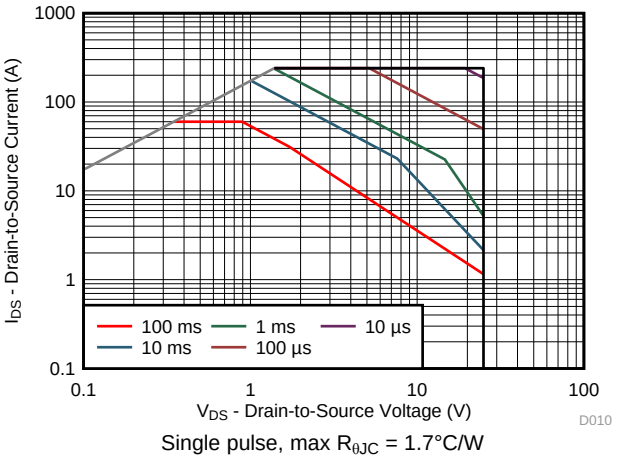


Figure 10. Maximum Safe Operating Area

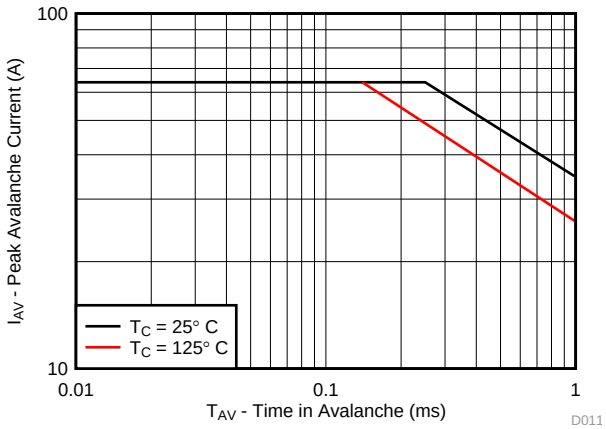


Figure 11. Single Pulse Unclamped Inductive Switching

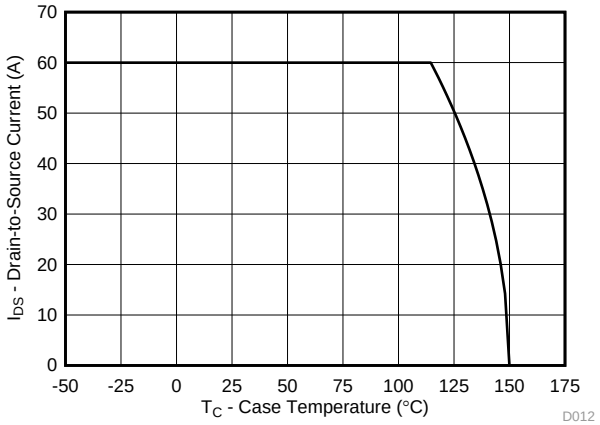


Figure 12. Maximum Drain Current vs Temperature

6 Device and Documentation Support

6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

6.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

6.3 Trademarks

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6.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.5 Glossary

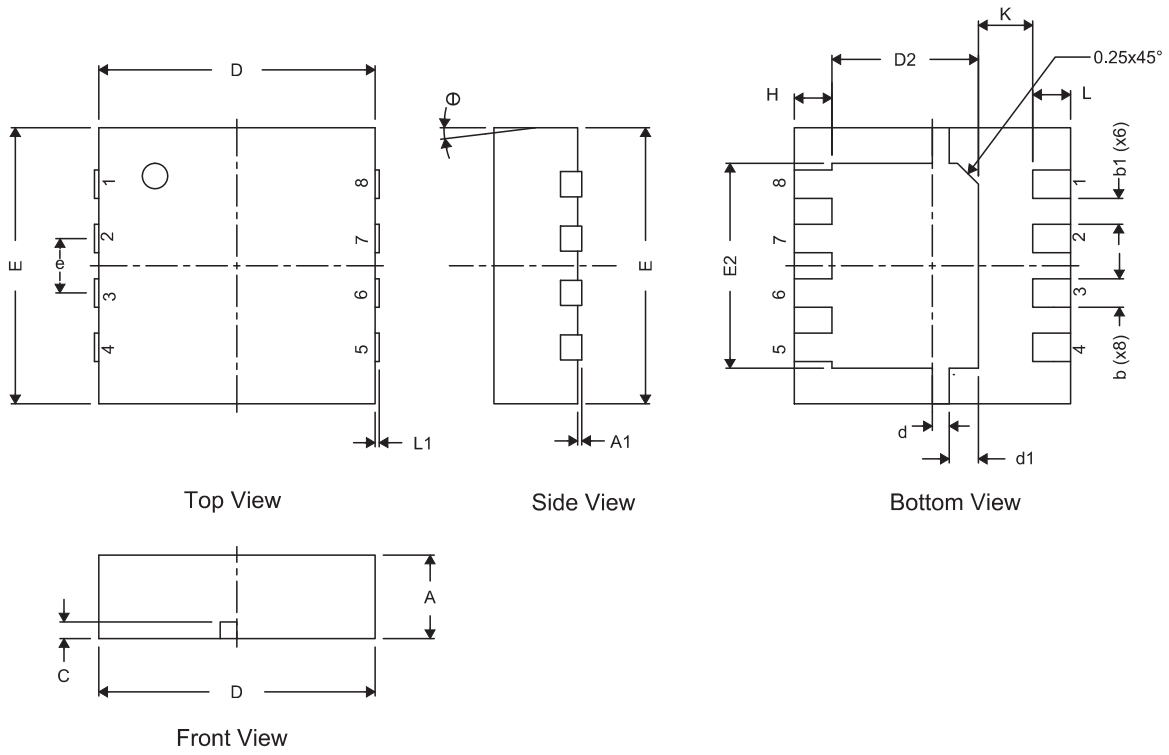
SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 Mechanical, Packaging, and Orderable Information

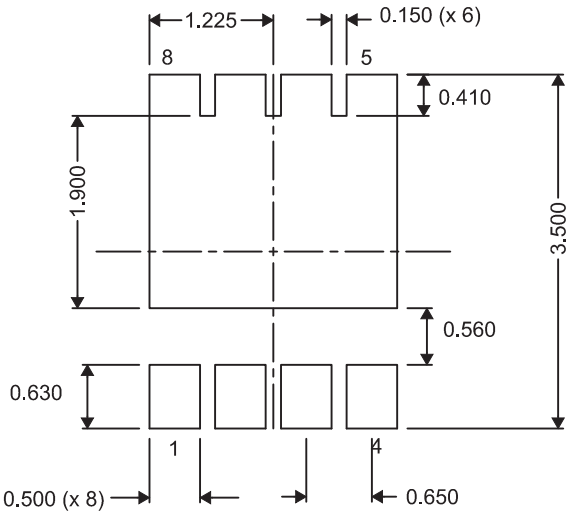
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 Q3 Package Dimensions



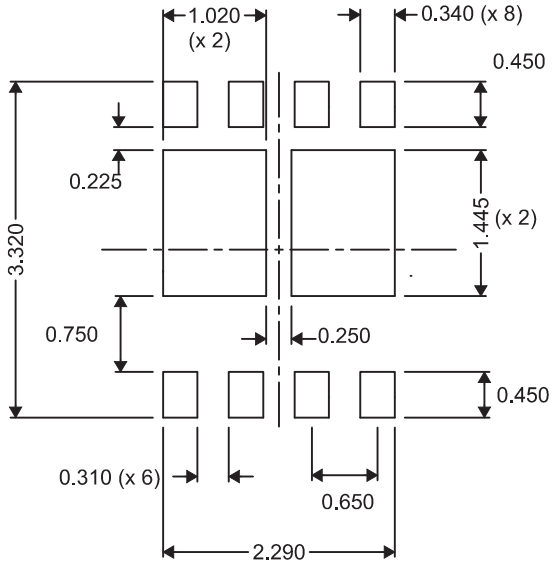
DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.950	1.000	1.100	0.037	0.039	0.043
A1	0.000	0.000	0.050	0.000	0.000	0.002
b	0.280	0.340	0.400	0.011	0.013	0.016
b1		0.310 NOM			0.012 NOM	
c	0.150	0.200	0.250	0.006	0.008	0.010
D	3.200	3.300	3.400	0.126	0.130	0.134
D2	1.650	1.750	1.800	0.065	0.069	0.071
d	0.150	0.200	0.250	0.006	0.008	0.010
d1	0.300	0.350	0.400	0.012	0.014	0.016
E	3.200	3.300	3.400	0.126	0.130	0.134
E2	2.350	2.450	2.550	0.093	0.096	0.100
e		0.650 TYP			0.026 TYP	
H	0.35	0.450	0.550	0.014	0.018	0.022
K		0.650 TYP			0.026 TYP	
L	0.35	0.450	0.550	0.014	0.018	0.022
L1	0	—	0	0	—	0
θ	0	—	0	0	—	0

7.2 Recommended PCB Pattern



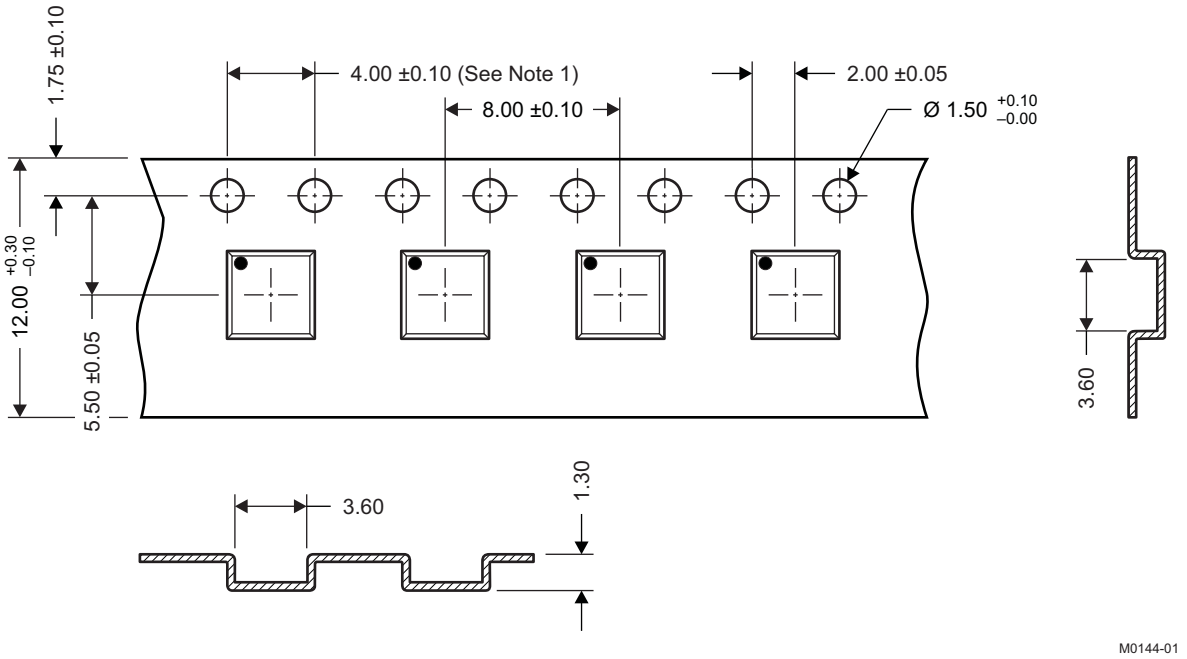
For recommended circuit layout for PCB designs, see *Reducing Ringing Through PCB Layout Techniques* (SLPA005).

7.3 Recommended Stencil Opening



All dimensions are in mm, unless otherwise specified.

7.4 Q3 Tape and Reel Information



Notes:

1. 10-sprocket hole pitch cumulative tolerance ±0.2.
2. Camber not to exceed 1 mm in 100 mm, noncumulative over 250 mm.
3. Material: black static dissipative polystyrene.
4. All dimensions are in mm (unless otherwise specified).
5. Thickness: 0.30 ±0.05 mm.
6. MSL1 260°C (IR and Convection) PbF-Reflow Compatible.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD16327Q3	ACTIVE	VSON-CLIP	DQG	8	2500	Pb-Free (RoHS Exempt)	CU SN	Level-1-260C-UNLIM	-55 to 150	CSD16327	Samples
CSD16327Q3T	ACTIVE	VSON-CLIP	DQG	8	250	Pb-Free (RoHS Exempt)	CU SN	Level-1-260C-UNLIM	-55 to 150	CSD16327	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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