DS25BR120 3.125 Gbps LVDS Buffer with Transmit Pre-Emphasis

Check for Samples: DS25BR120

FEATURES

- **DC - 3.125 Gbps Low Jitter, High Noise Immunity, Low Power Operation**
- **Four Levels of Transmit Pre-Emphasis Drive Lossy Backplanes and Cables**
- **On-Chip 100Ω Input and Output Termination Minimizes Insertion and Return Losses, Reduces Component Count, and Minimizes Board Space**
- **7 kV ESD on LVDS I/O pins Protects Adjoining Components**
- **Small 3 mm x 3 mm 8-WSON Space Saving Package**

APPLICATIONS

- **Clock and Data Buffering**
- **Metallic Cable Driving**
- **FR-4 Driving**

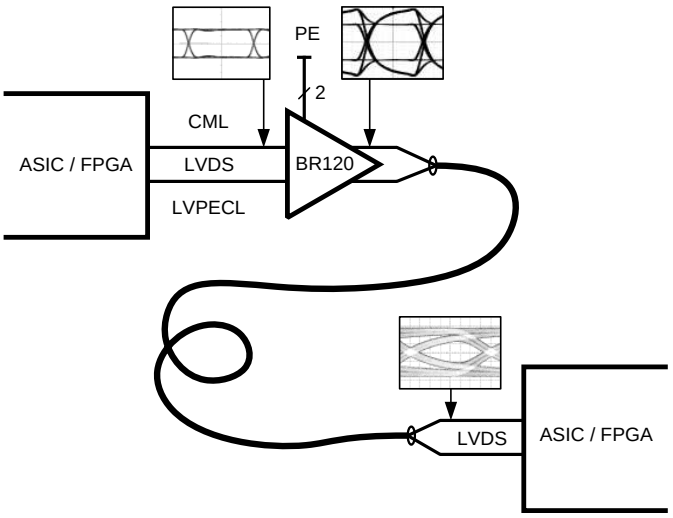
DESCRIPTION

The DS25BR120 is a single channel 3.125 Gbps LVDS buffer optimized for high-speed signal transmission over lossy FR-4 printed circuit board backplanes and balanced metallic cables. Fully differential signal paths ensure exceptional signal integrity and noise immunity.

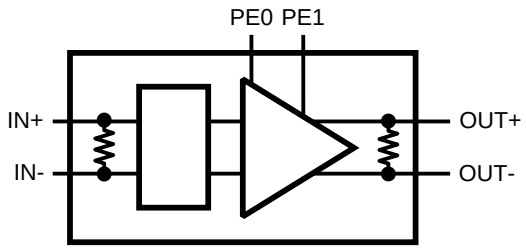
The DS25BR120 features four levels of pre-emphasis (PE) for use as an optimized driver device. Other LVDS devices with similar IO characteristics include the following products. The DS25BR110 features four levels of equalization for use as an optimized receiver device, while the DS25BR100 features both pre-emphasis and equalization for use as an optimized repeater device. The DS25BR150 is a buffer/repeater with the lowest power consumption and does not feature transmit pre-emphasis nor receive equalization.

Wide input common mode range allows the receiver to accept signals with LVDS, CML and LVPECL levels; the output levels are LVDS. A very small package footprint requires minimal space on the board while the flow-through pinout allows easy board layout. The differential inputs and outputs are internally terminated with a 100Ω resistor to lower device input and output return losses, reduce component count and further minimize board space.

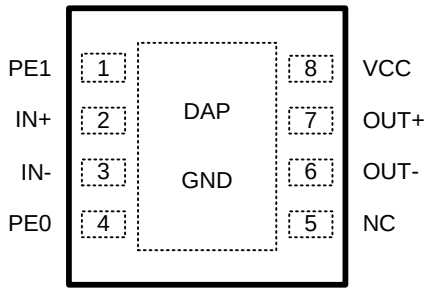
Typical Application



Block Diagram



Pin Diagram



WSON Package

PIN DESCRIPTIONS

Pin Name	Pin Name	Pin Type	Pin Description
PE1	1	Input	Pre-emphasis select pin.
IN+	2	Input	Non-inverting LVDS input pin.
IN-	3	Input	Inverting LVDS input pin.
PE0	4	Input	Pre-emphasis select pin.
NC	5	NA	"NO CONNECT" pin.
OUT-	6	Output	Inverting LVDS output pin.
OUT+	7	Output	Non-inverting LVDS Output pin.
VCC	8	Power	Power supply pin.
GND	DAP	Power	Ground pad (DAP - die attach pad)

Pre-Emphasis Truth Table

PE1	PE0	Pre-emphasis Level
0	0	Off
0	1	Low (Approx. 3 dB at 1.56 GHz)
1	0	Medium (Approx. 6 dB at 1.56 GHz)
1	1	High (Approx. 9 dB at 1.56 GHz)

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1][2]

Supply Voltage (V_{CC})	−0.3V to +4V
LVCMOS Input Voltage (PE0, PE1)	−0.3V to (V_{CC} + 0.3V)
LVDS Input Voltage (IN+, IN−)	−0.3V to +4V
Differential Input Voltage |VID|	1.0V
LVDS Output Voltage (OUT+, OUT−)	−0.3V to (V_{CC} + 0.3V)
LVDS Differential Output Voltage ((OUT+) - (OUT−))	0V to 1.0V
LVDS Output Short Circuit Current Duration	5 ms
Junction Temperature	+150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature Range	
Soldering (4 sec.)	+260°C
Maximum Package Power Dissipation at 25°C	
NGQ Package	2.08W
Derate NGQ Package	16.7 mW/°C above +25°C
Package Thermal Resistance	
θ_{JA}	+60.0°C/W
θ_{JC}	+12.3°C/W
ESD Susceptibility	
HBM[3]	≥7 kV
MM[4]	≥250V
CDM[5]	≥1250V

(1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
(3) Human Body Model, applicable std. JESD22-A114C
(4) Machine Model, applicable std. JESD22-A115-A
(5) Field Induced Charge Device Model, applicable std. JESD22-C101-C

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	3.0	3.3	3.6	V
Receiver Differential Input Voltage (V_{ID})	0		1.0	V
Operating Free Air Temperature (T_A)	−40	+25	+85	°C

Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.[1][2][3]

Symbol	Parameter	Conditions	Min	Typ	Max	Units
LVCMOS INPUT DC SPECIFICATIONS (PE0, PE1)						
V_{IH}	High Level Input Voltage		2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage		GND		0.8	V
I_{IH}	High Level Input Current	V_{IN} = 3.6V V_{CC} = 3.6V		0	±10	µA
I_{IL}	Low Level Input Current	V_{IN} = GND V_{CC} = 3.6V		0	±10	µA

(1) The Electrical Characteristics tables list ensured specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not ensured.
(2) Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except V_{OD} and ΔV_{OD}.
(3) Typical values represent most likely parametric norms for V_{CC} = +3.3V and T_A = +25°C, and at the Recommended Operation Conditions at the time of product characterization and are not ensured.

Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.(1)(2)(3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA, V_{CC} = 0V		-0.9	−1.5	V
LVDS OUTPUT DC SPECIFICATIONS (OUT+, OUT-)						
V_{OD}	Differential Output Voltage	R_L = 100Ω	250	350	450	mV
ΔV_{OD}	Change in Magnitude of V_{OD} for Complimentary Output States		-35		35	mV
V_{OS}	Offset Voltage	R_L = 100Ω	1.05	1.2	1.375	V
ΔV_{OS}	Change in Magnitude of V_{OS} for Complimentary Output States		-35		35	mV
I_{OS}	Output Short Circuit Current(4)	OUT to GND PE0 = PE1 = 0		-35	-55	mA
		OUT to V_{CC} PE0 = PE1 = 0		7	55	mA
C_{OUT}	Output Capacitance	Any LVDS Output Pin to GND		1.2		pF
R_{OUT}	Output Termination Resistor	Between OUT+ and OUT-		100		Ω
LVDS INPUT DC SPECIFICATIONS (IN+, IN-)						
V_{ID}	Input Differential Voltage		0		1	V
V_{TH}	Differential Input High Threshold	V_{CM} = +0.05V or V_{CC}-0.05V		0	+100	mV
V_{TL}	Differential Input Low Threshold		−100	0		mV
V_{CMR}	Common Mode Voltage Range	V_{ID} = 100 mV	0.05		V_{CC} - 0.05	V
I_{IN}	Input Current	V_{IN} = 3.6V or 0V V_{CC} = 3.6V or 0V		±1	±10	µA
C_{IN}	Input Capacitance	Any LVDS Input Pin to GND		1.7		pF
R_{IN}	Input Termination Resistor	Between IN+ and IN-		100		Ω
SUPPLY CURRENT						
I_{CC}	Supply Current	PE0 = 0, PE1 = 0		35	43	mA

(4) Output short circuit current (I_{OS}) is specified as magnitude only, minus sign indicates direction only.

AC Electrical Characteristics(1)

Over recommended operating supply and temperature ranges unless otherwise specified.(2)(3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
LVDS OUTPUT AC SPECIFICATIONS (OUT+, OUT-)						
t_{PHLD}	Differential Propagation Delay High to Low	R_L = 100Ω		350	465	ps
t_{PLHD}	Differential Propagation Delay Low to High			350	465	ps
t_{SKD1}	Pulse Skew $\lvert t_{PLHD} - t_{PHLD} \rvert$(4)			45	100	ps
t_{SKD2}	Part to Part Skew(5)			45	150	ps
t_{LHT}	Rise Time	R_L = 100Ω		80	150	ps
t_{HLT}	Fall Time			80	150	ps

(1) Specification is ensured by characterization and is not tested in production.
(2) The Electrical Characteristics tables list ensured specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not ensured.
(3) Typical values represent most likely parametric norms for V_{CC} = +3.3V and T_A = +25°C, and at the Recommended Operation Conditions at the time of product characterization and are not ensured.
(4) t_{SKD1}, $\lvert t_{PLHD} - t_{PHLD} \rvert$, is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.
(5) t_{SKD2}, Part to Part Skew, is defined as the difference between the minimum and maximum specified differential propagation delays. This specification applies to devices at the same V_{CC} and within 5°C of each other within the operating temperature range.

AC Electrical Characteristics[1] (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.[2][3]

Symbol	Parameter	Conditions		Min	Typ	Max	Units
JITTER PERFORMANCE WITH PE = OFF							
t_{RJ1A}	Random Jitter (RMS Value) No Test Channels [6]	V_{ID} = 350 mV, V_{CM} = 1.2V, Clock (RZ), PE0 = 0, PE1 = 0	2.5 Gbps		0.5	1	ps
t_{RJ2A}			3.125 Gbps		0.5	1	ps
t_{DJ1A}	Deterministic Jitter (Peak to Peak) No Test Channels [7]	V_{ID} = 350 mV, V_{CM} = 1.2V, K28.5 (NRZ), PE0 = 0, PE1 = 0	2.5 Gbps		9	31	ps
t_{DJ2A}			3.125 Gbps		16	40	ps
t_{TJ1A}	Total Jitter (Peak to Peak) No Test Channels [8]	V_{ID} = 350 mV, V_{CM} = 1.2V, PRBS-23 (NRZ), PE0 = 0, PE1 = 0	2.5 Gbps		0.05	0.13	UI_{P-P}
t_{TJ2A}			3.125 Gbps		0.09	0.16	UI_{P-P}
JITTER PERFORMANCE WITH PE = LOW (Figure 5 and Figure 6)							
t_{RJ1B}	Random Jitter (RMS Value) Test Channel A [6]	V_{ID} = 350 mV, V_{CM} = 1.2V, Clock (RZ), PE0 = 1, PE1 = 0	2.5 Gbps		0.5	1.3	ps
t_{RJ2B}			3.125 Gbps		0.5	1.3	ps
t_{DJ1B}	Deterministic Jitter (Peak to Peak) Test Channel A [7]	V_{ID} = 350 mV, V_{CM} = 1.2V, K28.5 (NRZ), PE0 = 1, PE1 = 0	2.5 Gbps		17	31	ps
t_{DJ2B}			3.125 Gbps		18	40	ps
t_{TJ1B}	Total Jitter (Peak to Peak) Test Channel A [8]	V_{ID} = 350 mV, V_{CM} = 1.2V, PRBS-23 (NRZ), PE0 = 1, PE1 = 0	2.5 Gbps		0.09	0.14	UI_{P-P}
t_{TJ2B}			3.125 Gbps		0.12	0.19	UI_{P-P}
JITTER PERFORMANCE WITH PE = MEDIUM (Figure 5 and Figure 6)							
t_{RJ1C}	Random Jitter (RMS Value) Test Channel B [6]	V_{ID} = 350 mV, V_{CM} = 1.2V, Clock (RZ), PE0 = 0, PE1 = 1	2.5 Gbps		0.5	1.2	ps
t_{RJ2C}			3.125 Gbps		0.5	1.2	ps
t_{DJ1C}	Deterministic Jitter (Peak to Peak) Test Channel B [7]	V_{ID} = 350 mV, V_{CM} = 1.2V, K28.5 (NRZ), PE0 = 0, PE1 = 1	2.5 Gbps		21	44	ps
t_{DJ2C}			3.125 Gbps		27	48	ps
t_{TJ1C}	Total Jitter (Peak to Peak) Test Channel B [8]	V_{ID} = 350 mV, V_{CM} = 1.2V, PRBS-23 (NRZ), PE0 = 0, PE1 = 1	2.5 Gbps		0.09	0.16	UI_{P-P}
t_{TJ2C}			3.125 Gbps		0.13	0.23	UI_{P-P}
JITTER PERFORMANCE WITH PE = HIGH (Figure 5 and Figure 6)							
t_{RJ1D}	Random Jitter (RMS Value) Test Channel C [6]	V_{ID} = 350 mV, V_{CM} = 1.2V, Clock (RZ), PE0 = 1, PE1 = 1	2.5 Gbps		0.5	1.2	ps
t_{RJ2D}			3.125 Gbps		0.5	1.2	ps
t_{DJ1D}	Deterministic Jitter (Peak to Peak) Test Channel C [7]	V_{ID} = 350 mV, V_{CM} = 1.2V, K28.5 (NRZ), PE0 = 1, PE1 = 1	2.5 Gbps		30	65	ps
t_{DJ2D}			3.125 Gbps		30	58	ps
t_{TJ1D}	Total Jitter (Peak to Peak) Test Channel C [8]	V_{ID} = 350 mV, V_{CM} = 1.2V, PRBS-23 (NRZ), PE0 = 1, PE1 = 1	2.5 Gbps		0.09	0.20	UI_{P-P}
t_{TJ2D}			3.125 Gbps		0.13	0.22	UI_{P-P}

(6) Measured on a clock edge with a histogram and an accumulation of 1500 histogram hits. Input stimulus jitter is subtracted geometrically.
(7) Tested with a combination of the 1100000101 (K28.5+ character) and 0011111010 (K28.5- character) patterns. Input stimulus jitter is subtracted algebraically.
(8) Measured on an eye diagram with a histogram and an accumulation of 3500 histogram hits. Input stimulus jitter is subtracted.

APPLICATION INFORMATION

DC TEST CIRCUITS

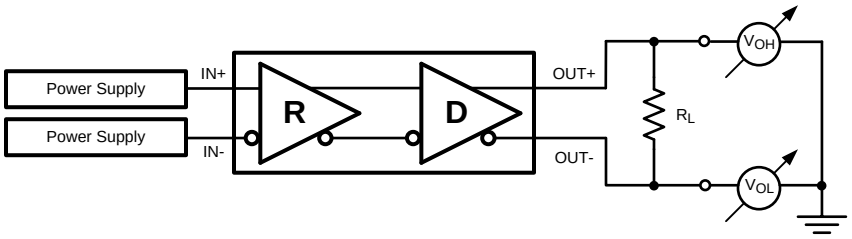


Figure 1. Differential Driver DC Test Circuit

AC TEST CIRCUITS AND TIMING DIAGRAMS

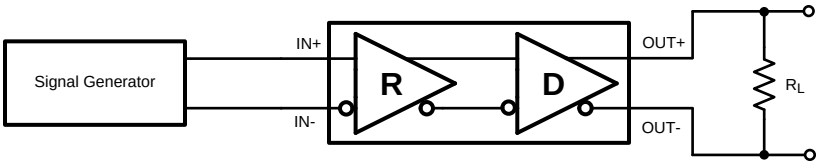


Figure 2. Differential Driver AC Test Circuit

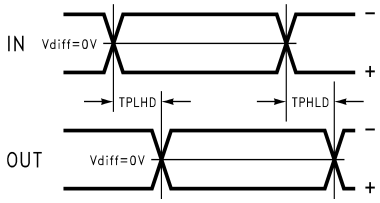


Figure 3. Propagation Delay Timing Diagram

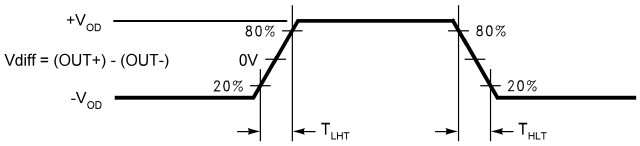


Figure 4. LVDS Output Transition Times

PRE-EMPHASIS TEST CIRCUITS

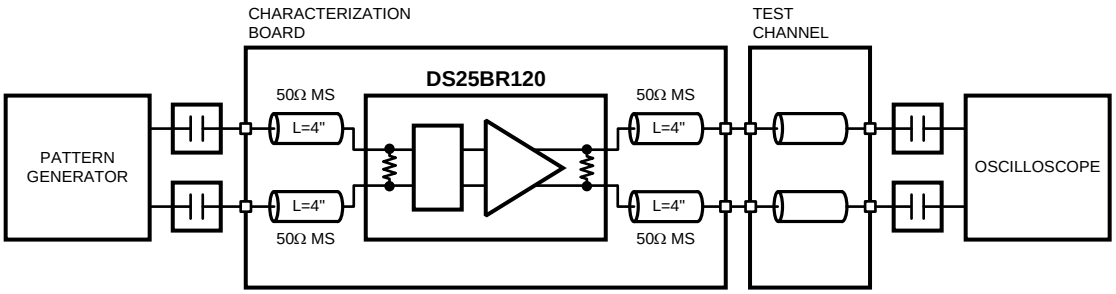


Figure 5. Pre-emphasis Performance Test Circuit

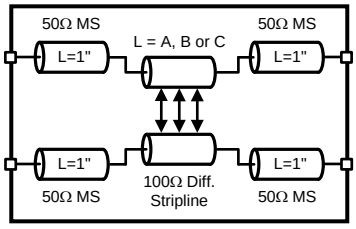


Figure 6. Test Channel Description

Test Channel Loss Characteristics

The test channel was fabricated with Polyclad PCL-FR-370-Laminate/PCL-FRP-370 Prepreg materials (Dielectric constant of 3.7 and Loss Tangent of 0.02). The edge coupled differential striplines have the following geometries: Trace Width (W) = 5 mils, Gap (S) = 5 mils, Height (B) = 16 mils.

Test Channel	Length (inches)	Insertion Loss (dB)					
		500 MHz	750 MHz	1000 MHz	1250 MHz	1500 MHz	1560 MHz
A	10	-1.2	-1.7	-2.0	-2.4	-2.7	-2.8
B	20	-2.6	-3.5	-4.1	-4.8	-5.5	-5.6
C	30	-4.3	-5.7	-7.0	-8.2	-9.4	-9.7
D	15	-1.6	-2.2	-2.7	-3.2	-3.7	-3.8
E	30	-3.4	-4.5	-5.6	-6.6	-7.7	-7.9
F	60	-7.8	-10.3	-12.4	-14.5	-16.6	-17.0

Device Operation

INPUT INTERFACING

The DS25BR120 accepts differential signals and allows simple AC or DC coupling. With a wide common mode range, the DS25BR120 can be DC-coupled with all common differential drivers (i.e. LVPECL, LVDS, CML). The following three figures illustrate typical DC-coupled interface to common differential drivers. Note that the DS25BR120 inputs are internally terminated with a 100Ω resistor.

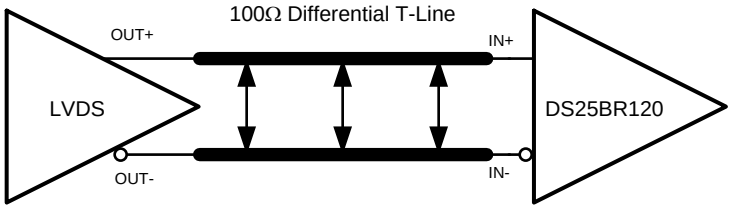


Figure 7. Typical LVDS Driver DC-Coupled Interface to DS25BR120 Input

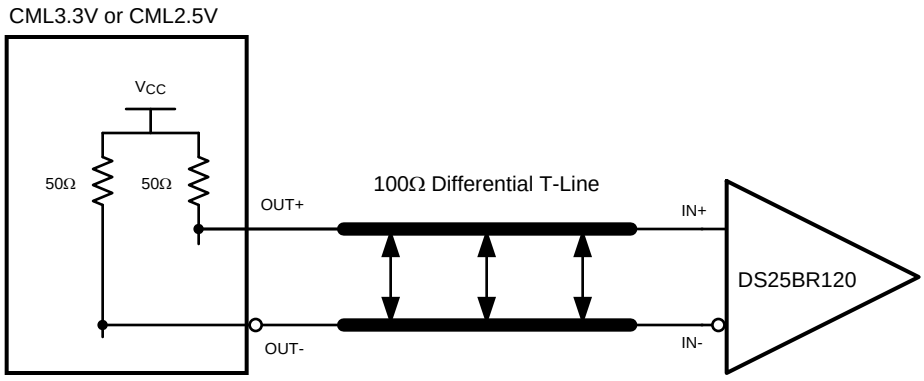


Figure 8. Typical CML Driver DC-Coupled Interface to DS25BR120 Input

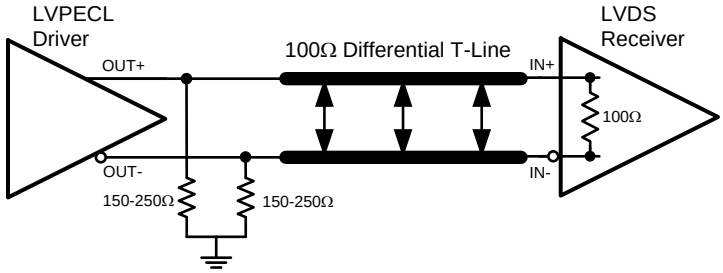


Figure 9. Typical LVPECL Driver DC-Coupled Interface to DS25BR120 Input

OUTPUT INTERFACING

The DS25BR120 outputs signals compliant to the LVDS standard. It can be DC-coupled to most common differential receivers. The following figure illustrates typical DC-coupled interface to common differential receivers and assumes that the receivers have high impedance inputs. While most differential receivers have a common mode input range that can accommodate LVDS compliant signals, it is recommended to check the respective receiver's datasheet prior to implementing the suggested interface implementation.

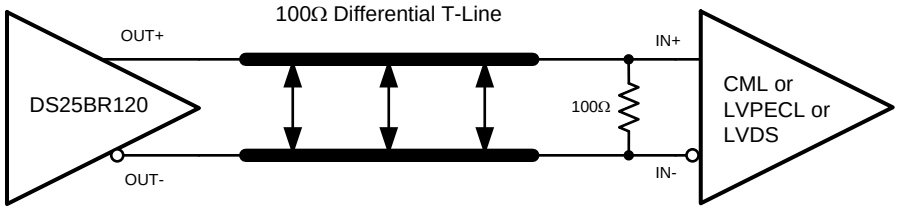


Figure 10. Typical DS25BR120 Output DC-Coupled Interface to an LVDS, CML or LVPECL Receiver

TYPICAL PERFORMANCE CHARACTERISTICS

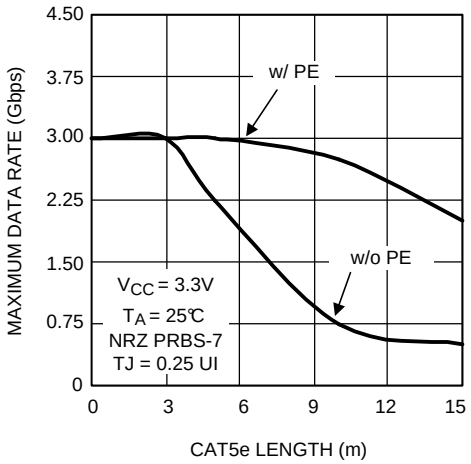


Figure 11. Maximum Data Rate as a Function of CAT5e (Belden 1700A) Length

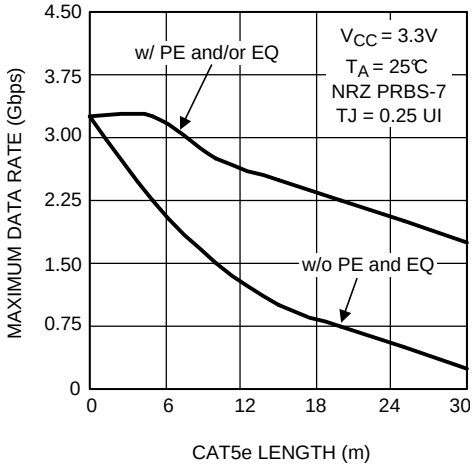


Figure 12. Maximum Data Rate as a Function of CAT5e (Belden 1700A) Length DS25BR120 Used as a Driver DS25BR110 Used as a Receiver

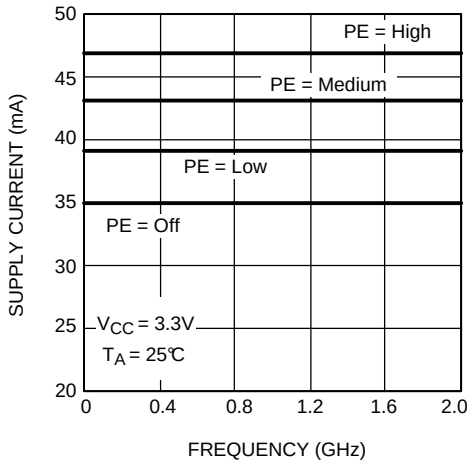


Figure 13. Power Supply Current as a Function of Frequency

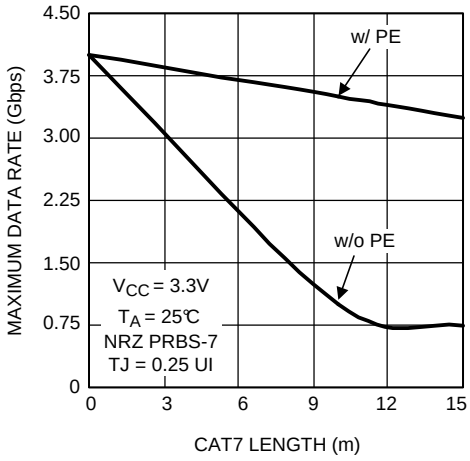


Figure 14. Maximum Data Rate as a Function of CAT7 (Siemon Tera) Length

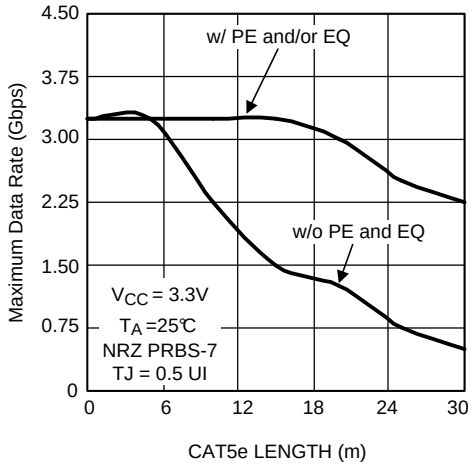


Figure 15. Maximum Data Rate as a Function of CAT5e (Belden 1700A) Length DS25BR120 Used as a Driver DS25BR110 Used as a Receiver

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

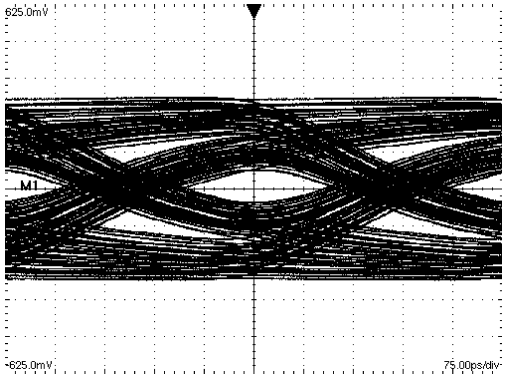


Figure 16. A 2.5 Gbps NRZ PRBS-7 After 40" Differential FR-4 Stripline V:125 mV / DIV, H:75 ps / DIV

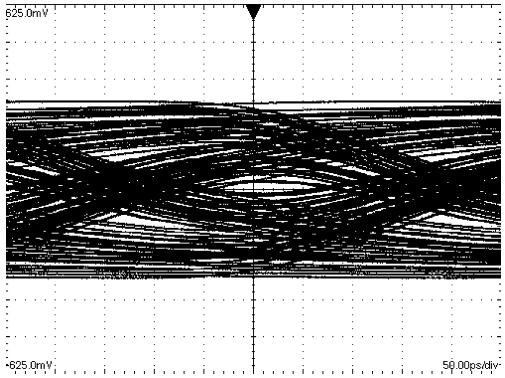


Figure 17. A 3.125 Gbps NRZ PRBS-7 After 40" Differential FR-4 Stripline V:125 mV / DIV, H:50 ps / DIV

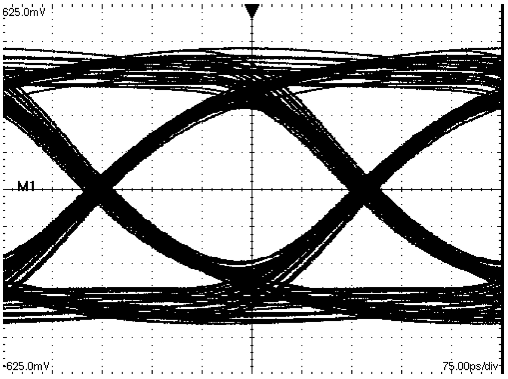


Figure 18. An Equalized (with PE) 2.5 Gbps NRZ PRBS-7 After 40" Differential FR-4 Stripline V:125 mV / DIV, H:75 ps / DIV

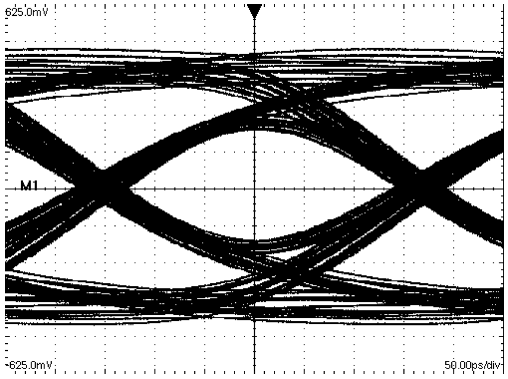


Figure 19. An Equalized (with PE) 3.125 Gbps NRZ PRBS-7 After 40" Differential FR-4 Stripline V:125 mV / DIV, H:50 ps / DIV

REVISION HISTORY

Changes from Revision D (April 2013) to Revision E	Page
• Changed layout of National Data Sheet to TI format	10

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS25BR120TSD/NOPB	ACTIVE	WSON	NGQ	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	2R120	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

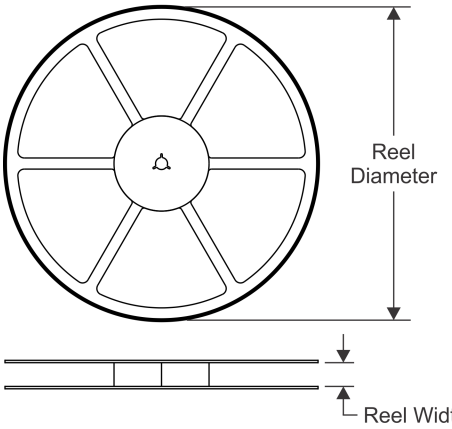
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

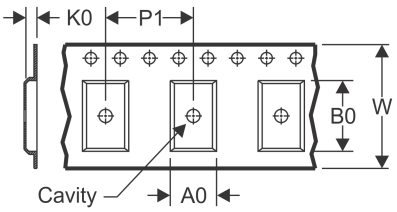
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

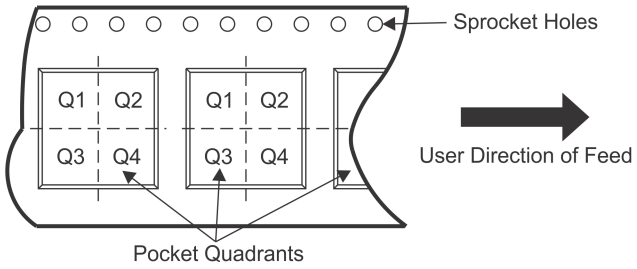


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

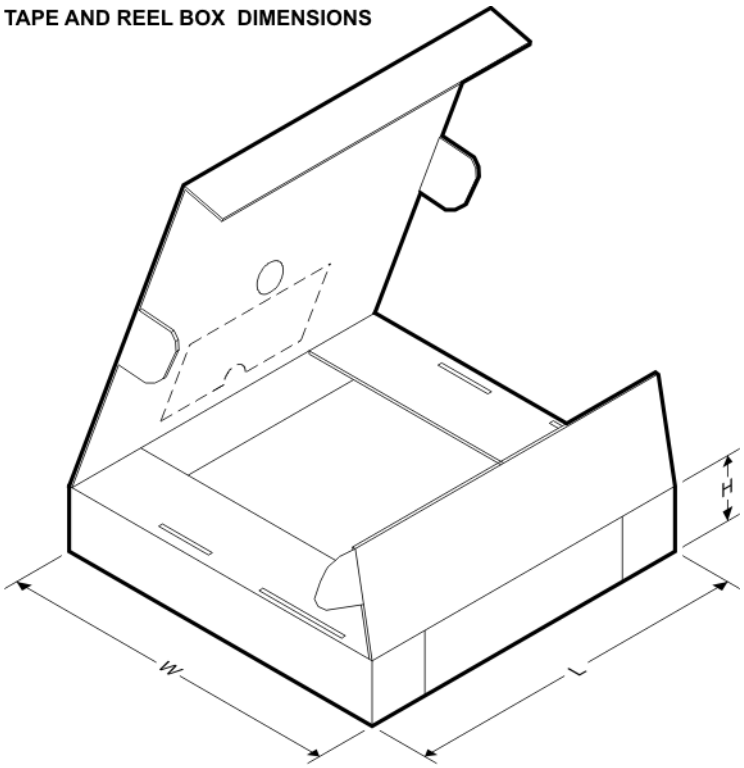
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS25BR120TSD/NOPB	WSON	NGQ	8	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

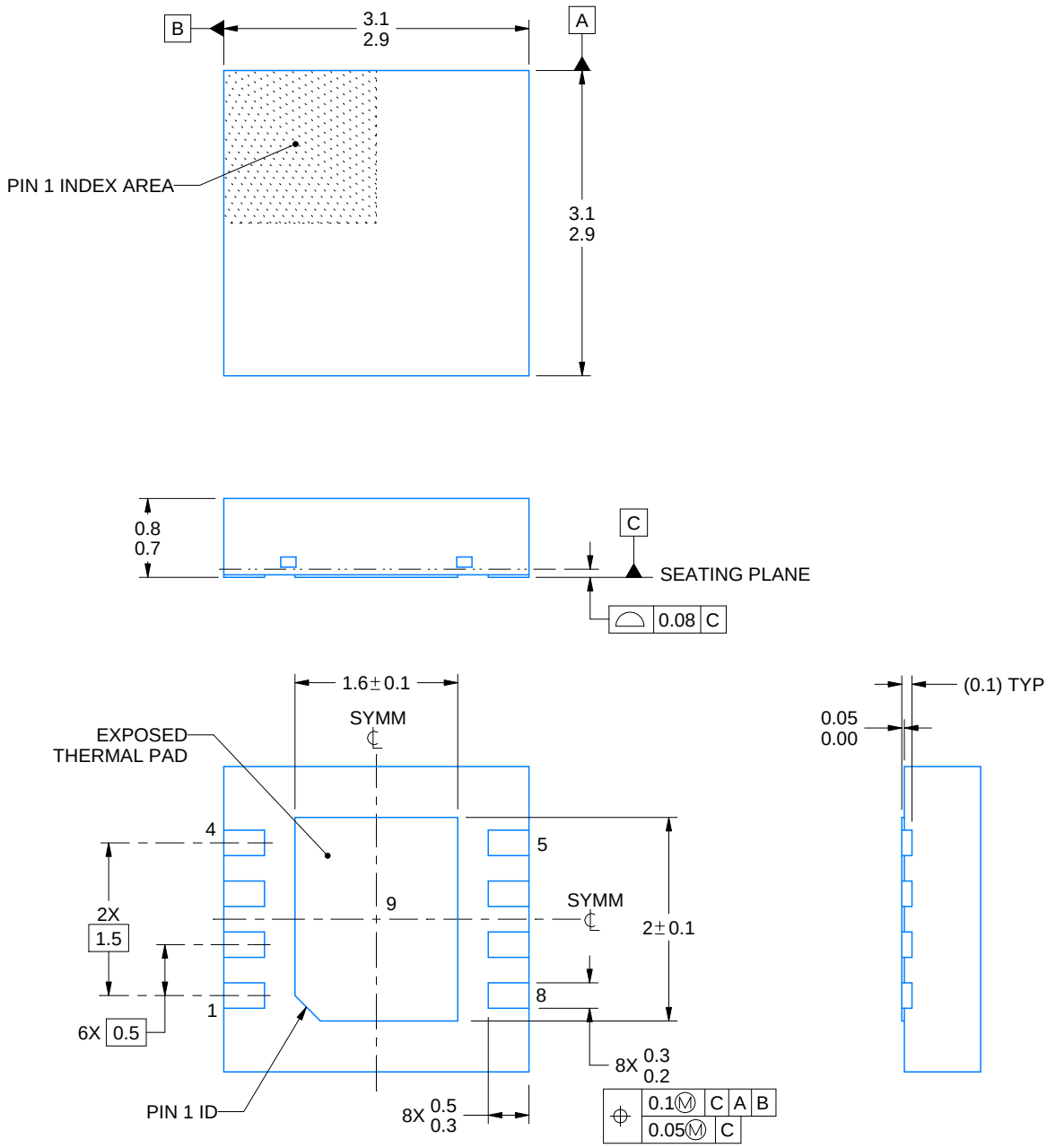
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS25BR120TSD/NOPB	WSON	NGQ	8	1000	210.0	185.0	35.0

PACKAGE OUTLINE

NGQ0008A

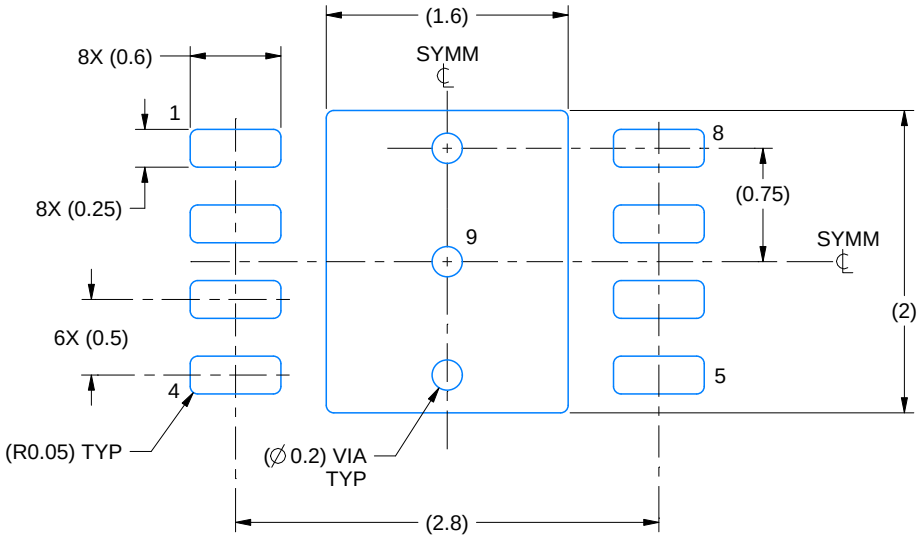
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

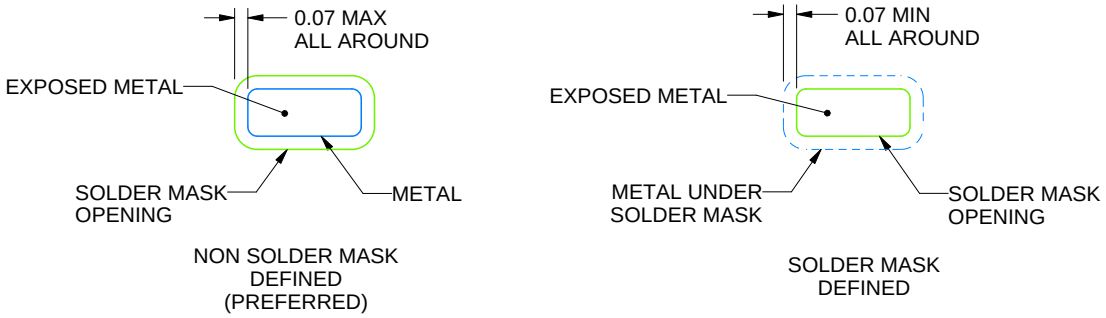


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

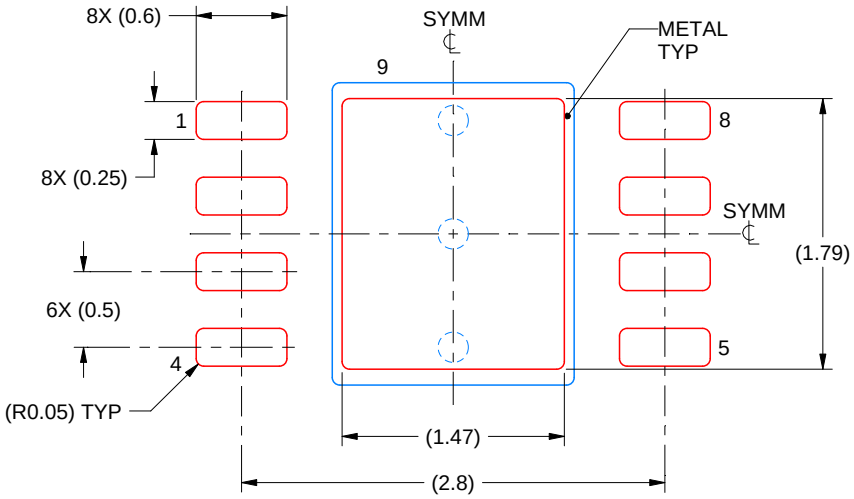


SOLDER MASK DETAILS

4214922/A 03/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 9:
82% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4214922/A 03/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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