## DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC


## HEF4104B MSI <br> Quadruple low to high voltage translator with 3-state outputs

Product specification
File under Integrated Circuits, IC04

PHILIPS

## DESCRIPTION

The HEF4104B quadruple low voltage to high voltage translator with 3-state outputs provides the capability of interfacing low voltage circuits to high voltage circuits, such as low voltage LOCMOS and TTL to high voltage LOCMOS. It has four data inputs ( $\mathrm{I}_{0}$ to $\mathrm{I}_{3}$ ), an active HIGH output enable input (EO), four data outputs $\left(\mathrm{O}_{0}\right.$ to $\left.\mathrm{O}_{3}\right)$ and their complements ( $\overline{\mathrm{O}}_{0}$ to $\overline{\mathrm{O}}_{3}$ ).

With EO $\mathrm{HIGH}, \mathrm{O}_{0}$ to $\mathrm{O}_{3}$ and $\overline{\mathrm{O}}_{0}$ to $\overline{\mathrm{O}}_{3}$ are in the low impedance ON -state, either HIGH or LOW as determined by $\mathrm{I}_{0}$ to $\mathrm{I}_{3}$; with EO LOW, $\mathrm{O}_{0}$ to $\mathrm{O}_{3}$ and $\overline{\mathrm{O}}_{0}$ to $\overline{\mathrm{O}}_{3}$ are in the high impedance OFF-state.

The device uses a common negative supply ( $\mathrm{V}_{\mathrm{SS}}$ ) and separate positive supplies for inputs ( $\mathrm{V}_{\mathrm{DII}}$ ) and outputs $\left(\mathrm{V}_{\mathrm{DDO}}\right)$. $\mathrm{V}_{\mathrm{DDI}}$ must always be less than or equal to $\mathrm{V}_{\mathrm{DDO}}$, even during power turn-on and turn-off. For the permissible operating range of $\mathrm{V}_{\mathrm{DDI}}$ and $\mathrm{V}_{\mathrm{DDO}}$ see graph Fig. 4.
Each input protection circuit is terminated between $\mathrm{V}_{\mathrm{DDO}}$ and $\mathrm{V}_{\mathrm{SS}}$. This allows the input signals to be driven from any potential between $\mathrm{V}_{\mathrm{DDO}}$ and $\mathrm{V}_{\mathrm{SS}}$, without regard to current limiting. When driving from potentials greater than $\mathrm{V}_{\text {DDO }}$ or less than $\mathrm{V}_{\mathrm{SS}}$, the current at each input must be limited to 10 mA .


Fig. 2 Pinning diagram.

HEF4104BP(N): 16-lead DIL; plastic
(SOT38-1)
HEF4104BD(F): 16-lead DIL; ceramic (cerdip)
(SOT74)
HEF4104BT(D): 16-lead SO; plastic
(SOT109-1)
( ): Package Designator North America

PINNING

| $\mathrm{I}_{0}$ to $\mathrm{I}_{3}$ | data inputs |
| :--- | :--- |
| EO | output enable input |
| $\mathrm{O}_{0}$ to $\mathrm{O}_{3}$ | data outputs |
| $\overline{\mathrm{O}}_{0}$ to $\overline{\mathrm{O}}_{3}$ | complementary data outputs |

## FAMILY DATA, IDD LIMITS category MSI

See Family Specifications

Quadruple low to high voltage translator


Fig. 3 Logic diagram.

## Quadruple low to high voltage translator

## AC CHARACTERISTICS

$\mathrm{V}_{\mathrm{SS}}=0 \mathrm{~V} ; \mathrm{T}_{\mathrm{amb}}=25^{\circ} \mathrm{C} ; \mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}$; input transition times $\leq 20 \mathrm{~ns}$


|  | $\mathrm{V}_{\mathrm{DD}}$ | TYPICAL FORMULA FOR P ( $\mu \mathrm{W}$ ) |  |
| :---: | :---: | :---: | :---: |
| Dynamic power dissipation per package (P) | $\begin{array}{r} 5 \\ 10 \\ 15 \end{array}$ | $\begin{array}{r} 3000 f_{i}+\sum\left(f_{0} C_{L}\right) \times V_{D D^{2}} \\ 12200 f_{i}+\sum\left(f_{o} C_{L}\right) \times V_{D D^{2}} \\ 31000 f_{i}+\sum\left(f_{o} C_{L}\right) \times V_{D D^{2}} \end{array}$ | where <br> $\mathrm{f}_{\mathrm{i}}=$ input freq. $(\mathrm{MHz})$ <br> $\mathrm{f}_{\mathrm{O}}=$ output freq. $(\mathrm{MHz})$ <br> $\mathrm{C}_{\mathrm{L}}$ = load capacitance ( pF ) <br> $\sum\left(\mathrm{f}_{0} \mathrm{C}_{\mathrm{L}}\right)=$ sum of outputs <br> $\mathrm{V}_{\mathrm{DD}}=$ supply voltage $(\mathrm{V})$ |

# Quadruple low to high voltage translator <br> HEF4104B <br> with 3-state outputs 



Fig. $4 \mathrm{~V}_{\mathrm{DDO}}$ as a function of $\mathrm{V}_{\mathrm{DDI}}$; the shaded area shows the permissible operating range.

