SY7T609+S1

Energy Measurement Processor with Integrated Oscillator

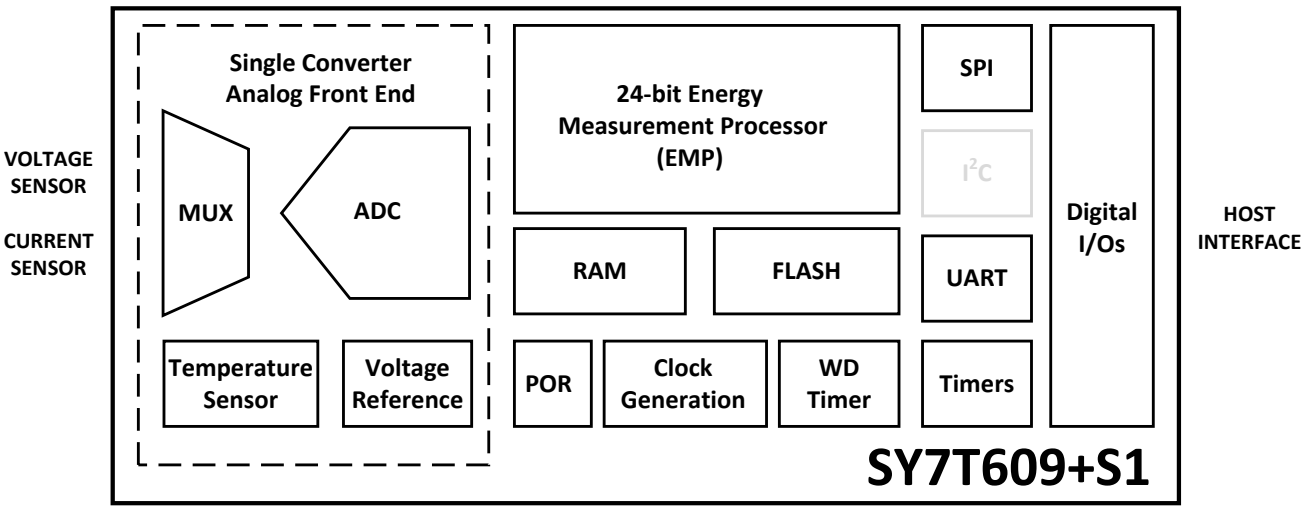
DESCRIPTION

The SY7T609+S1 is an energy measurement processor (EMP) designed for monitoring any 2-wire circuit. With an integrated oscillator and small profile, it is ideally suited for BOM optimized applications such as smart-plugs, smart appliances, lighting and building automation. SPI and UART interface options are supported. An optimized protocol for low baud rate UART communications further reduces the BOM cost when data isolation is required.

The analog front end (AFE) provides differential analog inputs for interfacing to current sensors and voltage sensors. Scaled voltages from the sensors are fed to a high-resolution delta-sigma converter. A low power 24-bit energy measurement processor (EMP) with embedded firmware performs all the necessary computation, compensation, and data formatting for interfacing to any host controller. With available nonvolatile memory for storing calibration coefficients and configuration data, the SY7T609+S1 provides an autonomous solution that greatly simplifies system integration.

FEATURES

- High resolution delta-sigma ADC with two analog (sensor) inputs
- Precision internal voltage and timing references minimize external components
- 24-bit energy measurement processor with nonvolatile storage of calibration and configuration data
- Flexible SPI or UART interface options with user configurable DIO
- Small 14-pin TSSOP package



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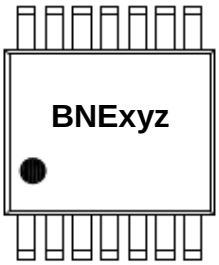
1 Ordering Information

Ordering Number	Carrier	Firmware	Package	Top Marking
SY7T609B+S1	Tubes	+S1	TSSOP-14	BNExyz
SY7T609T+S1	Tape & Reel			

S Y 7 T 6 0 9 □ + S 1

- Firmware version code
- Pre-programming adder
- Carrier Type (B for bulk, T for tape & reel)



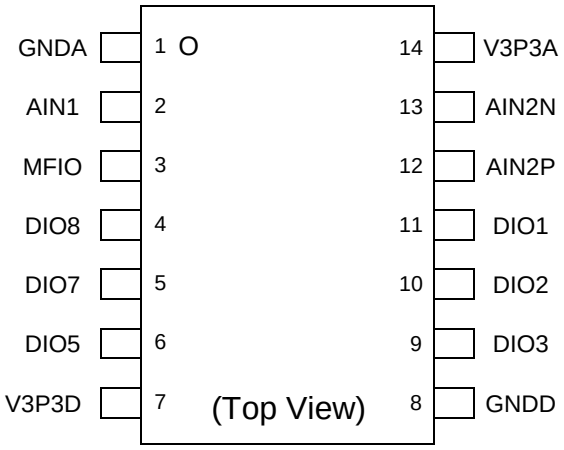
BNE = Device Code for all SY7T609

x = Year Code

y = Week Code

z = Lot Number Code

2 Pinout



Pin	Name	Description
1	GNDA	Ground pin (Analog)
2	AIN1	Voltage Sense Input (pos)
3	MFIO	Multi-function I/O: Defined as Voltage Sense Input (neg) in this solution.
4	DIO8	Interface Select, and Digital I/O. Pin is sampled upon reset to select the serial interface.
5	DIO7	Digital I/O
6	DIO5	SPI SSB or Digital I/O
7	V3P3D	3.3VDC Supply (Digital)
8	GNDD	GROUND (Digital)
9	DIO3	SPI MISO, UART TX (Data Out)
10	DIO2	SPI MOSI, UART RX (Data In)
11	DIO1	SPI SCK or Digital I/O
12	AIN2P	Current Sense Input (pos)
13	AIN2N	Current Sense Input (neg)
14	V3P3A	3.3VDC Supply (Analog)

3 Hardware Resources Overview

The SY7T609 hardware integrates all the functional blocks required for solid-state power and energy measurement of any two-wire circuit. Only a few external resistors and capacitors are required. Included on the device are:

- Temperature compensated oscillator and clock management logic
- Integrated power-on reset and watchdog timer
- High-accuracy analog front-end (AFE) with trimmed voltage reference and temperature sensor
- 24-bit energy measurement processor with RAM and flash memory
- Peripheral interfaces (UART, I2C or SPI) with Digital I/O and PWM outputs – *usage varies with firmware*

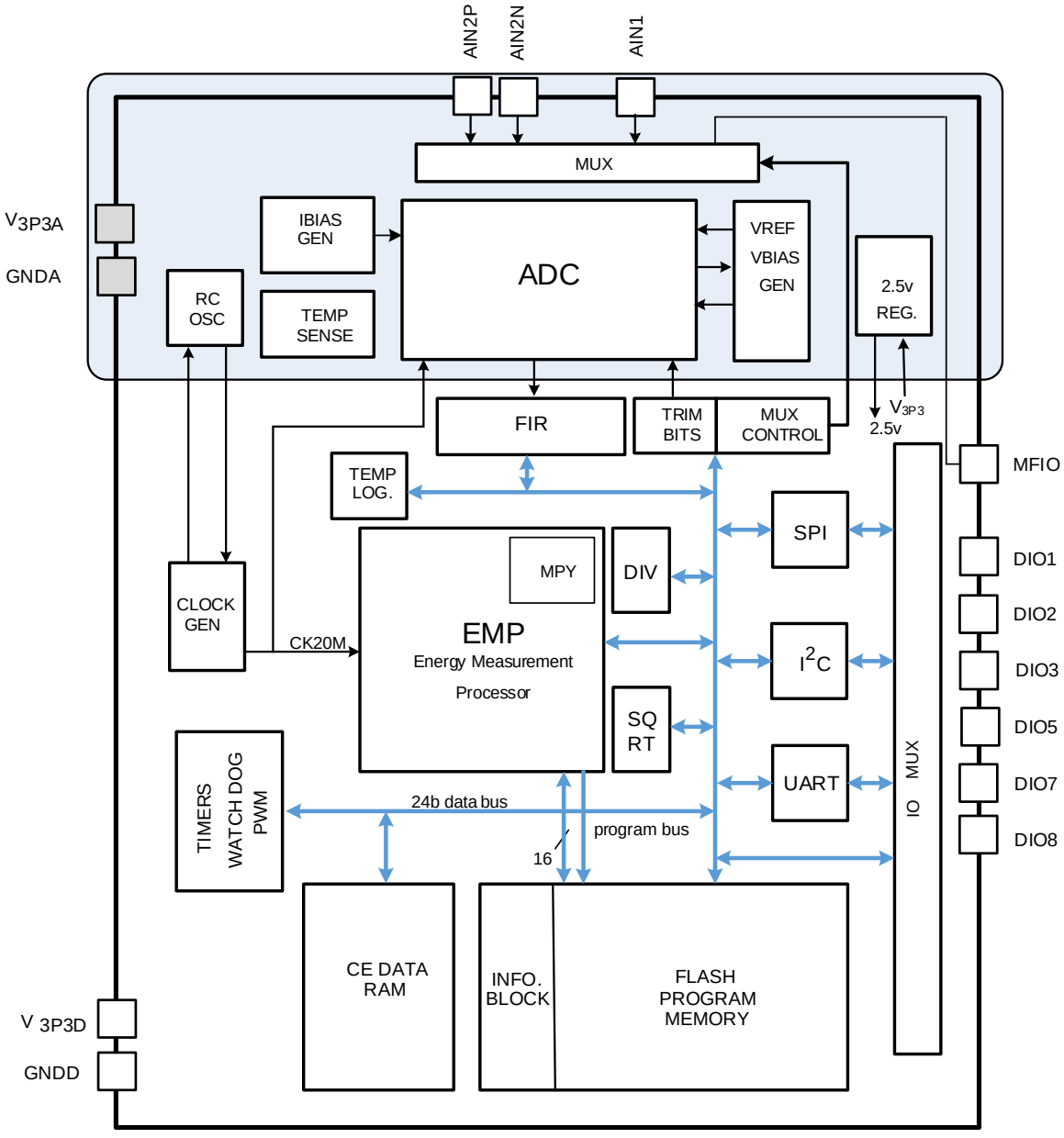


Figure 3-1. SY7T609 Functional Block Diagram

3.1 Clock Management, Power-On Reset, and WD Timer

Clock Management

The SY7T609 features an internal trimmed and temperature compensated RC oscillator running at 20MHz. A clock management unit distributes the clocks to the rest of the device.

Power-On Reset (POR)

An on-chip Power-On Reset (POR) block monitors the supply voltage (V_{3P3D}) and initializes the internal digital circuitry at power-on. Once V_{3P3D} is above the minimum operating threshold, the POR circuit triggers and initiates a reset sequence. It will also issue a reset to the digital circuitry if the supply voltage falls below the minimum operating level.

Watchdog Timer (WDT)

A Watchdog Timer (WDT) block detects any software processing errors. The embedded software periodically refreshes the free-running watchdog timer to prevent it from timing out. If the WDT times out, it is an indication that software is no longer being executed in the intended sequence; thus, a system reset is initiated.

3.2 Analog Front-End and Conversion

The Analog Front-End (AFE) of the SY7T609 includes an input multiplexer, delta-sigma A/D converter, bias current references, voltage references, temperature sensor, and several voltage fault comparators.

Delta-Sigma A/D Converter

A second-order delta-sigma converter digitizes the analog inputs. The converted data is then processed through an FIR filter.

Voltage Reference

The device includes an on-chip precision bandgap voltage reference that incorporates auto-zero techniques as well as production trims to minimize errors caused by component mismatch and drift. The voltage reference is digitally compensated over temperature.

Die Temperature Measurement

The device includes an on-chip die temperature sensor used for digital compensation of the voltage reference. It is also used to report temperature information to the user.

Voltage and Current Inputs

The external voltage and current sensors are connected to analog input pins. The full-scale signal level that can be applied to the analog input pins is V3P3A ±250 mVpk. With a sinusoidal waveform, the maximum RMS voltage is:

$$\mathrm{VrmsMAX} = \frac{250mVpk}{\sqrt{2}} = 176.78\mathrm{mVRMS}$$

Although the inputs are differential, a common-mode voltage of less than ±25 mV is recommended to fully utilize the available dynamic range.

3.3 Energy Measurement Processor

The SY7T609 integrates a dedicated 24-bit processor that performs all the digital signal processing necessary for measurement, calibration, compensation, analysis, alarms generation, etc. Refer to the *Functional Description and Operation* section for detailed information on the firmware implementation for SY7T609+S1.

3.4 Flash and RAM

The SY7T609 includes on-chip flash memory for storing program code, coefficients, calibration data, and configuration settings. The SY7T609 also includes on-chip RAM which is used to store the values of input and output registers and utilized by the firmware for its operations.

3.5 Digital I/O

The SY7T609 features general purpose digital I/O. The digital I/O are either managed directly by the user, by the embedded firmware, or multiplexed with the serial communication interfaces. The following table summarizes the multiplexing and pin assignment for the SY7T609+S1 firmware:

Pin Name	Pin #	Function at Power-On Reset	Function by Interface	
			SPI	UART
MFIO	3	--	Analog Input	
DIO8	4	Interface Select	DIO8	
DIO7	5	--	DIO7	
DIO5	6	--	SSB	DIO5
DIO3	9	--	MISO	TX
DIO2	10	--	MOSI	RX
DIO1	11	--	SCK	DIO1

3.6 Serial Interfaces

The SY7T609+S1 supports UART and SPI interface options, but only one interface can be active at a time. The pin DIO8 is sampled following a power-on reset to select between SPI interface or UART. The user should allow at least 10ms from a power-on reset event for the selection pin status to be latched and the serial interface selected. During this time the status of DIO8 must not change.

Selected Interface	DIO8
SPI	0
UART	1

Warning

Where applicable, pins should be configured via pull-up and pull-down resistors as these pins could become outputs after initialization. Therefore, direct connection to GNDD/GNDA or V3P3D/V3P3A supplies must be avoided.

3.6.1 UART Interface

The SY7T609 features a UART interface with a data rate ranging from 2400 up to 115k Baud. The UART interface has a fixed configuration supporting: 8-bit, one start bit, one stop bit and no-parity. The UART interface hardware does not provide handshaking hardware signals (i.e. RTS, CTS etc.).

The UART clock is derived from the 20MHz system clock. The error due to the clock division is reported in the following table.

BAUD	Actual Baud	Percent error
2400	2399.808	0.008
4800	4800.768	0.016
9600	9596.929	-0.032
19200	19193.86	-0.032
38400	38461.54	0.160
57600	57541.26	-0.2235
115200	114942.5	-0.2235

Refer to the *UART Protocol* section for further details on the communication protocol implemented in this firmware.

3.6.2 SPI Interface

The SPI featured in the SY7T609 is slave only. Once the SPI interface is activated, it utilizes the following digital I/O as the SPI interface:

DIO5: Slave select (SSB) is an active low input signal.
DIO1: Serial Data Clock (SCK) input.
DIO3: Master Input, Slave Output (MISO), serial data output.
DIO2: Master Output, Slave Input (MOSI), serial data input.

The SPI interface allows read and write access to the data RAM specified in the command bit field ADDR[5:0]. The command limits the access to RAM locations 0x00 through 0x3F. Refer to the *Indirect Register* Access section for details on accessing other RAM locations.

SPI Mode

The device operates in mode 3 (CPOL=1, CPHA=1) and as such the data is captured on the rising edge and propagated on the falling edge of the serial data clock (SCK). The figure below shows a single-byte transaction on the SPI bus. Bytes are transmitted/received MSB first.

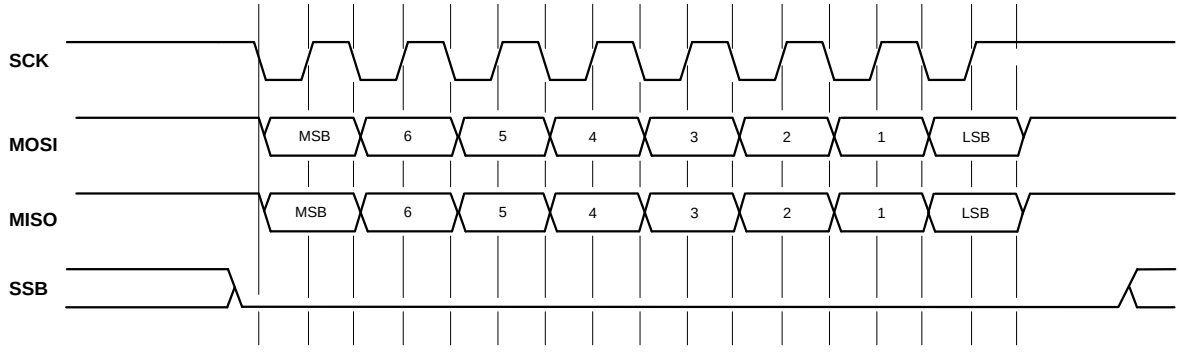


Figure 3-2. Signal Timing on the SPI Bus

Single Word SPI Reads

The device supplies direct read access to the device RAM memory. To read the RAM the master device must send a read command to the slave device and then clock out the resulting read data. SSB must be kept active low for the entire read transaction (command and response). SCK may be interrupted as long as SSB remains low. ADDR[5:0] is filled with the word address of the read transaction. RAM data contents are transmitted most significant byte first. ADDR[5:0] cannot exceed 0x3F. RAM words, and therefore the results, are natively 24 bits (3 bytes) long.

Single Word SPI Read Command (MOSI)

Byte #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0x01							
1	ADDR[5:0]						0x0	
2	0							
3	0							
4	0							

The slave responds with the data contents of the requested RAM addresses.

Single Word SPI Read Response (MISO)

Byte #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	Hi-Z (during Read Command)							
1	Hi-Z (during Read Command)							
2	DATA[23:16] @ ADDR							
3	DATA[15:8] @ ADDR							
4	DATA[7:0] @ ADDR							

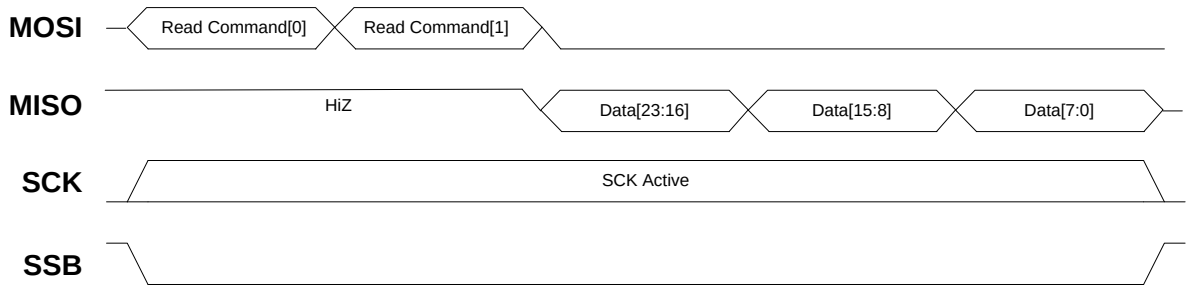


Figure 3-3. Single Word Read Access Timing

Single Word SPI Writes

The device supplies direct write access to the device RAM memory. To write the RAM the master device must send a write command to the slave device and then clock out the write data. SSB must be kept active low for the entire write transaction (command and data). SCK may be interrupted as long as SSB remains low. ADDR[5:0] is filled with the word address of the write transaction. RAM data contents are transmitted most significant byte first. ADDR[5:0] cannot exceed 0x3F. RAM words are natively 24 bits (3 bytes) long.

Single Word SPI Write Command and Data (MOSI)

Byte#	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0x01							
1	ADDR[5:0]						0x02	
2	DATA[23:16] @ ADDR							
3	DATA[15:8] @ ADDR							
4	DATA[7:0] @ ADDR							

The slave SDO remains Hi-Z during a write access.

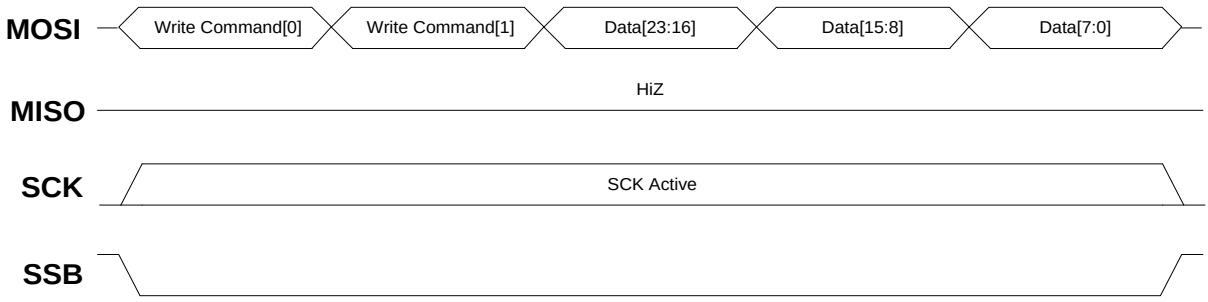


Figure 3-4. Single Word Write Access Timing

4 Functional Description and Operation

The SY7T609+S1 firmware implements features ideally suited for applications such as smart-plugs, smart appliances, lighting and home/building automation. It provides relevant signal processing and measurement outputs along with auxiliary functions such as configurable alarm detection, calibration commands, zero-crossing detection, and user DIO control.

A set of input (write), output (read) and read/write registers are provided to allow access to calculated data and alarms and to configure the device. The input (write) registers values can be saved into flash memory through a specific command. The values saved into flash memory will be loaded in these registers at reset or power-on as defaults.

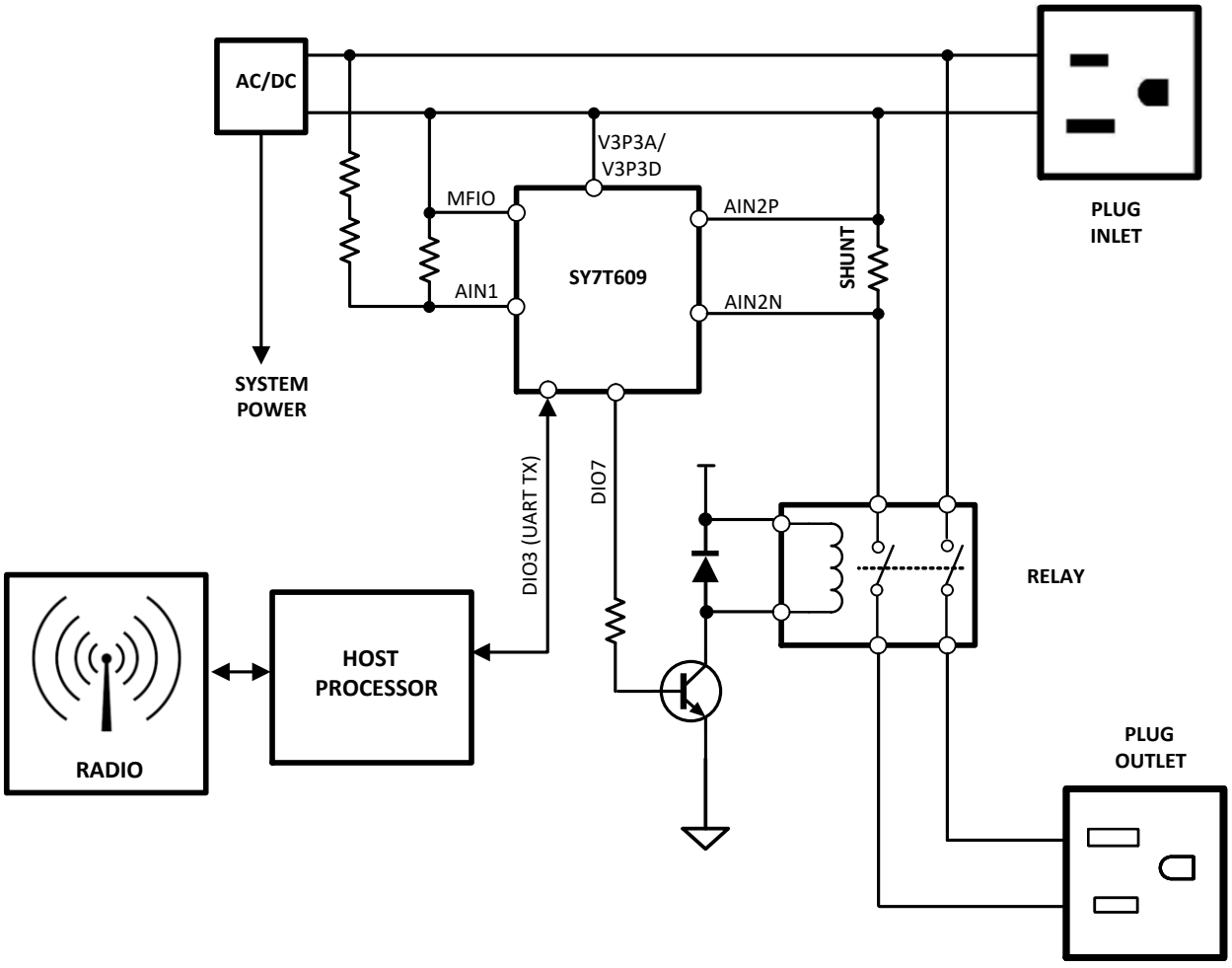


Figure 4-1. Typical Smart-Plug Block Diagram Example

4.1 Voltage and Current Inputs Conditioning

The sensor input voltages are digitized using a single integrated second-order delta-sigma A/D converter. The analog front-end includes a temperature sensor whose output is digitized and used for temperature (gain) compensation.

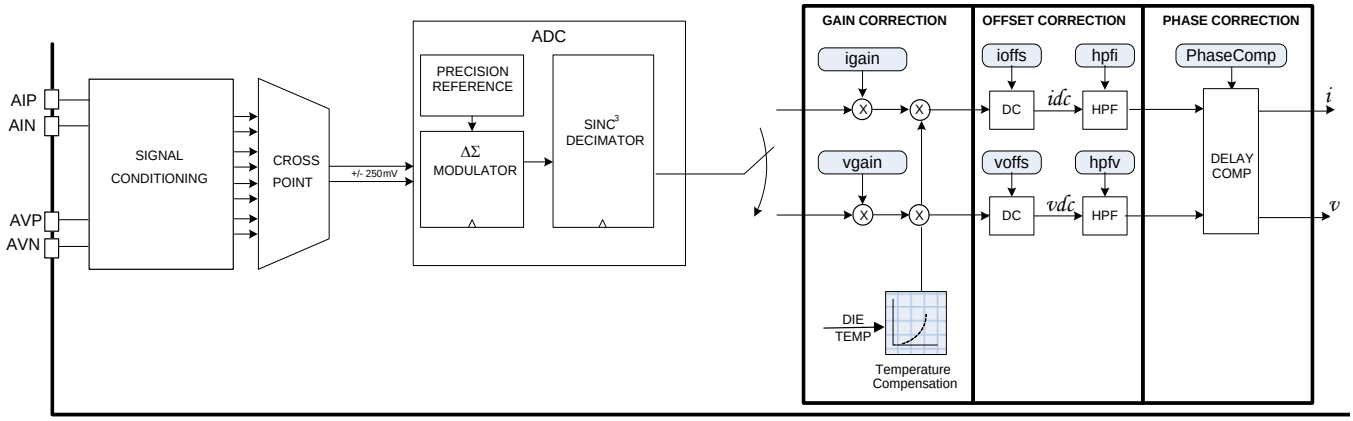


Figure 4-2: Analog Input Signal Conditioning

4.1.1 Gain Correction

The firmware implements individual gain correction for the Voltage and Current sensors as well as common gain correction for the temperature effects on the gain of the ADC.

4.1.2 Offset Correction

The fixed offsets and high-pass filters (HPF) can remove any DC from the signal paths and consequently from power and RMS calculated values. The offset registers (Voffs, Ioffs) remove any fixed ADC or system level DC offsets from the raw samples. These offsets can be set by the user, by an automatic calibration routine, or adjusted dynamically by the FW.

4.1.3 Phase Compensation

A phase compensation register is provided to compensate phase errors introduced by current transformers (CT) or external filters. The amount of phase shift is set by the PhaseComp register as a fractional number of ADC samples with a total range of +/- 4 ADC samples (roughly +/- 20 degrees for a 60Hz line frequency). The register is signed fixed point with the binary point to the left of bit 21. Values are in units of high rate (6702 Hz) sample delays so each integer unit of delay is 149µs with a total possible delay of ±4 samples (roughly ±20° at 60Hz).

Example: To compensate a phase error of 277.77µs (or 6° at 60Hz) introduced by a current transformer (CT) it is necessary to enter the following:

$$Phase\ Compensation\ =\ \frac{Phase\ Error}{\frac{1}{Sample\ Rate}}$$

$$Phase\ Compensation\ =\ \frac{277E^{-6}}{\frac{1}{6702}} = 1.86$$

The value to be entered in the phase compensation register is therefore:

$$PhaseComp\ =\ 1.86 * 2^{21} = 3900703 = 0x3B851E$$

4.2 Zero-Crossing & Line Frequency

The SY7T609+S1 includes a zero-crossing detection feature on the AC input channels. The zero-crossing detection allows measurements to be synchronized to the frequency of the incoming waveforms. There is an internal time delay of the zero-crossing detection versus from the external zero crossing of approximately 750µs.

The zero-crossing detection employs a hysteresis value to prevent spurious detection in case the input is left floating or in a noisy environment. If the absolute value of the input voltage does not go above the value specified in the VHYST register in each direction, the device will not detect zero-crossings.

The zero-crossing information can be redirected to a Digital I/O pin. The zero-crossing signal is a pulse with a 150µs width.

The measured AC line frequency is also calculated and reported.

4.3 Accumulation Interval

The accumulation interval is the amount of time over which the device processes instantaneous data samples before updating the measurement outputs. The accumulation interval is configurable by the user through the ACCUM and ACCUMCYC registers. The DIVISOR register reports the actual number of samples used within any given accumulation interval. A FRAME register counts accumulation intervals

4.3.1 Fixed Interval

When the ACCUMCYC register is 0 then the device will operate on a fixed time accumulation interval set by the ACCUM register. The ACCUM register contains an unsigned integer values representing the accumulation interval (time) expressed in number of high-rate samples.

$$Accumulation\ Interval = ACCUM * Sample\ Rate$$

4.3.2 Line Locked Interval

The accumulation interval can also be locked to the incoming line voltage cycles. When the ACCUMCYC register is set to a non-zero value, the accumulation interval will end after ACCUMCYC low-to-high zero crossings of the Reference AC Voltage (see Zero-Crossing Detection) unless the maximum accumulation time has elapsed. This will cause the device to use an accumulation interval of ACCUMCYC line cycles regardless of the line frequency.

$$Accumulation\ Interval = \frac{ACCUMCYC}{Line\ Frequency}$$

4.4 Current and Voltage RMS Calculations

The SY7T609+S1 provides true RMS measurements for both current and voltage inputs. The RMS is obtained by performing the square sum of the instantaneous samples of voltage and current over a time interval (commonly referred as accumulation time) and then performing a square root of the result after dividing by the number of samples in the time interval. Optional RMS offset controls are available for each reported value to help compensate for an uncorrelated system noise floor.

$$VRMS = \sqrt[2]{\left(\frac{\sum_{n=0}^{N-1} Vn^2}{N} - VrOFF\right)} \qquad IRMS = \sqrt[2]{\left(\frac{\sum_{n=0}^{N-1} In^2}{N} - IrOFF\right)}$$

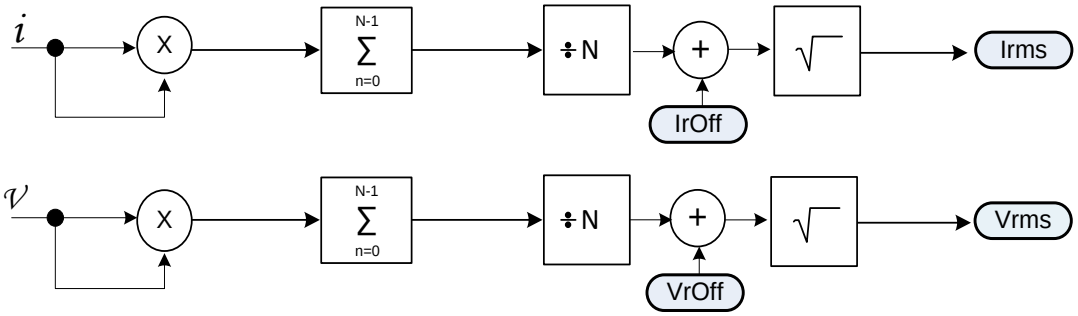


Figure 4-3: RMS Calculations

4.5 Current and Voltage Average Calculations

The SY7T609+S1 provides average/DC measurements for both current and voltage inputs. The average is obtained by performing the sum of the instantaneous samples of voltage and current over a time interval (commonly referred as accumulation time) and then dividing by the number of samples in the time interval.

$$VAVG = \frac{\sum_{n=0}^{N-1} Vn}{N} \qquad IAVG = \frac{\sum_{n=0}^{N-1} In}{N}$$

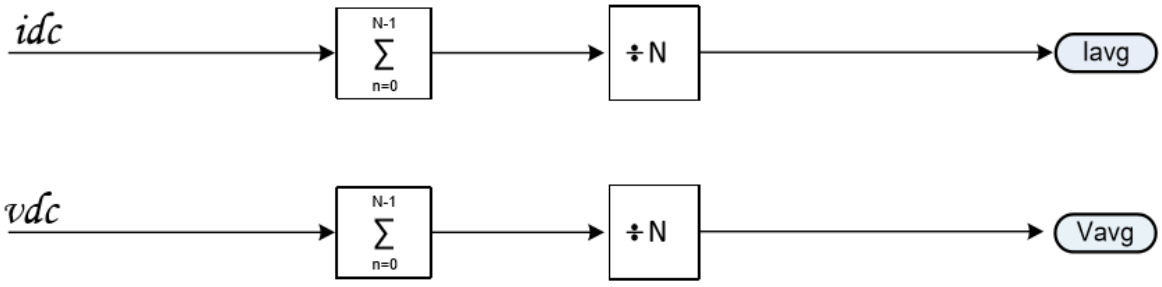


Figure 4-4: RMS Calculations

4.6 Power Calculations and Power Factor

The SY7T609+S1 computes the active, reactive, and apparent power. In addition, the SY7T609+S1 computes the fundamental power, determined only by the fundamental components of the voltage and current and the harmonic power, determined by the harmonic components of the voltage and current.

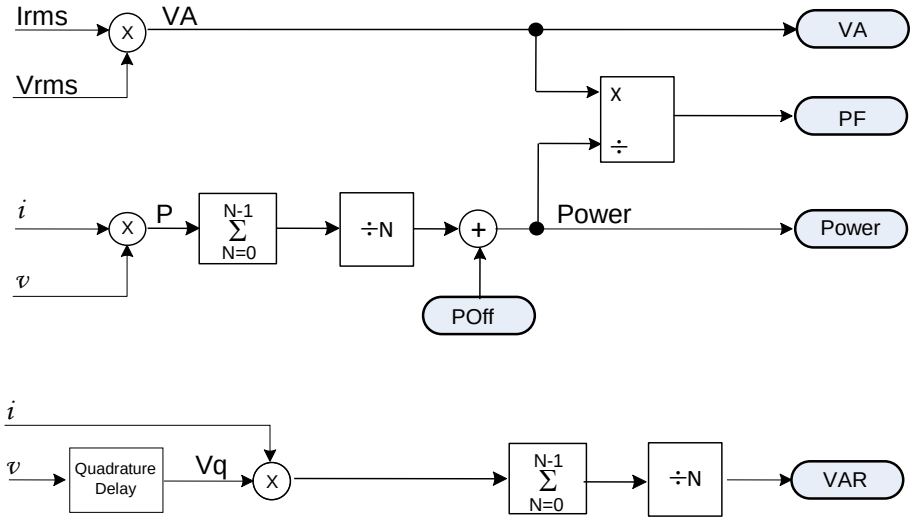


Figure 4-5: Power (Active, Reactive, and Apparent) and Power Factor Calculation

4.6.1 Active Power Calculation

Active power is calculated as the product of the voltage and current waveforms. The resulting waveform is the instantaneous power signal (P), and it is equal to the rate of energy flow at every instant of time. The unit of power is the watt or joules/sec. The instantaneous power is then averaged over N samples (accumulation time) for the computation of active power (Power). A rolling average of active power results (avgpower) calculated over multiple accumulation cycles is also reported. An optional power offset control is available to help compensate for an uncorrelated system noise floor.

$$Power = \frac{\sum_{n=1}^{N-1} v_n \, i_n}{N}$$

4.6.2 Reactive Power

The reactive power is calculated as multiplication of instantaneous samples of current (i) and the instantaneous quadrature voltage (Vq). The quadrature voltage is obtained through a 90° phase shift (quadrature delay) of the voltage samples. The samples are then averaged over the accumulation time interval for the computation of reactive power (VAR).

$$VAR = \sqrt{\sum_{n=0}^{N-1} i_n \times Vq_n}$$

4.6.3 Apparent Power

The apparent power (VA) is the product of RMS voltage (V_{RMS}) and current (I_{RMS}). The apparent power results, also referred as Volt-Amps, are available at the register VA.

$$VA = I_{RMS} * V_{RMS}$$

4.6.4 Power Factor

The power factor (PF) is calculated as active power (Power) divided by the apparent power (S). The sign of the power factor is determined by the active power sign.

$$PF = \frac{power}{S}$$

4.7 Fundamental and Harmonics Calculations

The SY7T609+S1 allows extraction and calculation of a single selected harmonic. By default, the fundamental (first harmonic) is selected for voltage, current, active, reactive real and apparent power calculations. The HARM register can be used to select a single harmonic to extract.

By setting the value in the HARM register to a higher harmonic, the fundamental result registers will contain amplitudes of the selected harmonic. In this case the harmonic result register will contain the balance of the voltage, current, or power.

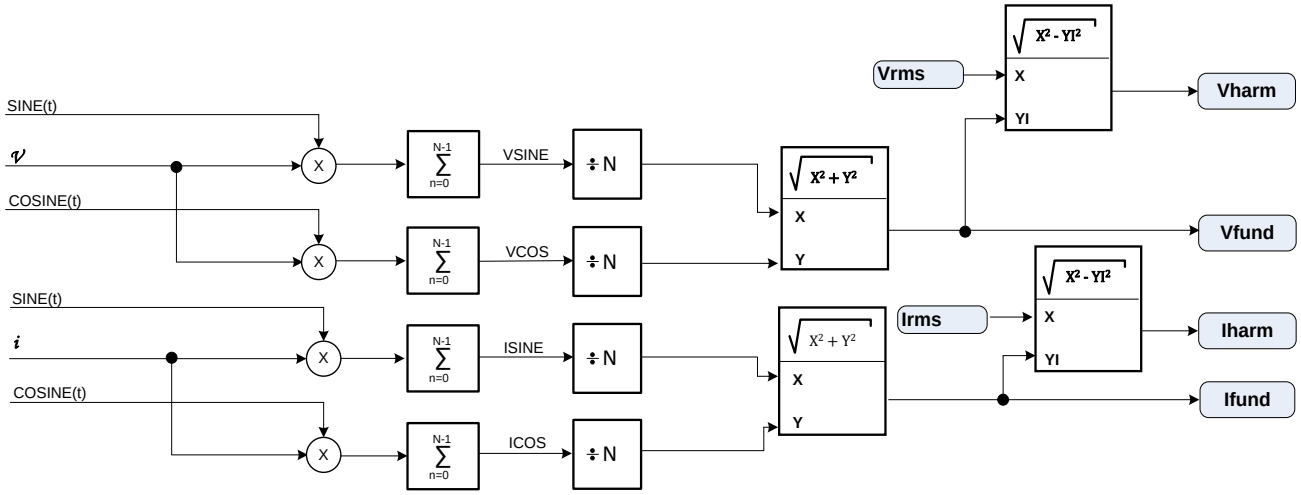


Figure 4-6: Voltage and Current Fundamental and Harmonic Calculations

4.8 Energy Accumulation

Energy calculations are included to minimize the traffic on the host interface and simplify system design. The energy in the accumulation intervals are summed together until a user defined “bucket size” is reached. When every bucket of energy is reached, the value in the energy counter register is incremented by one. All energy counter registers are low-rate 24-bit output registers that contain values calculated over multiple accumulation intervals. Both import (positive) and export (negative) results are provided for active energy.

Register	Description
EPPCNT	Positive Active Energy Counter
EPMCNT	Negative Active Energy Counter
EPNCNT	Net Active Energy
EQNCNT	Net Reactive Energy
ESNCNT	Net Apparent Energy

Energy results are cleared upon any power down or reset and can be manually cleared by the user using the command register. The FRAME register can be used to detect device resets (loss of energy data) or to track time between energy reads.

4.8.1 Bucket Size for Energy Counters

The BUCKET register(s) allows the user to define the unit of measure for the energy counter registers. It is an unsigned 48-bit fixed-point number with 24 bits for the integer part and 24 bits for the fractional part. The bucket size can be saved to flash memory as the register default.

	High Word						Low Word						
Bit Position	23	22	…	2	1	0	23	22	21	20	…	1	0
Value	2^{23}	2^{22}	…	2^{2}	2^{1}	2^{0}	2^{-1}	2^{-2}	2^{-3}	2^{-4}	…	2^{-23}	2^{-24}

$$BUCKET = bucketh + \frac{bucketl}{2^{24}}$$

$$Bucket\ in\ Wh = BUCKET * \frac{3600s * 6702sps}{FSI * FSV}$$

Example:
If FSV=667Vpk, FSI=62Apk then to increment the energy counters in 1.0 watt-hours for example, the value in BUCKET should be:

$$Bucket\ in\ Wh = 1.0 * \frac{3600s * 6702sps}{FSI * FSV} = 583.4309$$

bucketh=583 (0x000247)

bucketl=0.4309 * 2^{24}= 7229302 (0x6E4F76)

4.9 Min, Max, and Peak Tracking

The SY7T609+S1 reports the lowest and highest voltage and current RMS values. To reset these values it is necessary to write to these registers. For example, a value of 0x000000 should be written in the Vhi or Ihi register to reset them. Similarly, a value of 0x7FFFFF should be written to the Vlo and Ilo registers to reset them.

The highest instantaneous voltage and current measured during an accumulation interval is also reported in output registers Vpeak and Ipeak. These values are updated at each accumulation interval.

4.10 Alarm Monitoring

The SY7T609+S1 includes a set of user-configurable alarms for die temperature, voltage, current, power, and line frequency. Most alarms have a corresponding register to store the threshold above which (in the case of “max” limits), or below which (in the case of “min” limits) an alarm condition is generated. Such a condition does not necessarily cause an alarm. The condition must exist for the duration of the associated hold-off time measured in number of accumulation intervals. If the alarm condition exceeds the hold-off time, an alarm event is generated and reported in the corresponding bit of the alarm register.

A corresponding event counter is also incremented. Counter registers increment at each alarm occurrence and can be cleared by the user by writing a zero value to the respective counter register.

4.10.1 Voltage Sag/Surge and Drop-Out Detection

Additional voltage monitoring functions are implemented that are refreshed at intervals shorter than an accumulation interval.

Voltage Sag and Surge function performs cycle-by-cycle monitoring of the AC line voltage. The RMS value of the line voltage is calculated over a full line cycle and compared with sag and surge thresholds. Registers VSagTh and VSurgeTh contain the values of the sag and surge thresholds.

The drop-out detection is meant to generate an even faster response to an AC dropout. It is based on a configurable threshold and a configurable number of high-rate samples. The dropout alarm is generated each time in which the AC input voltage is below the VDropTh threshold for a time greater than VDropHold.

4.10.2 Alarm Bit Definitions and Configuration Registers

The following bit definitions apply to the Alarms, Alarm_Sticky, Alarm_Set, Alarm_Reset, and Mask# registers. The corresponding counter and alarm configuration registers are summarized below.

Bit #	Bit Name	Alarm Counter	Alarm Conditions		Bit Definition
			Threshold	Hold-Off	
23	DataReady		--	--	Low-Rate results have been updated.
22	OverTemp	TmaxCnt	TmaxTh	TminHold	Die Temperature is Over Limit.
21	UnderTemp	TminCnt	TminTh	TminHold	Die Temperature is Under Limit.
20:14	Not Used		--	--	Not Used.
13	ISign		--	--	Polarity of the current waveform.
12	VSign		--	--	Polarity of the voltage waveform.
11	Vsag	VsagCnt	VsagTh	--	Voltage Sagged below limit.
10	Vsurge	Vsurgecnt	VsurgeTh	--	Voltage Surged above limit.
9	VdropOut		VdropTh	VdropHold	Voltage Dropped below limit
8	OverVolt	VmaxCnt	VmaxTh	VminHold	RMS Voltage went above upper limit.
7	UnderVolt	VminCnt	VminTh	VminHold	RMS Voltage fell below lower limit.
6	OverCurrent	ImaxCnt	ImaxTh	ImaxHold	RMS Current went above limit.
5	OverPower	PmaxCnt	PmaxTh	PmaxHold	Power went above limit.
4	OverFreq	FmaxCnt	FmaxTh	FminHold	Line Frequency went above upper limit.
3	UnderFreq	FminCnt	FminTh	FminHold	Line Frequency fell below lower limit.
2	Not Used		--	--	Not Used
1	Zero_Cross		--	--	Voltage low-to-high Zero Crossing Detected
0	Not Used		--	--	Not Used.

4.10.2.1 Alarms Status Register

The Alarms register is an output register (read-only) that contains the status of the alarms and other conditions.

4.10.2.2 Alarm_Sticky Register

The Alarm_Sticky register is an input register that allows configuring individual bits into the Alarms register to hold the alarm status (“sticky”) until an Alarm_Reset command is issued. Each alarm can otherwise be set to auto-reset after the removal of the offending condition and the completion of the next accumulation interval. The Alarm_Sticky register can be saved into flash memory.

4.10.2.3 Alarm_Set and Alarm_Reset Registers

Setting the bit Alarm_Reset[#] to 1 will clear the corresponding Alarm register bit (Alarms[#]). Likewise, By setting the bit Alarm_Set[#] to 1, the user can force the corresponding Alarm register bit (Alarms[#]). This register is mainly used for system test purposes or relay control. Both Alarm_Set[#] and Alarm_Reset[#] will return to 0 upon completion.

4.10.2.4 DIO Mask Registers

A Mask register associated with each digital I/O pin allows the user to select which alarm will activate the pin. For example, to select OverCurrent and Vsurge to drive the DIO7 pin, the Mask7 register should be set to 0x000440. The value of the Mask register can be saved into flash memory.

4.11 Digital Input Output Usage and Control

The SY7T609 has a set of digital I/O's that are multi-function and user-configurable. The digital I/O pins can be driven through the relevant registers or assigned to a function by the firmware. Their functional assignment depends on the interface that is selected and the firmware implementation.

Table 4-1. Digital I/O's Function and Pin Mapping

DIO Register [(1)] Bit#	DIO MASK Register	Pin Name	Pin #	Function at Power-On Reset	Function by Interface	
					SPI	UART
23:16	-	-	-	-	-	
15	-	MFIO	3		Analog Input	
14-9	-	-	-	-	-	
8	MASK8	DIO8	4	Interface Select	DIO8	
7	MASK7	DIO7	5	-	DIO7	
5	MASK5	DIO5	6	-	SSB	DIO5
4	-	-	-	-	-	
3	-	DIO3	9	-	MISO	TX
2	-	DIO2	10	-	MOSI	RX
1	MASK1	DIO1	11	-	SCK	DIO1
0	-	-	-	-	-	

Note:

1) Applies to registers: DIO_DIR, DIO_STATE, DIO_SET, DIO_RST and DIO_POL.

4.11.1 Digital I/O Pins Direction (DIO_DIR)

The DIO_DIR register sets the direction of the pins, where "1" is input and "0" is output. For pins used as part of the selected serial interface, the DIO_DIR register has no effect. If a DIO is defined as an input, a weak internal pull-up is active.

4.11.2 Digital I/O Pins Input State (DIO_STATE)

The DIO_STATE register reports the current state of the DIOs (1 = active and 0= non-active).

4.11.3 Digital I/O Pins Output Set (DIO_SET)

By setting the bit DIO_SET[#] to 1 the user can set the state of the corresponding DIO pin to high if configured as an output. DIO_STATE[#] will also reflect this change. DIO_SET[#] will return to 0 upon completion.

4.11.4 Digital I/O Pins Reset (DIO_RST)

By setting the bit DIO_RST[#] to 1 the user can set the state of the corresponding DIO pin to low if configured as an output. DIO_STATE[#] will also reflect this change. DIO_RST[#] will return to 0 upon completion.

4.11.5 Digital I/O Pins Polarity (DIO_POL)

For digital I/O's configured as outputs (DIO#), the DIO_POL[#] determines the active state polarity. For DIO_STATE, 1 = active and 0= non-active. For DIO_POL, 1 = active low, 0 = active high.

4.11.6 Digital I/O Pins MASK registers

The device provides MASK# registers for translating the state of any Alarms bit(s) to one of the DIO# pins if configured as an output. For example, if the bit-wise AND of MASK7[#] and Alarms[#] is non-zero then DIO7 is set to its active state. If the Mask register is set to 0 or the DIO pin is configured as an input, then the corresponding DIO is unaffected by Alarms.

4.12 On-Chip Calibration Routines

The SY7T609+S1 includes current and voltage and die temperature calibration routines. These routines modify gain and offset coefficients.

The user can set and start a calibration routine through the Command register. When the calibration process completes, command register bits 23:16 (set to 0xCA to issue a calibration command) are cleared along with bits associated with channels that calibrated successfully. Any channels that failed will have their corresponding bit left set. After completion of the calibration, the new coefficients can be saved into flash memory as defaults by issuing the Save to Flash Command (0xACC2xx).

4.12.1 Voltage Gain Calibration using VRMS target

In order to calibrate the voltage gain, a stable supply must be applied to analog input. The value corresponding to the applied supply (usually obtained from a power meter) must be entered in the relevant target register (vrmstarget). To start the calibration, the calibration command (0xCAxxxx) with the calib.vrms bit (0x000020) set must be written to the Command register.

For each iteration, the RMS value for voltage is averaged over the number of measurement cycles set by the register CalCyc. At the end of each iteration, the voltage gain is multiplied by the ratio of the target to the measured value.

$$VgainNew = \mathrm{VgainOld} * \frac{\mathrm{VrmsTarget}}{\mathrm{Vrms}}$$

4.12.2 Current Gain Calibration using IRMS target

In order to calibrate the current gain, a stable load must be applied to the channel to be calibrated. The value corresponding to the applied load (usually obtained from a power meter) must be entered in the relevant target register (irmstarget). To start the calibration, the calibration command (0xCAxxxx) with the calib.irms bit (0x000010) set must be written to the Command register.

For each iteration, the RMS value for current is averaged over the number of measurement cycles set by the register CalCyc. At the end of each iteration, the current gain is multiplied by the ratio of the target to the measured value.

$$IgainNew = \mathrm{IgainOld} * \frac{\mathrm{IrmsTarget}}{\mathrm{Irms}}$$

4.12.3 Current Gain Calibration using power target

In order to calibrate the current gain, a stable load must be applied to the channel to be calibrated. The value corresponding to the applied load (usually obtained from a power meter) must be entered in the relevant target register (powertarget). To start the calibration, the calibration command (0xCAxxxx) with the calib.power bit (0x000100) set must be written to the Command register.

For each iteration, the active power value is averaged over the number of measurement cycles set by the register CalCyc. At the end of each iteration, the current gain is multiplied by the ratio of the target to the measured value.

$$IgainNew = \mathrm{IgainOld} * \frac{\mathrm{PowerTarget}}{\mathrm{Power}}$$

4.12.4 Voltage Offset Calibration using vavg target

In order to calibrate the voltage offset, a supply with a stable DC voltage must be applied to the channel to be calibrated. The value corresponding to the applied voltage (usually obtained from a power meter) must be entered in the relevant target register (vavgtarget). To start the calibration, the calibration command (0xCAxxxx) with the calib.voffs bit (0x000080) set must be written to the Command register.

For each iteration, the average voltage value is averaged over the number of measurement cycles set by the register CalCyc. At the end of each iteration, the delta between measured and target voltage is added to the existing offset.

$$voffsnew = voffsold + (vavg - vavgtarget)$$

4.12.5 Current Offset Calibration using iavg target

In order to calibrate the current offset, a supply with a stable DC current must be applied to the channel to be calibrated. The value corresponding to the applied current (usually obtained from a power meter) must be entered in the relevant target register (iavgtarget). To start the calibration, the calibration command (0xCAxxxx) with the calib.ioffs bit (0x000040) set must be written to the Command register.

For each iteration, the average current value is averaged over the number of measurement cycles set by the register CalCyc. At the end of each iteration, the delta between measured and target voltage is added to the existing offset.

$$ioffsnew = ioffsold + (iavg - iavgtarget)$$

4.12.6 On-Chip Temperature Calibration

To calibrate the on-chip temperature sensor, the user must first set the “ct” bit (0x000400) in the Control register. This command prevents the firmware from overwriting the CTemp register. Next the user must write the known chip temperature reading to CTemp. To start the calibration, the calibration command (0xCAxxxx) with the calib.ctemp bit (0x000001) set must be written to the Command register. This will cause the Toffs parameter to be updated with a new offset based on the known temperature supplied by the user.

5 Data Access and Configurability

The SY7T609+S1 has several user accessible registers that are used for configuring the device and to access results data. These registers are read (output), write (input), or read/write type, such as the Command register. These registers are accessible through the serial interface protocols described in this section.

Writing to reserved registers or to unspecified memory locations could result in malfunctions or unexpected results!

5.1 Registers Description

All user registers are contained in a 256-word (24-bits each) area of the on-chip RAM and can be accessed through the serial interface. The input and output registers have different data types, depending on their assignment and functions. The notation used, indicates whether the number is signed, unsigned or bit-mapped and the location of the binary point. U indicates an unsigned value, S indicated a signed value. The following notation indicates whether the number is signed, unsigned, or bit-mapped and the location of the binary point.

(S|U|B)(xx)?(.yy)?	
S|U|B	Indicates a Two's Compliment **S**igned, **U**nsigned or **B**it Mapped Value.
xx	(optional) Indicates a number with xx total bits. Defaults to 24 bits if absent.
.yy	(optional) Indicates a fixed-point number with yy bits to the right of the binary point. Defaults to 0 bits if absent

Example: S24.21 and S.21 are notations for a signed 24-bit number with 21 bits to the right of the decimal point.

Bit Position											
23	22	21	.	20	19	18	17	…	2	1	0
$S(-2^2)$	2^1	2^0		2^{-1}	2^{-2}	2^{-3}	2^{-4}	…	2^{-19}	2^{-20}	2^{-21}

Table 5-1. Data Types

Data Type	Description
S24	A 24-bit signed integer with a range of -8388608 to +8388607
U.24	A 24-bit unsigned fixed-point value with the binary point to the left of bit 23 with a range of 0 to 1 - 2^{-24}
U.23	A 24-bit unsigned fixed-point number with the binary point to the left of bit 22 and with a range of 0 to 1 - 2^{-23}
U.22	A 24-bit unsigned fixed-point number with the binary point to the left of bit 22 and with a range of 0 to 1 - 2^{-22}
U.21	A 24-bit unsigned fixed-point number with the binary point to the left of bit 22 and with a range of 0 to 4 - 2^{-21}
S.23	A 24-bit signed fixed point number with the binary point to the left of bit 22 and with a range of -1.0 to 1 - 2^{-23}
S.21	A 24-bit signed fixed-point number with a binary point to the left of bit 20 and with a range of -4.0 to 4-2^{-21}
S.16	A 24-bit signed fixed-point number with a binary point to the left of bit 16 and with a range of -128 to +128
B24	A variable containing 24 independent single-bit values
U48.24	See Energy Bucket

5.2 Register Map

Address		Name	Data Type	Flash Saved	Description	Default
Word (SPI)	Byte (UART)					
0x000	0x000	Command	B24	N	See Command Register Section	0x000000
0x001	0x003	FW Version	U24	NA	Firmware release version in hex format	0x0A1329
0x002	0x006	Control	B24	Y	See Control Register Section	0x001815
0x003	0x009	Reserved	U24	N	Reserved	NA
0x004	0x00C	Divisor	U24	N	Number of samples used for last accumulation interval	NA
0x005	0x00F	Frame	U48	N	Low Rate Accumulation interval counter	NA
0x006	0x012					
0x007	0x015	ALARMS	B24	N	Alarm Status Registers	NA
0x008	0x018	dio_state	B24	N	State of DIO Outputs	NA
0x009	0x01B	spi.wr.data	NA	N	See Indirect Register Access Section	0
0x00A	0x01E	spi.wr.addr	U24	N	See Indirect Register Access Section	0
0x00B	0x021	spi.rd.addr	U24	N	See Indirect Register Access Section	0
0x00C	0x024	spi.rd.data	NA	N	See Indirect Register Access Section	0
0x00D	0x027	CTemp	U24	N	Scaled Chip/Die Temperature	NA
0x00E	0x02A	Reserved	U24	N	Reserved	NA
0x00F	0x02D	VAVG	S24	N	Scaled Average Voltage	NA
0x010	0x030	IAVG	S24	N	Scaled Average Current	NA
0x011	0x033	VRMS	U24	N	Scaled RMS Voltage	NA
0x012	0x036	IRMS	U24	N	Scaled RMS Current	NA
0x013	0x039	Power	S24	N	Scaled Active Power	NA
0x014	0x03C	VAR	S24	N	Scaled Reactive Power	NA
0x015	0x03F	VA	S24	N	Scaled Apparent Power	NA
0x016	0x042	Frequency	U24	N	Scaled Line Frequency	NA
0x017	0x045	avgpower	S24	N	Scaled Average Active Power	NA
0x018	0x048	PF	S24	N	Scaled Power Factor	NA
0x019	0x04B	Vfund	U24	N	Scaled Fundamental RMS Voltage	NA
0x01A	0x04E	Ifund	U24	N	Scaled Fundamental RMS Current	NA
0x01B	0x051	Pfund	S24	N	Scaled Fundamental Active Power	NA
0x01C	0x054	Qfund	S24	N	Scaled Fundamental Reactive Power	NA
0x01D	0x057	VAfund	S24	N	Scaled Fundamental Apparent Power	NA
0x01E	0x05A	Vharm	U24	N	Scaled Harmonic RMS Voltage	NA
0x01F	0x05D	Iharm	U24	N	Scaled Harmonic RMS Current	NA
0x020	0x060	Pharm	S24	N	Scaled Harmonic Active Power	NA
0x021	0x063	Qharm	S24	N	Scaled Harmonic Reactive Power	NA
0x022	0x066	VAharm	S24	N	Scaled Harmonic Apparent Power	NA
0x023	0x069	EPPcnt	U24	N	Positive Active Energy Count	NA
0x024	0x06C	EPMcnt	U24	N	Negative Active Energy Count	NA
0x025	0x06F	EPNcnt	U24	N	Net Active Energy Count	NA
0x026	0x072	Reserved	U24	N	Reserved	NA

Address		Name	Data Type	Flash Saved	Description	Default
Word (SPI)	Byte (UART)					
0x027	0x075	Reserved	U24	N	Reserved	NA
0x028	0x078	EQNcnt	U24	N	Net Reactive Energy Count	NA
0x029	0x07B	Reserved	U24	N	Reserved	NA
0x02A	0x07E	Reserved	U24	N	Reserved	NA
0x02B	0x081	ESNcnt	U24	N	Net Apparent Energy Count	NA
0x02C	0x084	ILo	U24	N	Lowest scaled RMS Current result since last clear or reset	NA
0x02D	0x087	IHi	U24	N	Highest scaled RMS Current result since last clear or reset	NA
0x02E	0x08A	Ipeak	U24	N	Highest scaled instantaneous Current sample in last accumulation Interval	NA
0x02F	0x08D	VLo	U24	N	Lowest scaled RMS Voltage result since last clear or reset	NA
0x030	0x090	VHi	U24	N	Highest scaled RMS Voltage result since last clear or reset	NA
0x031	0x093	Vpeak	U24	N	Highest scaled instantaneous Voltage sample in last accumulation Interval	NA
0x032	0x096	DevAddr	U24	Y	Reserved for multi-point communications	0
0x033	0x099	DIO_dir	B24	Y	DIO Direction Setting	0xFFFFFF
0x034	0x09C	DIO_pol	B24	Y	DIO Polarity Setting	0
0x035	0x09F	DIO_set	B24	N	DIO Set High State Register	0
0x036	0x0A2	DIO_rst	B24	N	DIO Reset to Low State Register	0
0x037	0x0A5	Mask1	B24	Y	Alarm mask bits for DIO1 pin	0
0x038	0x0A8	Mask5	B24	Y	Alarm mask bits for DIO5 pin	0
0x039	0x0AB	Mask7	B24	Y	Alarm mask bits for DIO7 pin	0
0x03A	0x0AE	Mask8	B24	Y	Alarm mask bits for DIO8 pin	0
0x03B	0x0B1	Reserved	B24	Y	Reserved	0
0x03C	0x0B4	Reserved	B24	Y	Reserved	0
0x03D	0x0B7	Alarm_Sticky	B24	Y	Bits to control auto-reset of alarm status	0xFFFFFF
0x03E	0x0BA	Alarm_Set	B24	Y	Sets corresponding alarm bits	0
0x03F	0x0BD	Alarm_Reset	B24	Y	Clears corresponding alarm bits	0
0x040	0x0C0	bucketl	U.24	Y	Bucket Register(s) for Energy Accumulation	0x7780A5
0x041	0x0C3	bucketh	U24	Y	Combined Bucket is a U48.24	0x000247
0x042	0x0C6	PhaseComp	S.21	Y	Phase compensation (high-rate samples)	0
0x043	0x0C9	IrOff	U.23	Y	RMS Current Offset Adjust	0
0x044	0x0CC	VrOff	U.23	Y	RMS Voltage Offset Adjust	0
0x045	0x0CF	POff	U.23	Y	Power Offset Adjust	0
0x046	0x0D2	Reserved	U.21	Y	Reserved	0x20CE70
0x047	0x0D5	igain	U.21	Y	Current Gain Setting	0x200000
0x048	0x0D8	vgain	U.21	Y	Voltage Gain Setting	0x200000
0x049	0x0DB	Ioffs	S.23	Y	Current DC offset.	0
0x04A	0x0DE	Voffs	S.23	Y	Voltage DC offset.	0
0x04B	0x0E1	Tgain	U.24	Y	Die temperature gain setting.	0x0AB331

Address		Name	Data Type	Flash Saved	Description	Default
Word (SPI)	Byte (UART)					
0x04C	0x0E4	Toffs	U.24	Y	Die Temperature offset.	0xFFA800
0x04D	0x0E7	Reserved	S24	Y	Reserved	0
0x04E	0x0EA	Reserved	S24	Y	Reserved	0
0x04F	0x0ED	ISCALE	U24	Y	Current scaling register.	62,000
0x050	0x0F0	VSCALE	U24	Y	Voltage scaling register.	667,000
0x051	0x0F3	PSCALE	U24	Y	Power scaling register.	161,539
0x052	0x0F6	PFSCALE	U24	Y	Power Factor scaling register.	1,000
0x053	0x0F9	FSCALE	U24	Y	Frequency scaling register.	1,000
0x054	0x0FC	TSCALE	U24	Y	Temperature Scaling register.	1,000
0x055	0x0FF	Reserved	U24	Y	Reserved	0
0x056	0x102	AccumCyc	U24	Y	Line Cycles to set Accumulation Interval at	30
0x057	0x105	Accum	U24	Y	Accumulation Interval for low rate calculations (RMS, etc.).	6,700
0x058	0x108	CalCyc	U24	Y	# of accumulation intervals to average in each Calibration Iteration.	4
0x059	0x10B	CalItr	U24	Y	# of Iterations in each Calibration command.	4
0x05A	0x10E	Harm	U24	Y	Harmonic selector.	1
0x05B	0x111	iavgtarget	U24	Y	Average Current target for Calibration.	0
0x05C	0x114	vavgtarget	U24	Y	Average Voltage target for Calibration.	0
0x05D	0x117	irmstarget	U24	Y	RMS Current target for Calibration.	1,000
0x05E	0x11A	vrmstarget	U24	Y	RMS Voltage target for Calibration.	120,000
0x05F	0x11D	powertarget	U24	Y	Active Power target for Calibration.	120,000
0x060	0x120	baud	U24	Y	Baud Rate Register for UART	9,600
0x061	0x123	Reserved	NA	Y	Reserved	NA
0x062	0x126	Reserved	NA	Y	Reserved	NA
0x063	0x129	VHYST	U24	Y	Hysteresis Voltage for ZC detection	0x028F5C
0x064	0x12C	ACDCV	U24	Y	Average Voltage Threshold to Disable HPF	10,000
0x065	0x12F	ACDCI	U24	Y	Average Current Threshold to Disable HPF	100
0x066	0x132	Reserved	NA	Y	Reserved	NA
0x067	0x135	VsurgeTh	U24	Y	Voltage threshold above which VSURGE alarm is activated.	225,000
0x068	0x138	VsagTh	U24	Y	Voltage threshold below which VSAG alarm will be activated.	90,000
0x069	0x13B	VminTh	U24	Y	Voltage threshold below which UNDERVOLT alarm will be activated.	95,000
0x06A	0x13E	VmaxTh	U24	Y	Voltage threshold above which OVERVOLT alarm will be activated.	245,000
0x06B	0x141	VdropTh	U24	Y	Voltage threshold below which VDROPOUT alarm will be activated.	10,000
0x06C	0x144	ImaxTh	U24	Y	Current High Alarm Limit.	15,000
0x06D	0x147	PmaxTh	U24	Y	Power High Alarm Limit.	800,000
0x06E	0x14A	TminTh	S24	Y	Die temperature threshold below which the UNDERTEMP alarm will be activated.	-40,000

Address		Name	Data Type	Flash Saved	Description	Default
Word (SPI)	Byte (UART)					
0x06F	0x14D	TmaxTh	S24	Y	Die temperature threshold above which the OVERTEMP alarm will be activated.	125,000
0x070	0x150	Reserved	U24	Y	Reserved	0
0x071	0x153	FminTh	U24	Y	Line Frequency threshold below which the UNDERFREQ alarm will be activated.	40,000
0x072	0x156	FmaxTh	U24	Y	Line frequency threshold above which the OVERFREQ alarm will be activated.	70,000
0x073	0x159	VDropHold	U24	Y	Number of ADC samples below VdropTh (Threshold) to generate alarm	6
0x074	0x15C	VminHold	U24	Y	# of consecutive accumulation intervals in which the RMS voltage must exceed the specified limit before the UNDERVOLT or OVERVOLT alarms will be activated.	4
0x075	0x15F	ImaxHold	U24	Y	# of consecutive accumulation intervals in which the RMS current must exceed ImaxTh before the OVERCURRENT alarm will be activated.	4
0x076	0x162	PmaxHold	U24	Y	# of consecutive accumulation intervals in which power must exceed the PMAX threshold before the OVERPOWER alarm will be activated.	4
0x077	0x165	TminHold	U24	Y	# of consecutive accumulation intervals in which the die temperature must exceed either TMIN or TMAX before the OVERTEMP or UNDERTEMP alarm will be activated.	4
0x078	0x168	FminHold	U24	Y	# of consecutive accumulation intervals in which the line frequency must exceed either FMIN or FMAX before the UNDERFREQ or OVERFREQ alarm will be activated.	4
0x079	0x16B	TminCnt	U24	N	The number of times an UNDERTEMP event has been detected.	NA
0x07A	0x16E	TmaxCnt	U24	N	The number of times an OVERTEMP event has been detected.	NA
0x07B	0x171	VminCnt	U24	N	The number of times an UNDERVOLT event has been detected.	NA
0x07C	0x174	VmaxCnt	U24	N	The number of times an OVERVOLT event has been detected.	NA
0x07D	0x177	ImaxCnt	U24	N	The number of times an OVERCURRENT event has been detected.	NA
0x07E	0x17A	PmaxCnt	U24	N	The number of times an OVERPOWER event has been detected.	NA
0x07F	0x17D	FminCnt	U24	N	The number of times an UNDERFREQ event has been detected.	NA
0x080	0x180	FmaxCnt	U24	N	The number of times an OVERFREQ event has been detected.	NA
0x081	0x183	VsagCnt	U24	N	The number of times a VSAG event has been detected.	NA
0x082	0x186	VsurgeCnt	U24	N	The number of times a VSURGE event has been detected.	NA

5.3 Scaling Registers

The scaling registers can be used to set the full-scale values and/or choosing the resolution of related parameters and results.

Scaling Register	Registers Affected by Scaling
ISCALE	iavg, irms, irmstarget, iavgtarget, Ifund, Iharm, Ihi, Ilo, Ipeak, ImaxTh
VSCALE	vavg, vrms, vrmstarget, vavgtarget, Vfund, Vharm, Vhi, Vlo, Vpeak, Vsurge, Vsag, Vdrop, VminTh, VmaxTh
PSCALE	Power, powertarget, VA, VAR, avgpower, Pfund, Pharm, Qfund, Qharm, VAfund, VAharm, Pmax
PFSCALE	PF
TSCALE	CTemp, TminTh, TmaxTh
FSCALE	Frequency, Fmin, Fmax

5.3.1 VSCALE

For voltage inputs, full scale (FSV) is defined as the peak system voltage or current that results in +/-250 mVpk at the ADC input. The voltage input is usually scaled down from the AC inlet using a sensing element: resistor divider, voltage transformer, etc. The VSCALE parameters need to be set in order to match the full-scale range of the voltage input with the full-scale range of the sensor.

$$Scaled\ Register\ Value = \left(\frac{\text{Measured Voltage}}{\text{FSV}}\right) * \text{VSCALE}$$

Example: A voltage divider produces an output of 250 mVpk with 667Vpk applied at its input. A resolution of 1 mV is needed. In this case, the value of VSCALE register should be:

$$\text{VSCALE} = 667 * (1/0.001) = 667000$$

Therefore, when the system RMS Voltage is 120Vrms we would expect.

$$Vrms = \left(\frac{\text{RMS Voltage}}{\text{FSV}}\right) * \text{VSCALE} = \left(\frac{120}{667}\right) * 667000 = 120000$$

5.3.2 ISCALE

For current inputs, full scale (FSI) is defined as the peak system current that results in +/-250 mVpk at the ADC input. The current input is connected to current sensing element, generally a low value resistive shunt or current transformer (CT). The ISCALE parameter needs to be set in order to match the full scale range of the current with the full scale range of the sensor. The effective value used for current calculations can be shifted left by 8 (multiplied by 256) from the programed value if the ishift bit is set in the Control register.

$$Scaled\ Register\ Value = \left(\frac{\text{Measured Current}}{\text{FSI}}\right) * \text{ISCALE} * (\text{control. ishift? } 256 : 1)$$

Example: A current shunt produces a voltage drop of 250 mVpk at 62.5Apk (0.004Ohms). A resolution of 1/128mA is needed. In this case the value of ISCALE register should be:

$$\text{ISCALE} = 62.5 * (1/(0.001/128)) = 8000000$$

Therefore, when the system RMS Current is 1.0Arms we would expect:

$$Irms = \left(\frac{\text{RMS Current}}{\text{FSI}}\right) * \text{ISCALE} = \left(\frac{1.0}{62.5}\right) * 8000000 = 128000$$

5.3.3 PSCALE

Full Scale Power is defined as FSI*FSV. The effective value used for Power calculations can be shifted left by 8 (multiplied by 256) from the programed value if the pshift bit is set in the Control register.

$$Scaled\ Register\ Value = \left(\frac{\text{Measured Power}}{\text{FSP}}\right) * \text{PSCALE} * (\text{control. pshift? } 256 : 1)$$

Example: Assuming FSV = 667Vpk and FSI = 62.5Apk then FSP = 41687.5VApk. For a 5mW resolution, PSCALE should be:

PSCALE = 41687.5 * (1/0.005) = 8337500.

Therefore, when the system Active Power is 100W we would expect:

$$Power = \left(\frac{\text{Active Power}}{\text{FSP}}\right) * \text{PSCALE} = \left(\frac{100}{41687.5}\right) * 8337500 = 20000$$

Example: Assuming FSV = 667Vpk and FSI = 62.5Apk then FSP = 41687.5VApk. For a 1mW resolution the normal calculation for PSCALE would be…

PSCALE = 41687.5 * (1/0.001) = 41687500.

This number is too large to fit in a 24 bit value and will not fit in PSCALE. 8388.607 Watts. If the actual system will never go above 8388.607 VAs then by setting pshift=1 the calculation for PSHIFT would be:

PSCALE = 41687.5 * (1/0.001) / 256 =162842

Therefore, when the system Active Power is 100W we would expect:

$$Power = \left(\frac{\text{Active Power}}{\text{FSP}}\right) * \text{PSCALE} * 256 = \left(\frac{100}{41687.5}\right) * 162842 * 256 = 100000$$

5.3.1 PFSCALE

The scaling register for Power Factor does not set full scale values. It only sets resolution.

$$Scaled\ Register\ Value = \text{Measured Power Factor} * P\text{FSCALE}$$

Example: By setting PFSCALE to 100 the value of the power factor is represented in 0.01 per LSB. For a AC load with a Power Factor of 0.5 …

$$PF = \text{Measured Power Factor} * P\text{FSCALE} = 0.5 * 100 = 50$$

5.3.2 TSCALE

The scaling register for Temperature does not set full scale values. It only sets resolution.

$$Scaled\ Register\ Value = \text{Measured Temperature} * \text{TSCALE}$$

Example: By setting TSCALE to 1000 the value of the temperature is represented in 1/1000 of Degree Celsius. For a chip temperature of 27°C, we would expect:

$$CTemp = \text{Measured Temperature} * \text{TSCALE} = 27 * 1000 = 27000$$

5.3.3 FSCALE

The scaling register for Frequency does not set full scale values. It only sets resolution.

$$Scaled\ Register\ Value = \text{Measured Frequency} * \text{FSCALE}$$

Example: By setting FSCALE to 100 the value of the frequency is represented in 1/100 of Hz. For a AC source voltage frequency of 60Hz…

$$Frequency = \text{Measured Frequency} * \text{FSCALE} = 60 * 100 = 6000$$

5.4 Control Register

This register is used to control the basic operating modes of the SY7T609+S1.

Table 5-2. Control Register

Bit(s)	Name	Description	Default
23:19	NA	Reserved. **Set to 0**	0
18	ishift	ISCALE shift: 1=ISCALE<<8; 0=ISCALE To allow more range in allowed ISCALE values the device will effectively use ISCALE<<8 for scaling calculations if ishift=1.	0
17	negpower	Negative Active Power not allowed. 1= P← MAX(P,0); 0= P← P;	0
16	Reserved	Reserved. **Set to 0**	0
15	swapi	Swap Current Input: 1= V← (AIN-AIP); 0= V←(AIP-AIN)	0
14	swapv	Swap Voltage Input: 1= V← (AVN-AVP); 0= V←(AVP-AVN)	0
13	acdci	Auto Current HPF Control: 1=Automatic control; 0=use hpfi if (control.acdci==1) then { if (abs(iavg)<acdci) then hpfi =1 else hpfi = 0}	0
12	acdcv	Auto Voltage HPF Control: 1=Automatic control; 0=use hpfv if (control.acdcv==1) then { if (abs(vavg)<acdcv) then hpfv =1 else hpfv = 0}	1
11	pshift	PSCALE shift: 1=PSCALE<<8; 0=PSCALE To allow more range in allowed PSCALE values the device will effectively use PSCALE<<8 for scaling calculations if pshift=1.	1
10	ct	Stop chip/die temperature update: 1=stop update; 0=update. This bit prevents the firmware from overwriting the CTemp (temperature result) register. This is necessary when supplying a known temperature for calibration.	0
9	arrst	Set Auto-Report (ar) on reset. 1 = will set the ar bit to 1 on device reset regardless of saved ar value.	0
8:5	Reserved	Reserved. **Set to 0**	0
4	tc	Enable Gain/Temperature compensation 1=enable; 0=disable. This bit allows the firmware to modify the system gain based on measured chip temperature.	1
3	ar	Enable Auto Reporting 1=enable; 0=disable. This bit enables or disables auto reporting mode on the UART interface.	0
2	Reserved	Reserved. **Set to 1**	1
1	hpfi	Current HPF; 1=enable; 0=disable.	0
0	hpfv	Voltage HPF; 1=enable; 0=disable.	1

5.5 Command Register

This register is used to issue commands to perform specific tasks to the SY7T609+S1.

5.5.1 Save to Flash Command

Use this command to save to flash the calibration coefficients and system defaults contained in the some of the input registers. Upon reset or power-on, the values stored in flash will become new system defaults. The following table describes the command bits:

Table 5-3. Command Register, Save to Flash

Bit(s)	Value	Description
23:12	0xACC	“Access” Command.
11:0	0x200	2: Save Calibration to flash.

5.5.2 Auto Reporting Command

Use this command to enable or disable auto reporting mode. When the device is in Auto Reporting mode a read-modify-write of the Control register to stop auto reporting is generally unreliable. This command provides a way to set/clear the ar bit without directly accessing the Control register. The following table describes the command bits:

Table 5-4. Command Register Auto-Reporting

Bit(s)	Value	Description
23:16	0xAE	Auto Reporting Command
15:0		0x000 = Clear Control.ar 0x001 = Set Control.ar

5.5.3 Clear Energy Counters

Use this command to clear all energy counters. The following table describes the command bits:

Table 5-5. Command Register Clear Energy Counters

Bit(s)	Value	Description
23:0	0xEC0000	Clear All Energy Counters

5.5.4 Soft-Reset

Use this command invoke a reset. Note that it resets the program counter only and not the HW. The following table describes the command bits:

Table 5-6. Command Register Soft-Reset

Bit(s)	Value	Description
23:0	0xBD0000	Invoke Soft-Reset

5.5.5 Calibration Command

The Calibration Command starts the calibration process. It is assumed that appropriate input signals are applied and target values set before starting calibration.

When the calibration process completes, bits 23:16 are cleared. If the calibration has completed without a detected error bits 15:0 are also cleared. If an error is detected during the calibration the bit associated with the offending calibration routine is left set. All selected calibration routines run in parallel over CalItr iterations that are each CalCyc accumulation intervals long.

Table 5-7. Command Register, Calibration Command

Bit(s)	Value	Description
23:16	0xCA	“Calibrate” Command.
15:19	0x00	Reserved
8	power	Calibrate Current Gain using powertarget.
7	0	Reserved
6	0	Reserved
5	vrms	Calibrate Voltage Gain using vrmstarget.
4	irms	Calibrate Current Gain using irmstarget.
3	voffs	Calibrate Voltage Offset using vavgtarget.
2	ioffs	Calibrate Current Offset using iavgtarget.
1	0	Reserved.
0	ctemp	Calibrate Chip Temperature.

5.5.6 Clear Flash Storage 0 Command

Use this command to clear the flash coefficients (nonvolatile system defaults for some of the input registers). Upon reset or power-on, the values revert to factory system defaults. When the process completes, bits [23:8] are cleared.

Table 5-8. Clear Flash Storage 0 Command Bits

Bit(s)	Value	Description
23:12	0xACC	“Access” Command
11:8	0x0	Clear nonvolatile values in flash
7:0	—	See General Settings (0x00xxxx)

5.5.7 Clear Flash Storage 1 Command

Use this command to clear the flash coefficients (nonvolatile system defaults for some of the input registers). Upon reset or power-on, the values revert to factory system defaults. This command should always be used in conjunction with Clear Flash Storage 0 Command (0xACC0xx). When the process completes, bits [23:8] are cleared.

Table 5-9. Clear Flash Storage 1 Command Bits

Bit(s)	Value	Description
23:12	0xACC	“Access” Command
11:8	0x1	Clear nonvolatile values in flash
7:0	—	See General Settings (0x00xxxx)

5.6 UART Protocols

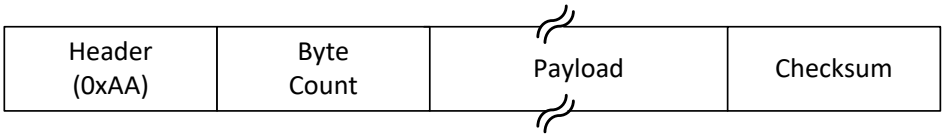
The SY7T609+S1 firmware implements a “simple serial interface” (SSI) protocol on the UART interface. While the protocol supports multi-point communications, the SY7T609+S1 firmware sets the device for single point (Single Target Mode). The protocol includes data integrity check.

The protocol also includes an auto-report mode. This mode allows the SY7T609+S1 to autonomously send packets at the completion of the accumulation intervals.

5.6.1 Command-Response Mode

In this protocol, the host is the master and must initiate communications. The master should first set the device’s register address pointer before performing read or write operations.

After sending the synchronization header code (0xAA), the master sends (in the following order) the byte counts (bytes in payload), the payload and then the checksum that provides data integrity check. The following figure shows a generic command packet generated from the master:



The payload contains commands, registers address, data etc. The payload can contain either a single command or multiple commands. The protocol allows for reading or writing one up to 252 bytes in a single operation. Following is the data access method for both read and write. Only the payload is shown.

Register Address Pointer Selection

The following message sets the address pointer to the register (or set of registers) to read or write:

PAYLOAD	
0xA3 Command	Register Address (2 Bytes)

The SY7T609+S1 replies with an acknowledge message.

Read Command

It is possible to read data from the SY7T609+S1 using the 0xE command. To read 0 to 15 bytes, the command byte is completed with the number of bytes to read. For example, to read 3 bytes:

PAYLOAD
0xE3 Command

In order to read a larger number of bytes (up to 255), the command 0xE0 must be used. In this case, the command 0xE0 must be followed by a byte containing the number of bytes to be read. For example to read 31 bytes:

PAYLOAD	
0xE0 Command	0x1F (Number of Bytes to Read)

Write Command

It is possible to write data to the SY7T609+S1 using the 0xD command. To write 1 to 15 bytes, the command byte must be completed with the number of bytes of data to write. For example to write 3 bytes:

PAYLOAD	
0xD3 Command	Data (Number of Bytes = 3)

In order to write a larger number of bytes (up to 255), the command 0xD0 must be used. In this case, the number of data bytes to follow is determined by the Byte Count. For example, to write 31 bytes:

PAYLOAD	
0xD0 Command	Data (Number of Bytes = Byte Count – 4)

After each read or write operation, the internal address pointer is incremented to point to the address that followed the target of the previous read or write operation.

Summary of Commands

Table 5-10: Host SSI Commands

Command	Parameters	Description
0 - 7F		(invalid)
80 - 9F		(not used)
A0		Clear address
A1	[byte-L]	Set Read/Write address bits [7:0]
A2	[byte-H]	Set Read/Write address bits [15:8]
A3	[byte-L][byte-H]	Set Read/Write address bits [15:0]
A4 - AF		(reserved for larger address targets)
B0 - BF		(not used)
C0		De-select Target (target will Acknowledge)
C1 - CE		Select target 1 to 14
CF	[byte]	(reserved for multi-point communications)
D0	[data...]	Write bytes set by remainder of Byte Count
D1 - DF	[data...]	Write 1 to 15 bytes
E0	[byte]	Read 0 to 255 bytes
E1 – EF		Read 1 to 15 bytes
F0 - FF		(not used)

Slave Packets

The SY7T609+S1 replies to the host processor either with an acknowledge (either ACK or NACK) or with data. The format of slave packets depends upon the type of response to the master device. The table below lists the reply codes and their meanings.

Table 5-11: Slave Reply Codes

Code	Definition
0xAA	Acknowledge with data.
0xAE	Auto Reporting Header (with data).
0xAD	Acknowledge without data.
0xB0	Negative Acknowledge (NACK).
0xBC	Command not implemented.
0xBD	Checksum failed.
0xBF	Buffer overflow (or packet too long).
- timeout -	Any condition too difficult to handle with a reply.

5.6.2 Auto-Reporting Mode

By default, the SY7T609+S1 automatically reports a set of data at the completion of each accumulation interval. This mode is used in systems where the host will not have to poll the SY7T609+S1 for data but it receives automatically data updated at the accumulation interval rate. Table 5-12 shows the default auto-reported data format.

Table 5-12: Default Measurements

Parameter/Register	Number of Bytes	Description
Packet Header(0xAE)	1	Start of Data Packet
Packet Length(0x21)	1	Number of Bytes in the Packet
Chip Temperature	3	Chip Temperature
Frequency	3	Line Frequency
Vavg	3	Avg Voltage
Iavg	3	Avg Current
Vrms	3	RMS Voltage
Irms	3	RMS Current
Power	3	Active Power
VAR	3	Reactive Power
VA	3	Apparent Power
PF	3	Power Factor (address 0x27)
CHKSUM	1	Check Sum

The content of the auto-reported data packet is configurable by the user. Refer to the relevant application note describing the auto-report packet configuration procedure.

5.7 Indirect Register Access

The indirect access method supplies a set of memory locations in a user accessible address space which allows reliable access to a larger memory space using any serial interface than might otherwise be available.

Registers

The indirect method is implemented using several registers in user accessible space. The location of these registers may be solution dependent.

Table 5-13: Indirect Access Registers

Register Name	Access Type	Description
IND_RD_ADDR	RD/WR	Indirect Read Address and Control
IND_RD_DATA	R	Indirect Read Data
IND_WR_DATA	W	Indirect Write Data
IND_WR_ADDR	RD/WR	Indirect Write Address and Control

Indirect Read Access

The solution supplies a method for indirect read access to the device memory. The firmware will write the contents of IND_RD_DATA with the content of the device memory at the word address indicated by (IND_RD_ADDR and 0x00FFFF). That value (IND_RD_ADDR and 0x00FFFF) is then written back into IND_RD_ADDR to indicate the read has completed. The check/action for the contents of IND_RD_ADDR is performed at every high rate sample.

Indirect Write Access

The solution supplies a method for indirect write access to the device memory. If any of the upper 8 bits of IND_WR_ADDR are nonzero, the firmware writes the contents of IND_WR_DATA into the word address indicated by (IND_WR_ADDR and 0x00FFFF). That value (IND_WR_ADDR and 0x00FFFF) is then written back into IND_WR_ADDR to indicate the write has completed. The check/action for the contents of IND_WR_ADDR is performed at every high rate sample.

6 Electrical Specifications

6.1 Absolute Maximum Ratings

Supplies and Ground Pins:	
V_{3P3D}, V_{3P3A}	-0.5V to 4.6V
GNDD, GNDA	-0.5V to +0.5V
Analog Input Pins:	
AIN1, AIN2N, AIN2P, MFIO	-10mA to +10mA -0.5V to (V_{3P3} + 0.5V)
Digital Pins:	
MFIO, DIO8, DIO7, DIO5, DIO3, DIO2, DIO1	-30mA to +30mA, -0.5V to (V_{3P3D}+ 0.5V)
Temperatures:	
Operating Junction Temperature (peak, 100ms)	+140°C
Operating Junction Temperature (continuous)	+125°C
Storage Temperature	-45°C to +165°C
Soldering Temperature (10-second duration)	+250°C
ESD Stress on All Pins	±4kV

Stresses beyond Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltages are with respect to GND.

6.2 Recommended Operating Conditions

Parameter	Condition	Min	Typ	Max	Unit
3.3V Supply Voltage (V_{3P3})	Normal Operation	3.0	3.3	3.6	V
Operating Temperature		-40	–	+85	ºC

6.3 Performance Specifications

Note that production tests are performed at room temperature.

6.3.1 Input Logic Levels

Parameter	Condition	Min	Typ	Max	Unit
Digital high-level input voltage, V_{IH}		2	–	–	V
Digital low-level input voltage, V_{IL}		–	–	0.8	V

6.3.2 Output Logic Levels

Parameter	Condition	Min	Typ	Max	Unit
Digital high-level output voltage V_{OH}	I_{LOAD} = 1 mA	V_{3P3} –0.4	–	–	V
	I_{LOAD} = 10 mA	V_{3P3}-0.6	–	–	V
Digital low-level output voltage V_{OL}	I_{LOAD} = 1 mA	0	–	0.4	V
	I_{LOAD} = 10 mA	–	–	0.5	V

6.3.3 Supply Current

Parameter	Condition	Min	Typ	Max	Unit
V_{3P3D} and V_{3P3A} current (compounded)	Normal Operation, V3P=3.3V	–	8.1	10.3	mA

6.3.4 Internal RC Oscillator

Parameter	Condition	Min	Typ	Max	Unit
Nominal Frequency	V3P=3.3V, 25ºC	–	20.000	–	MHz
Accuracy		–	±1.5	–	%

6.3.5 ADC Converter, V_{3P3} Referenced

LSB values do not include the 9-bit left shift at processor input.

Parameter	Condition	Min	Typ	Max	Unit
Usable Input Range (Vin-V_{3P3})		-250	–	250	mV peak
THD (First 10 harmonics)	Vin=65Hz, 64kpts FFT, Blackman-Harris window	–	-85	–	dB
Input Impedance	Vin=65Hz	30	–	90	kΩ
Temperature coefficient of Input Impedance	Vin=65Hz	–	1.7[1]	–	Ω/°C
ADC Gain Error vs %Power Supply Variation $\frac{10^6 \Delta Nout_{PK}\, 357nV/V_{IN}}{100\, \Delta V3P3A/3.3}$	Vin=200mVpk, 65Hz V_{3P3}=3.0V, 3.6V	–	–	50	ppm/%
Input Offset (Vin-V_{3P3})		-10		10	mV

[1] Guaranteed by design, not subject to test.

6.4 Timing Specifications

6.4.1 SPI Slave Port

Parameter		Condition	Min	Typ	Max	Unit
t_{SPIcyc}	SPCK cycle time		1	–	–	µs
$t_{SPILead}$	Enable lead time		15	–	–	ns
t_{SPILag}	Enable lag time		0	–	–	ns
t_{SPIW}	SPCK pulse width: High Low		 250 250	–	–	 ns ns
t_{SPISCK}	SSB to first SPCK fall	Ignore if SPCK is low when SSB falls.	–	2[1]	–	ns
t_{SPIDIS}	Disable time		–	0[1]	–	ns
t_{SPIEV}	SPCK to Data Out (MISO)			–	25	ns
t_{SPISU}	Data input setup time (MOSI)		10	–	–	ns
t_{SPIH}	Data input hold time (MOSI)		5	–	–	ns

[1] Guaranteed by design, not subject to test.

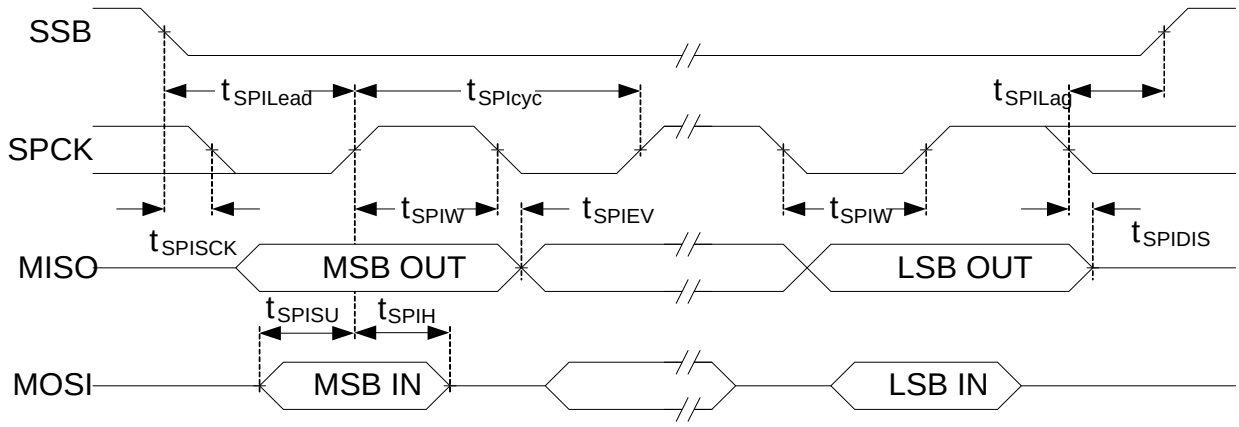
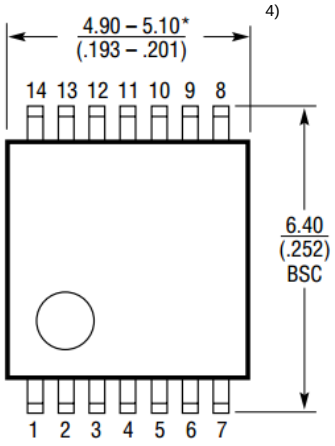
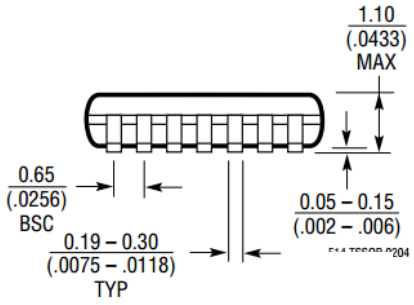


Figure 6-1: SPI Slave Port Timing

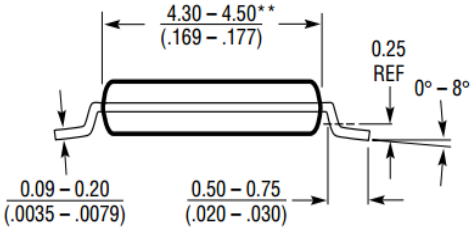
7 Package Outline Drawing



TOP-VIEW



SIDE-VIEW



FRONT-VIEW

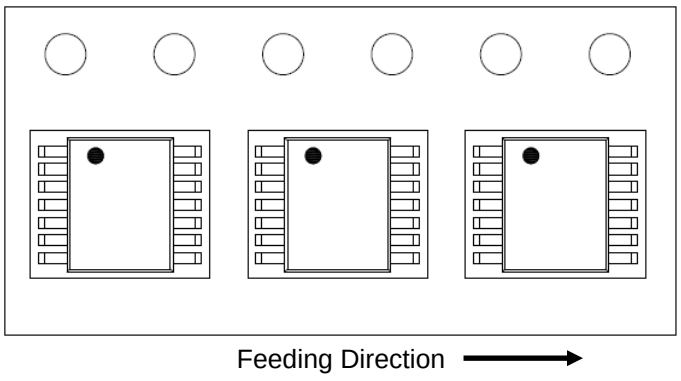
NOTES:

- Dimensions are in Millimeters/(Inches)
- Controlling Dimensions: Millimeters
- Drawing not to scale
- Dimensions not including mold-flash.

  Mold-flash not to exceed 0.152mm (.006'') per side.
- Dimensions do not include interlead flash.

  Interlead flash not to exceed 0.254mm (0.010'') per side

7.1 Tape & Reel Orientation



8 Contact Information

For more information about the SY7T609, contact support.em@silergy.com

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
1	4/17	Initial public release	--
1.1	4/17	Correction to pin names	5
1.2	8/17	Corrections to SPI timing diagrams and register defaults	10-11, 26-29