



MULTI-INNO TECHNOLOGY CO., LTD.

OLED MODULE SPECIFICATION

Model : MI12864PO

Revision	1.1
Engineering	
Date	
Our Reference	

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REVISION RECORD

REV.	REVISION DESCRIPTION	REV.DATE	PAGE
1.0	First Issue	2008-03-17	All
1.1	Modify PIN order of section 4 Mechanical Drawing and section 13 Contact us	2008-08-05	P5, P21

1 Overview

MI12864PO is an OLED monochrome 128×64 dot matrix display module. The characteristics of this display module are high brightness, self-emission, high contrast ratio, slim/thin outline, wide viewing angle, wide temperature range, and low power consumption.

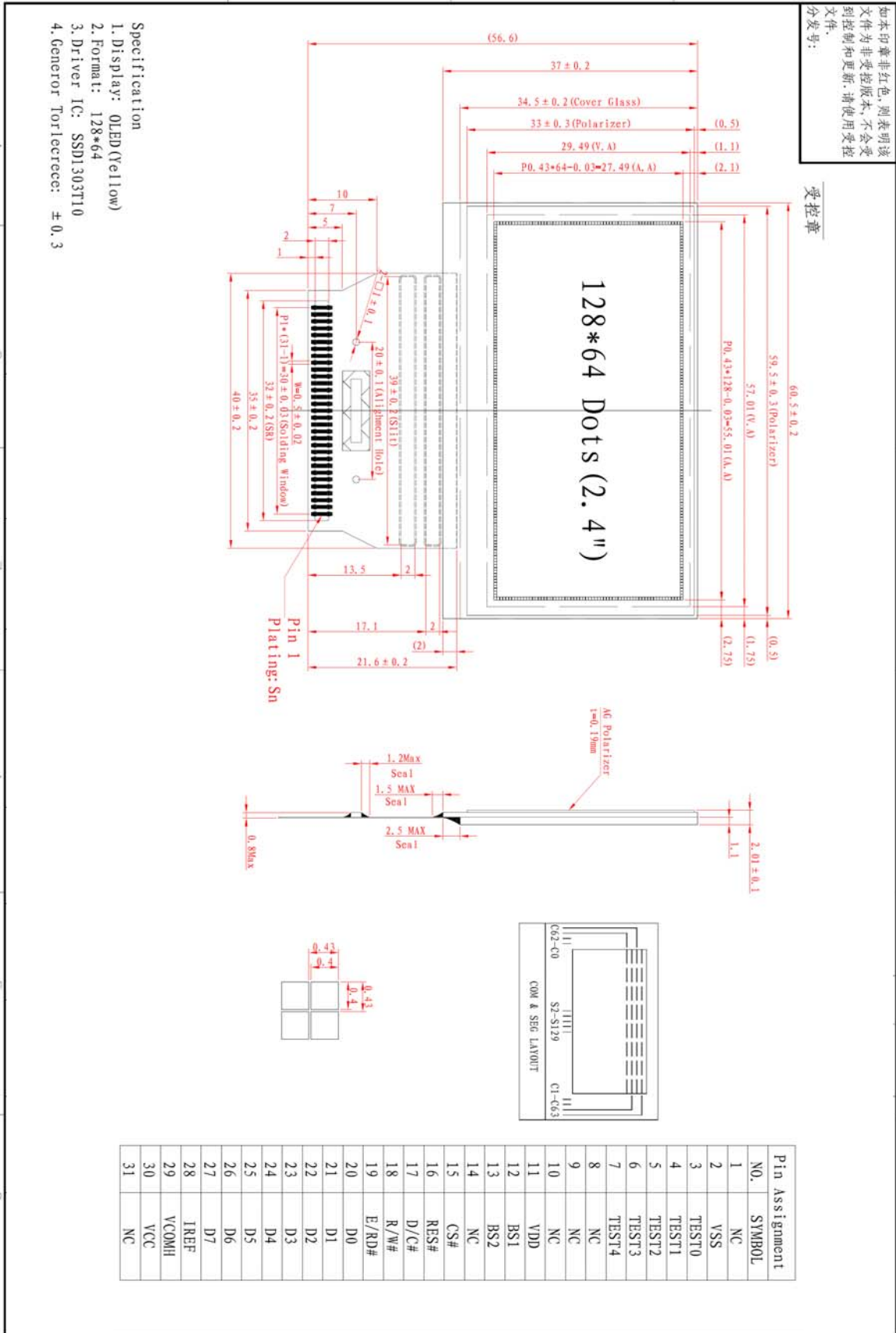
2 Features

- High contrast ratio
- Color: Yellow
- 128×64pixels
- Wide viewing angle
- Wide range of operating temperature
- low power consumption
- 8-bit 8080-Databus or 8-bit 6800-series parallel interface or series peripheral interface or I²C interface.
- Display data is stored in Display Data RAM from MPU
- Built-in SSD1303 standard OLED controller

3 Mechanical Data and Part Number

NO.	ITEM	SPECIFICATION	UNIT
1	Dot Matrix	128(W) x 64(rows)	-
2	Dot Size	0.4(W) x 0.4 (H)	mm
3	Dot Pitch	0.43 (W) x 0.43 (H)	mm
4	Aperture Rate	86	%
5	Active Area	55.01 (W) x 27.49 (H)	m ²
7	Module Size	60.5 (W) x 56.6 (H) x 2.01(D)	mm
8	Polarizer	with	
9	Duty	1/64	

4 Mechanical Drawing

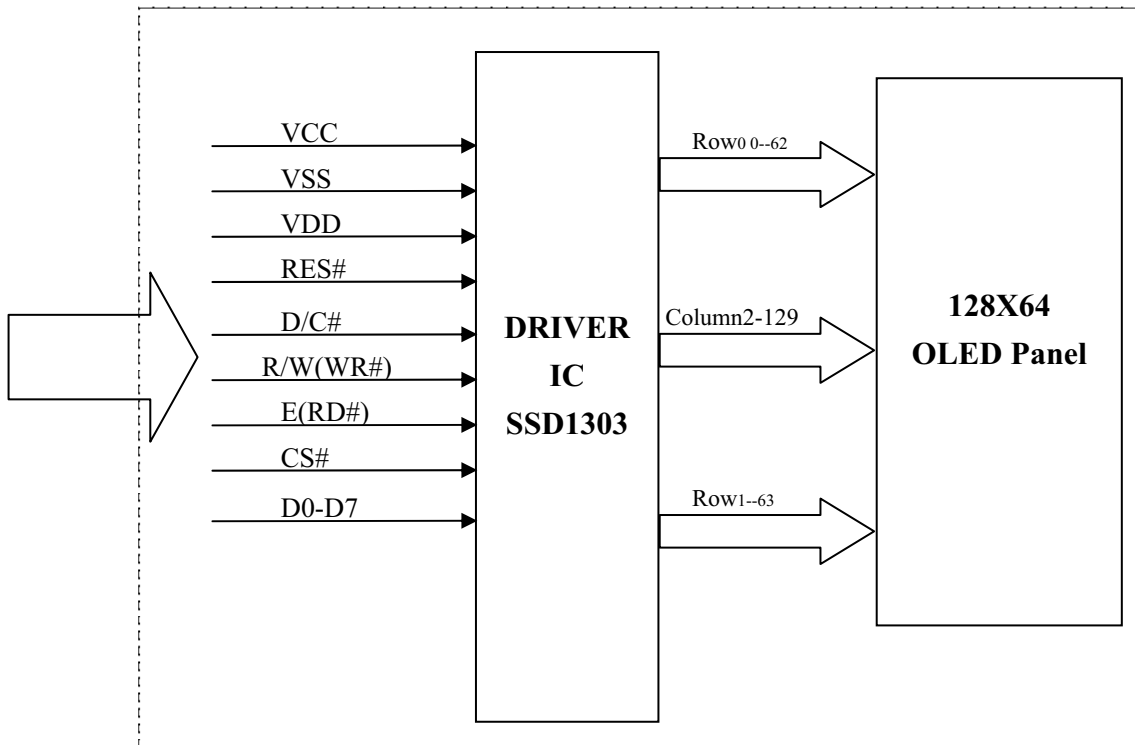


5 Module Interface

PIN NO	PIN NAME	DESCRIPTION															
1	NC	No Connection															
2	VSS	Ground															
3	Test0	Reserved pin; No connection and left float.															
4	Test1																
5	Test2																
6	Test3																
7	Test4																
8	NC	No connection															
9	NC																
10	NC																
11	VDD	Power supply for interface logic level. It should be match with MCU interface voltage level. VDDIO must always be equal or lower than VDD.															
12	BS1	These are MCU interface input selection pins. See the following table for selecting different interfaces: <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Pin Name</th> <th>I2C Interface</th> <th>6800-parallel Interface</th> <th>8080-parallel interface</th> <th>Serial interface</th> </tr> </thead> <tbody> <tr> <td>BS1</td> <td>1</td> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>BS2</td> <td>0</td> <td>1</td> <td>1</td> <td>0</td> </tr> </tbody> </table>	Pin Name	I2C Interface	6800-parallel Interface	8080-parallel interface	Serial interface	BS1	1	0	1	0	BS2	0	1	1	0
Pin Name	I2C Interface		6800-parallel Interface	8080-parallel interface	Serial interface												
BS1	1		0	1	0												
BS2	0	1	1	0													
13	BS2																
14	NC	No Connection															
15	CS#	Chip Select, active low															
16	RES#	Reset, active low															
17	D/C#	Data/Command Select. This is the Data/Command control pin. When it is pulled HIGH, the input at D7-D0 is treated as display data. When it is pulled LOW, the input at D7-D0 is transferred to the command registers. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams.															
18	R/W(WR#)	This is a MCU interface input pin. When 6800-series Parallel Interface mode is selected, this pin is used as Read/Write (R/W) selection input. Pull this pin to HIGH for read mode and pull it to LOW for write mode. When 8080-series Parallel Interface mode is selected, this pin is used as Write (WR#) selection input. Pull this pin to LOW for write mode. Data write operation is initiated when this pin is pulled LOW and the CS# is pulled LOW.															
19	E(RD#)	This is a MCU interface input pin. When 6800-series Parallel Interface is selected, this pin is used as Enable (E) signal. Read/Write operation is initiated when this pin is pulled HIGH and the CS# pin is pulled LOW. When 8080-series Parallel Interface is selected, this pin is used to receive the Read Data (RD#)signal. Data read operation is initiated when this pin is pulled LOW and CS# pin is pulled LOW.															
20-27	D0-D7	These are 8-bit bi-directional data bus to be connected to the microprocessor's data bus. When serial interface mode is selected, D1 will be the serial data input, SDIN, and D0 will be the serial clock input, SCLK.															
28	IREF	This is a segment current reference pin. A resistor should be connected between this pin and VSS. Set the current at 10uA.															
29	VCOMH	This is an input pin for the voltage output high level for COM signals. A capacitor should be connected between this pin and VSS.															
30	VCC	OLED drive voltage, It should be supplied externally.															
31	NC	No Connection															

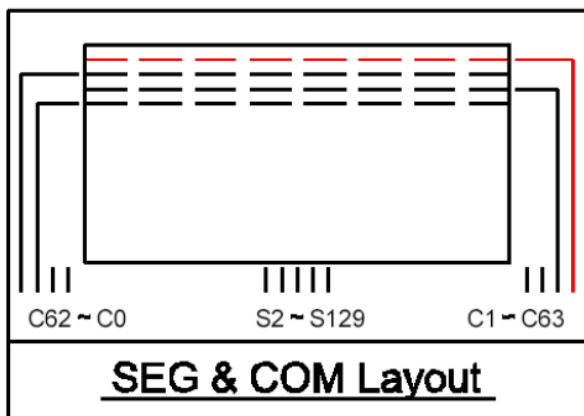
6 Function Block Diagram

6.1 Function Block Diagram



NOTE: Some pins omitted

6.2 PANEL LAYOUT DIAGRAM



7 Absolute Maximum ratings

ITEM	Symbol	MIN	MAX	Unit	Conditions	Remark
Logic supply voltage	V _{DD}	-0.3	+3.5	V	Ta = 25 °C	IC maximum rating
OLED Operating voltage	V _{CC}	8	+16	V	Ta = 25 °C	IC maximum rating
Operating Temp.	Top	-40	+80	°C		
Storage Temp	Tstg	-45	+85	°C		
Life Time		40,000			100 cd/m ² , 50% checkerboard	Note(1)
Life Time		50,000			80 cd/m ² , 50% checkerboard	Note(2)
Life Time		66,000			60 cd/m ² , 50% checkerboard	Note(3)

Note:

(A) Under V_{CC} = 13V, Ta = 25°C, 50% RH.

(B) Life time is defined the amount of time when the luminance has decayed to less than 50% of the initial measured luminance.

(1) Setting of 100 cd/m²:

- Contrast setting : 0XC5
- Frame rate : 105Hz
- Duty setting : 1/64

(2) Setting of 80 cd/m²:

- Contrast setting : 0x8F
- Frame rate : 105Hz
- Duty setting : 1/64

(3) Setting of cd/m²:

- Contrast setting : 0x4C
- Frame rate : 105Hz
- Duty setting : 1/4

8 Electrical Characteristics

8.1 DC Electrical Characteristics

ITEM	Symbol	Test condition	MIN	TYPE	MAX	Unit
Logic Supply Voltage	V_{DD}	Ta=-20°C to +70°C	2.4	2.7	3.5	V
OLED Driver Supply Voltage	V_{CC}	Ta=-20°C to +70°C	12.5	13	13.5	V
Operating Current for V_{DD}	I_{DD}	Contrast=FF	-	190	300	μA
Operating Current for V_{PP}	I_{CC}	Contrast=FF	-	550	1000	μA
High-level Input Voltage	V_{IH}		$0.8 \cdot V_{DD1}$	-	-	V
Low-level Input Voltage	V_{IL}		0	-	$0.2 \cdot V_{DD1}$	V
High-level Output Voltage	V_{OH}	-	$0.9 \cdot V_{DD1}$	-	-	V
High-level Output Voltage	V_{OL}	-	0	-	$0.1 \cdot V_{DD1}$	V

Note 1: $V_{DD} = 2.7V$, $V_{CC} = 13V$, Frame Rate = 105Hz, No panel attached.

Note 2: The V_{CC} input must keep in a stable value; ripple and noise are not allowed.

8.2 Electro-optical Characteristics

Item	Symbol	Test condition	MIN	TYPE	MAX	Unit
Normal mode Power consumption		All pixels on(1)			400	mW
Standby mode Power consumption		Standby mode 10% pixels on(2)			45	mW
Brightness	L_{br}	With polarizer	60	80	-	cd/m^2
C.I.E(Yellow)	(x)	x,y(CIE1931)	0.43	0.47	0.51	
	(y)		0.45	0.49	0.53	
Dark room contrast	CR		2000:1	-	-	
View angle			160			degree

(1) Normal mode condition

- Driving Voltage : 13V
- Contrast setting : 0x8F
- Frame rate : 105Hz
- Duty setting : 1/64

(2) Standby mode condition

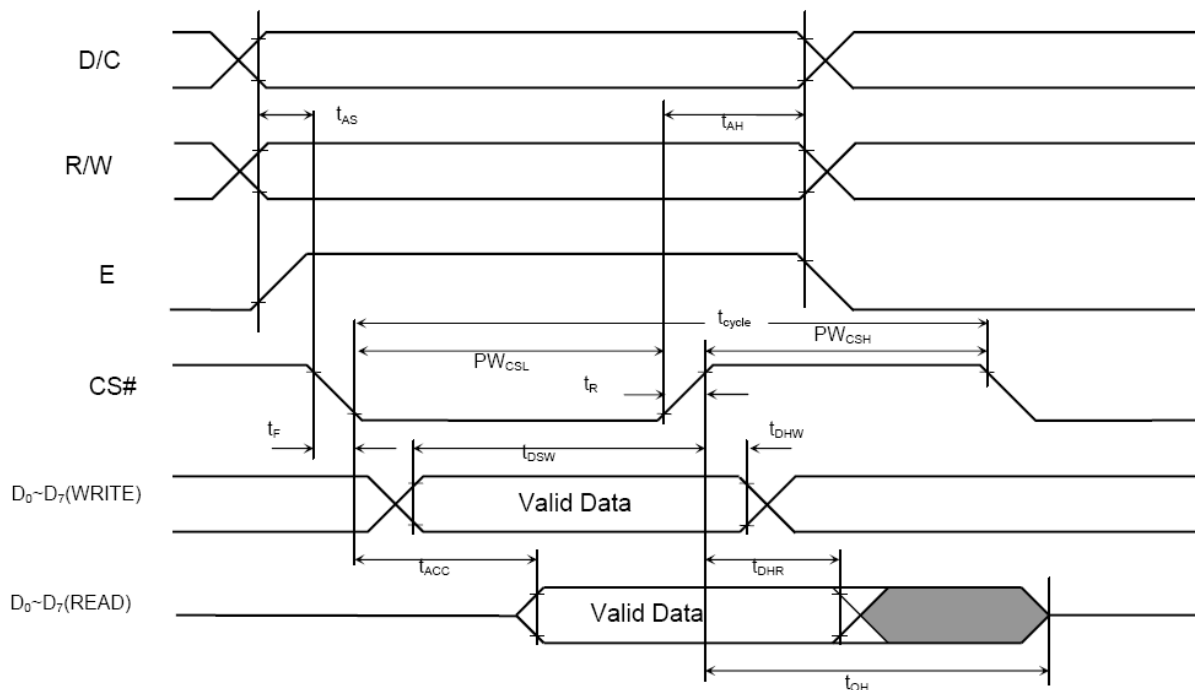
- Driving Voltage : 13V
- Contrast setting : 0x00
- Frame rate : 105Hz
- Duty setting : 1/64

8.3 AC Electrical Characteristics

6800-Series MPU Parallel Interface Timing Characteristics

(TA =25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	40	ns
t_F	Fall Time	-	-	40	ns

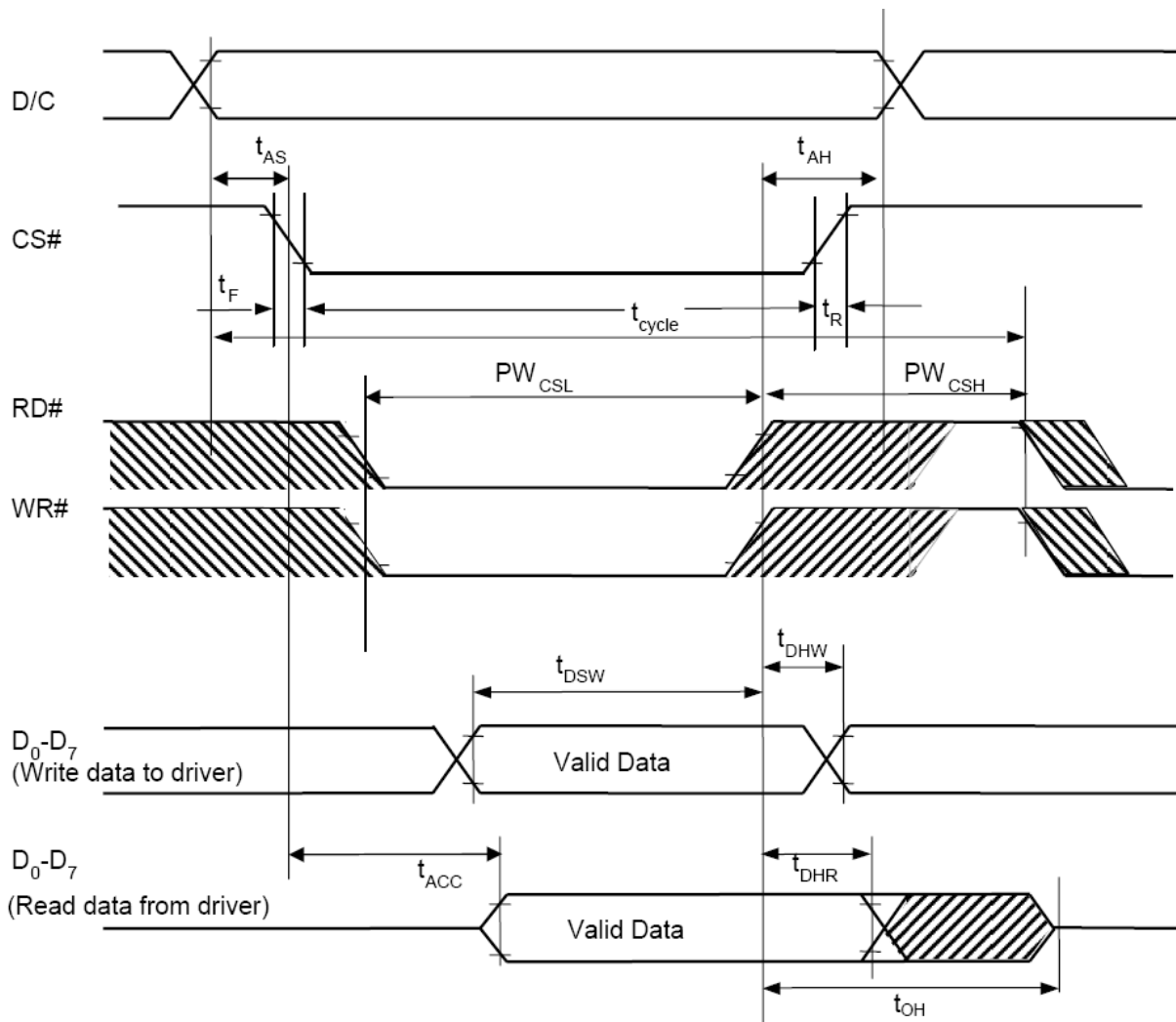


6800-series MPU parallel interface characteristics

8080-Series MPU Parallel Interface Timing Characteristics

(TA = 25°C)

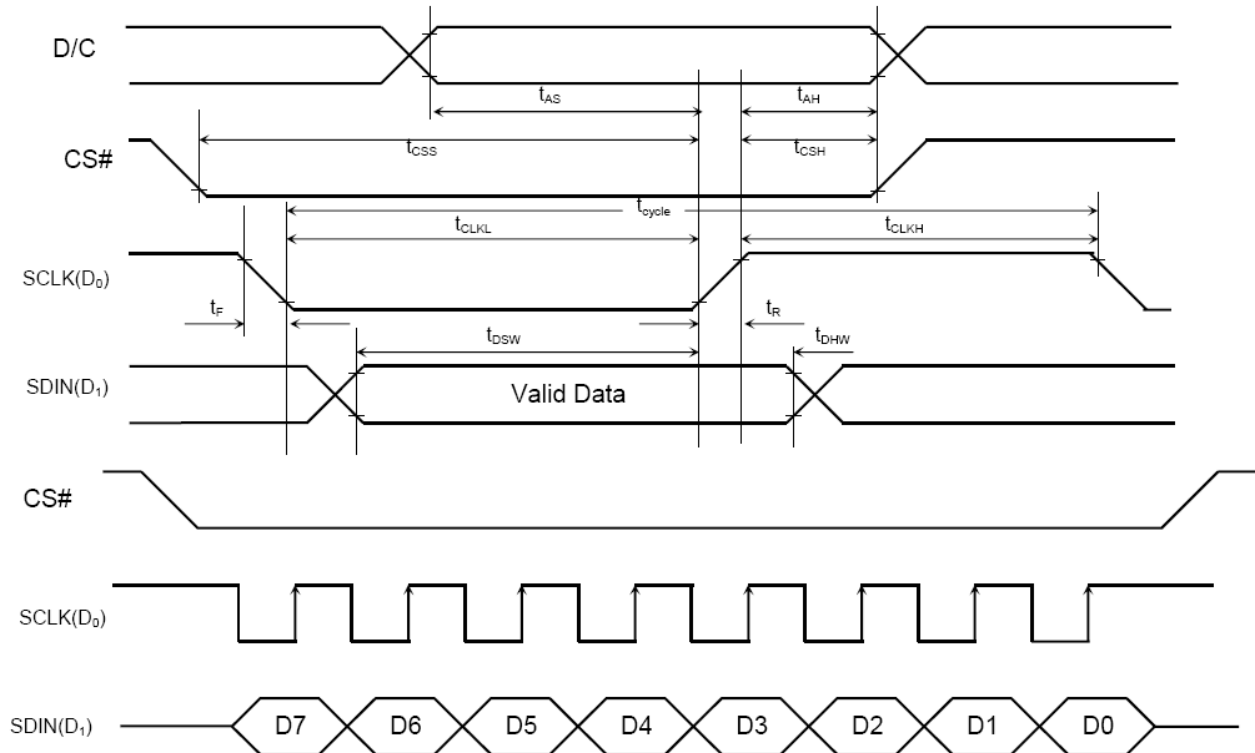
Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read)	150	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read)	60	-	-	ns
	Chip Select High Pulse Width (write)	60	-	-	ns
t_{R}	Rise Time	-	-	40	ns
t_{F}	Fall Time	-	-	40	ns


8080-series MPU parallel interface characteristics

Serial Interface Timing Characteristics

(TA = 25°C)

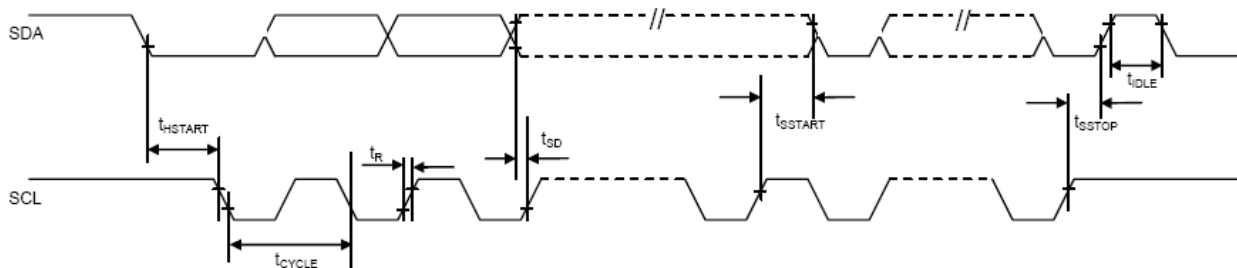
Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	250	-	-	ns
t_{AS}	Address Setup Time	150	-	-	ns
t_{AH}	Address Hold Time	150	-	-	ns
t_{CSS}	Chip Select Setup Time	120	-	-	ns
t_{CSH}	Chip Select Hold Time	60	-	-	ns
t_{DSW}	Write Data Setup Time	100	-	-	ns
t_{DHW}	Write Data Hold Time	100	-	-	ns
t_{CLKL}	Clock Low Time	100	-	-	ns
t_{CLKH}	Clock High Time	100	-	-	ns
t_R	Rise Time	-	-	40	ns
t_F	Fall Time	-	-	40	ns


Serial interface characteristics

I²C Interface Timing Characteristics

(TA = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	2.5	-	-	us
t_{HSTART}	Start condition Hold Time	0.6	-	-	us
t_{SD}	Data Setup Time	100	-	-	ns
t_{SSTART}	Start condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	-	us
t_{SSTOP}	Stop condition Setup Time	0.6	-	-	us
t_{R}	Rise Time for data and clock pin	-	-	300	ns
t_{IDLE}	Idle Time before a new transmission can start	1.3	-	-	us

I²C Interface Timing Characteristics


9 Display Control Instruction

Command table (D/C =0, R/W (WR#)=0, E (RD#)=1)

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	00~0F	0	0	0	0	X ₃	X ₂	X ₁	X ₀	Set Lower Column Address **	Set the lower nibble of the column address register using X ₃ X ₂ X ₁ X ₀ as data bits. The initial display line register is reset to 0000b after RESET.
0	10~1F	0	0	0	1	X ₃	X ₂	X ₁	X ₀	Set Higher Column Address **	Set the higher nibble of the column address register using X ₃ X ₂ X ₁ X ₀ as data bits. The initial display line register is reset to 0000b after RESET.
0 0 0 0 0	26 A[2:0] B[2:0] C[1:0] D[2:0]	0 * * * *	0 * * * *	1 * * * *	0 * * * *	0 * * * *	1 A ₂ B ₂ * D ₂	1 A ₁ B ₁ * D ₁	0 A ₀ B ₀ C ₀ D ₀	Horizontal scroll setup	A[2:0] Set the number of column scroll per step Valid value: 001b, 010b, 011b, 100b B[2:0] Define start page address C[1:0] Set time interval between each scroll step in terms of frame frequency D[2:0] Define end page address Set the value of D[2:0] larger or equal to B[2:0] 00b – 12 frame 01b – 64 frames 10b – 128 frames 11b – 256 frames
0	2F	0	0	1	0	1	1	1	1	Activate horizontal scroll	Start horizontal scrolling
0	2E	0	0	1	0	1	1	1	0	Deactivate horizontal scroll	Stop horizontal scrolling
0	40~7F	0	1	X ₅	X ₄	X ₃	X ₂	X ₁	X ₀	Set Display Start Line	Set display RAM display start line register from 0-63 using X ₅ X ₃ X ₂ X ₁ X ₀ . Display start line register is reset to 000000 during RESET
0 0	81 A[7:0]	1 A ₇	0 A ₆	0 A ₅	0 A ₄	0 A ₃	0 A ₂	0 A ₁	1 A ₀	Set Contrast Control Register **	Double byte command to select 1 out of 256 contrast steps. Contrast increases as the value increases. (RESET = 80h)
0 0	82 A[7:0]	1 A ₇	0 A ₆	0 A ₅	0 A ₄	0 A ₃	0 A ₂	1 A ₁	0 A ₀	Brightness for color banks	Double byte command to select 1 out of 256 brightness steps. Brightness increases as the value increases. (RESET = 80h)
0 0 0 0 0	91 X[5:0] A[5:0] B[5:0] C[5:0]	1 * * * *	0 * * * *	0 X ₅ A ₅ B ₅ C ₅	1 X ₄ A ₄ B ₄ C ₄	0 X ₃ A ₃ B ₃ C ₃	0 X ₂ A ₂ B ₂ C ₂	0 X ₁ A ₁ B ₁ C ₁	1 X ₀ A ₀ B ₀ C ₀	Set Look Up Table (LUT)	Set current drive pulse width of Bank 0, Color A, B and C. Bank 0: X[5:0] = 31... 63; for pulse width set to 32 ~ 64 clocks (RESET = 110001b) Color A: A[5:0] same as above (RESET = 111111b) Color B: B[5:0] same as above (RESET = 111111b) Color C: C[5:0] same as above (RESET = 111111b) Note: color D pulse width is fixed at 64 clocks pulse.

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	92	1	0	0	1	0	0	1	0	Set bank color of for bank 1-16 (Page 0)	A[1:0] : 00, 01, 10, or 11 for Color = A, B, C or D of bank 1
0	A[7:0]	A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		A[3:2] : 00, 01, 10, or 11 for Color = A, B, C or D of bank 2
0	B[7:0]	B ₇	B ₆	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀		:
0	C[7:0]	C ₇	C ₆	C ₅	C ₄	C ₃	C ₂	C ₁	C ₀		:
0	D[7:0]	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀		D[7:6] : 00, 01, 10, or 11 for Color = A, B, C or D of bank 16
0	93	1	0	0	1	0	0	1	1	Set bank color of for bank 17-32 (Page 1)	A[1:0] : 00, 01, 10, or 11 for Color = A, B, C or D of bank 17
0	A[7:0]	A ₇	A ₆	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		A[3:2] : 00, 01, 10, or 11 for Color = A, B, C or D of bank 18
0	B[7:0]	B ₇	B ₆	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀		:
0	C[7:0]	C ₇	C ₆	C ₅	C ₄	C ₃	C ₂	C ₁	C ₀		:
0	D[7:0]	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀		D[7:6] : 00, 01, 10, or 11 for Color = A, B, C or D of bank 32
0	A0~A1	1	0	1	0	0	0	0	X ₀	Set Segment Re-map **	X ₀ =0: column address 0 is mapped to SEG0 (RESET) X ₀ =1: column address 131 is mapped to SEG0
0	A4~A5	1	0	1	0	0	1	0	X ₀	Set Entire Display ON/OFF **	X ₀ =0: normal display (RESET) X ₀ =1: entire display ON
0	A6~A7	1	0	1	0	0	1	1	X ₀	Set Normal/Inverse Display **	X ₀ =0: normal display (RESET) X ₀ =1: inverse display
0	A8	1	0	1	0	1	0	0	0	Set Multiplex Ratio **	The next command, A[5:0] determines multiplex ratio N from 16MUX-64MUX, RESET= 64MUX
0	A[5:0]	*	*	A ₅	A ₄	A ₃	A ₂	A ₁	A ₀		
0	AA	1	0	1	0	1	0	1	0	NOP	Reserved, do not use
0	AB	1	0	1	0	1	0	1	1	NOP	Reserved, do not use
0	AD	1	0	1	0	1	1	0	1	Set DC-DC on/off	X ₀ : 1 DC-DC will be turned on when display on (RESET) 0 DC-DC is disable
0		1	0	0	0	1	0	1	X ₀		
0	AE~AF	1	0	1	0	1	1	1	X ₀	Set Display ON/OFF **	X ₀ =0: turns OFF OLED panel (RESET) X ₀ =1: turns ON OLED panel
0	B0~BF	1	0	1	1	X ₃	X ₂	X ₁	X ₀	Set Page Address **	Set GDDRAM Page Address (0-7) for read/write using X ₃ X ₂ X ₁ X ₀
0	C0/C8	1	1	0	0	X ₃	*	*	*	Set COM Output Scan Direction **	X ₃ =0: normal mode (RESET) Scan from COM 0 to COM [N-1] X ₃ =1: remapped mode. Scan from COM [N-1] to COM0 Where N is the Multiplex ratio.
0	D0-D1	1	1	0	1	0	0	0	X ₀	Reserved	Reserved, do not use

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0 0	D3 A[5:0]	1 *	1 *	0 A ₅	1 A ₄	0 A ₃	0 A ₂	1 A ₁	1 A ₀	Set Display Offset **	Set vertical scroll by COM from 0-63. The value is reset to 00H after RESET.
0 0	D5 A[7:0]	1 A ₇	1 A ₆	0 A ₅	1 A ₄	0 A ₃	1 A ₂	0 A ₁	1 A ₀	Set Display Clock Divide Ratio/Oscillator Frequency	A[3:0] Define the divide ratio of the display clocks (DCLK): Divide ratio= A[3:0] + 1, RESET is 0000b (divide ratio = 1) A[7:4] Set the Oscillator Frequency. Oscillator Frequency increases with the value of A[7:4] and vice versa. RESET is 0111b
0 0	D8 0	1 0	1 0	0 X ₅	1 X ₄	1 0	0 X ₂	0 0	0 X ₀	Set area color mode on/off & low power display mode	X ₅ X ₄ = 00 (RESET) : mono mode X ₅ X ₄ = 11 Area Color enable X ₂ =0 and X ₀ =0: Normal (RESET) power mode X ₂ =1 and X ₀ =1: Set low power save mode
0 0	D9 A[7:0]	1 A ₇	1 A ₆	0 A ₅	1 A ₄	1 A ₃	0 A ₂	0 A ₁	1 A ₀	Set Pre-charge period**	A[3:0] Phase 1 period of up to 15 dclk clocks [RESET=2h]; 0 is invalid entry A[7:4] Phase 2 period of up to 15 dclk clocks [RESET=2h]; 0 is invalid entry
0 0	DA 0	1 0	1 0	0 0	1 X ₄	1 0	0 0	1 1	0 0	Set COM pins hardware configuration	X ₄ =0, Sequential COM pin configuration (i.e. COM31, 30, 29....0 ; SEG0-132; COM31,32....62,63) X ₄ =1(RESET), Alternative COM pin configuration (i.e. COM62,60,58,...2,0; SEG0-132; COM1,3,5...61,63)
0 0	DB A[6:0]	1 *	1 A ₆	0 A ₅	1 A ₄	1 A ₃	0 A ₂	1 A ₁	1 A ₀	Set VCOM Deselect Level	A[6:0] 0000000 low VCOM deselect level (~ 0.43 Vref) 0110101 normal VCOM deselect level (~ 0.77*Vref (RESET)) 1111111 high VCOM deselect level (equal Vref)
0	E2	1	1	1	0	0	0	1	0	Reserved	Reserved
0	E3	1	1	1	0	0	0	1	1	NOP **	Command for No Operation
0	F*	1	1	1	1	*	*	*	*	Reserved	Reserved, do not use

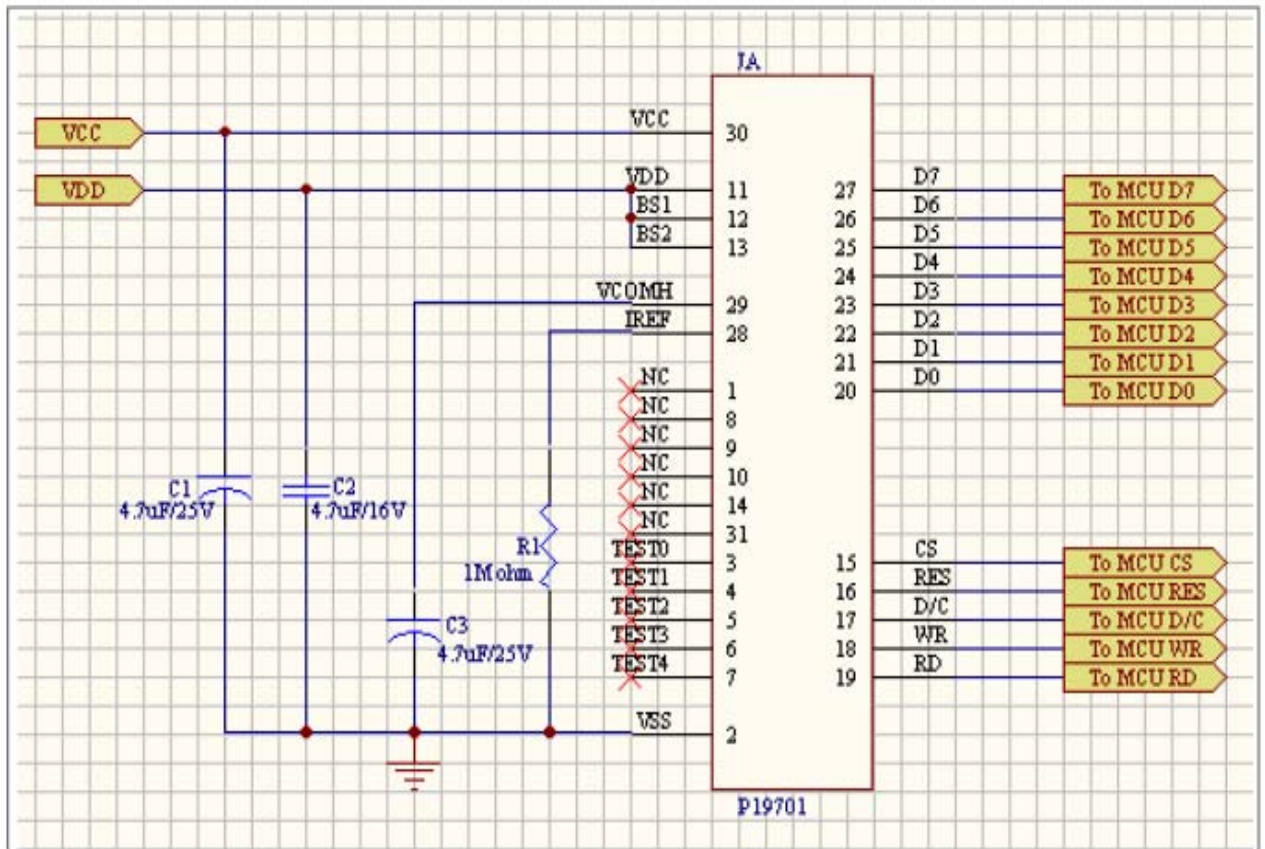
(D/C=0, R/W (WR#)=1, E (RD#)=1 for 6800 or E (RD#)=0 for 8080)

Bit Pattern	Command	Description
D ₇ D ₆ D ₅ D ₄ D ₃ D ₂ D ₁ D ₀	Status Register Read *	D ₇ : Reserve D ₆ : "1" for display OFF / "0" for display ON D ₅ : Reserve D ₄ : Reserve D ₃ : Reserve D ₂ : Reserve D ₁ : Reserve D ₀ : Reserve

Note: Patterns other than those given in the Command Table are prohibited to enter the chip as a command; as unexpected results can occur.

10 Application

10.1 Application Circuit



Recommended components

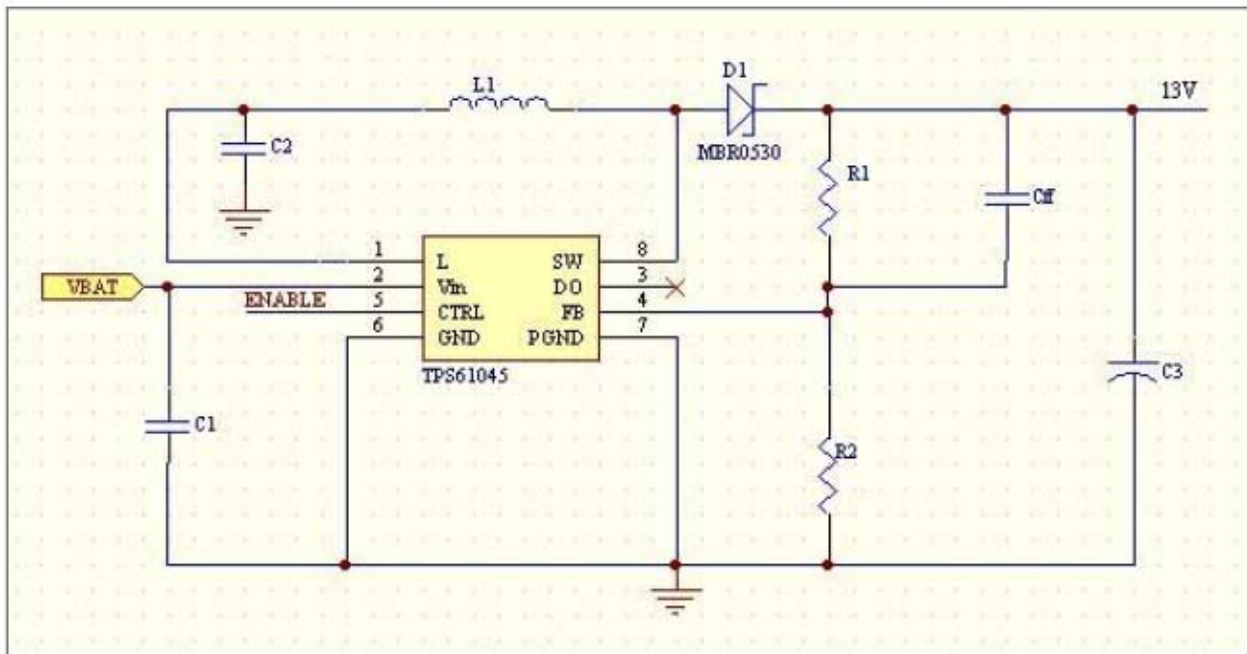
R1 : 1M ohm (0603),1%.

C1 : 4.7uF (Tantalum Type) / 25V, C2 : 4.7uF (0805) / 16V ,

C3 : 4.7uF (Tantalum Type) / 25V.

This circuit is designed for 8080 8-bits interface.

10.2 External DC-DC application circuit



Recommended components

C1: 0.1uF(0603) / 25V, C2 : 4.7uF (Tantalum Type) / **25V**,

C3 : 4.7uF (Tantalum Type) / 25V.

Cff : 22pF(0603) / 16V.

D1:Schottky Diode.

L1: 10uH.

R1: 1.2M ohm (0603), 1%, R2: 127K ohm (0603), 1%.

VBAT = 1.8V ~ 6.0V(The Detail Application,please refer the IC data sheet).

10.3 Initial software

```
void OM_ini()
{
    write_com(0xae);    //Set Display ON/OFF
    write_com(0xad);    //master configuration
        write_com(0x8a);    //second byte
    write_com(0xa8);    //Set Mux
        write_com(0x3f);    //64mux
    write_com(0xa0);    //Set Segment Re-map (0xa0 normal,0xa1 reverse)
    write_com(0xc8);    //Set COM Output Scan Direction (0xc0 normal,0xc8 reverse)
    write_com(0xa6);    //set normal/inverse display (normal)
    write_com(0xa4);    //set entire display (normal)
    write_com(0x81);    //set contrast control
        write_com(0x8f);    //second byte
    write_com(0xd5);    //Set Display Clock Divide Ratio/Oscillator Frequency
        write_com(0x70);    //105hz
    write_com(0xd8);    //Set Area Color Mode ON/OFF & LowPower Display Mode
        write_com(0x00);    //second byte
    write_com(0xd9);    //set pre-charge period
        write_com(0x61);    //set discharge/precharge
    write_com(0xaf);    //Set Display ON
}
```

11 Precautions for operation and Storage

11.1 Precautions for Operation

- (1) Since OLED panel is made of glass, in order to prevent from glass broken, please do not apply any mechanical shock or impact or excessive force to it when installing the OLED module. Any strong mechanical impact due to falling dropping etc. may cause damage (breakage or cracking).
- (2) The polarizer on the OLED surface is made of soft material and is easily scratched. Please take most care when handing.
- (3) If OLED surface is contaminated, please wipe it off gently by using moisten soft cloth with normal ethanol, do not use acetone, ketone, isopropyl alcohol or water. If there is saliva or water on the OLED surface, please wipe it off immediately.
- (4) When handling OLED module, please be sure that the body and the tools are properly rounded. And do not touch I/O pins with bare hands or contaminate I/O pins, it will cause disconnection or defective insulation of terminals.
- (5) Do not attempt to disassemble or process the OLED module.
- (6) OLED module should be used under recommended operating conditions shown in the specification. Since the higher voltage leads to the shorter lifetime, be sure to use the specified operating voltage.
- (7) Foggy dew, moisture condensation or water droplets deposited on surface and contact terminals will cause polarizer stain or damage, the deteriorated display quality and electrochemical reaction then leads to the shorter life time and permanent damage to the module probably. Please pay attention to the environmental temperature and humidity.

11.2 Soldering

- (8) Use the high quality solder. (60-63% tin mixed with lead)
- (9) Iron: no higher than 260°C and less than 3~4 sec during soldering.
- (10) Soldering: only to the I/O terminals.
- (11) Rewiring: no more than 3 times.

11.3 Precautions for Storage

- (12) Please store OLED module in a dark place, avoid exposure to sunlight, the light of fluorescent lamp or any ultraviolet ray.
- (13) Keep the environment temperature at between 10°C and 35°C and the relative humidity less than 60%. Avoid high temperature, high humidity.
- (14) That keeps the OLED modules stored in the container shipped from supplier before using them is recommended.
- (15) Do not leave any article on the OLED module surface for an extended period of time.

11.4 Warranty period

Multi-Inno Technology Co. Ltd. warrants for a period of 12 months from the shipping date when stored or used under normal condition

**12 Test Status**

TEST ITEM	TEST CONDITION	QUANTITY
High temperature storage	85°C,120 hours	3pcs
Low temperature storage	-40°C,120 hours	3pcs
Humidity (storage)	60°C, 90%RH, 120hours	3pcs
Low temperature (operating)	-40°C, 120 hours	3pcs
High temperature (operating)	80°C, 120hours	3pcs

Note: After test 2 hours (room temperature), check function & appearance.